Programmable Interval Timer - 8254

CEN433

King Saud University

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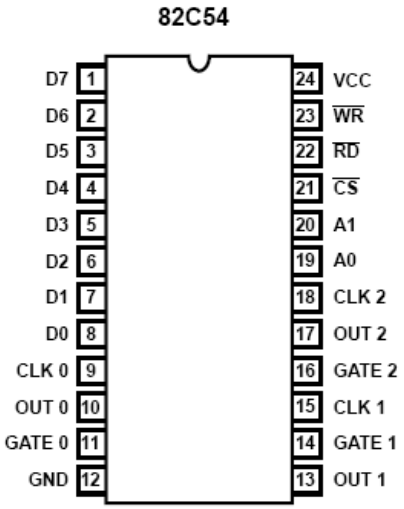
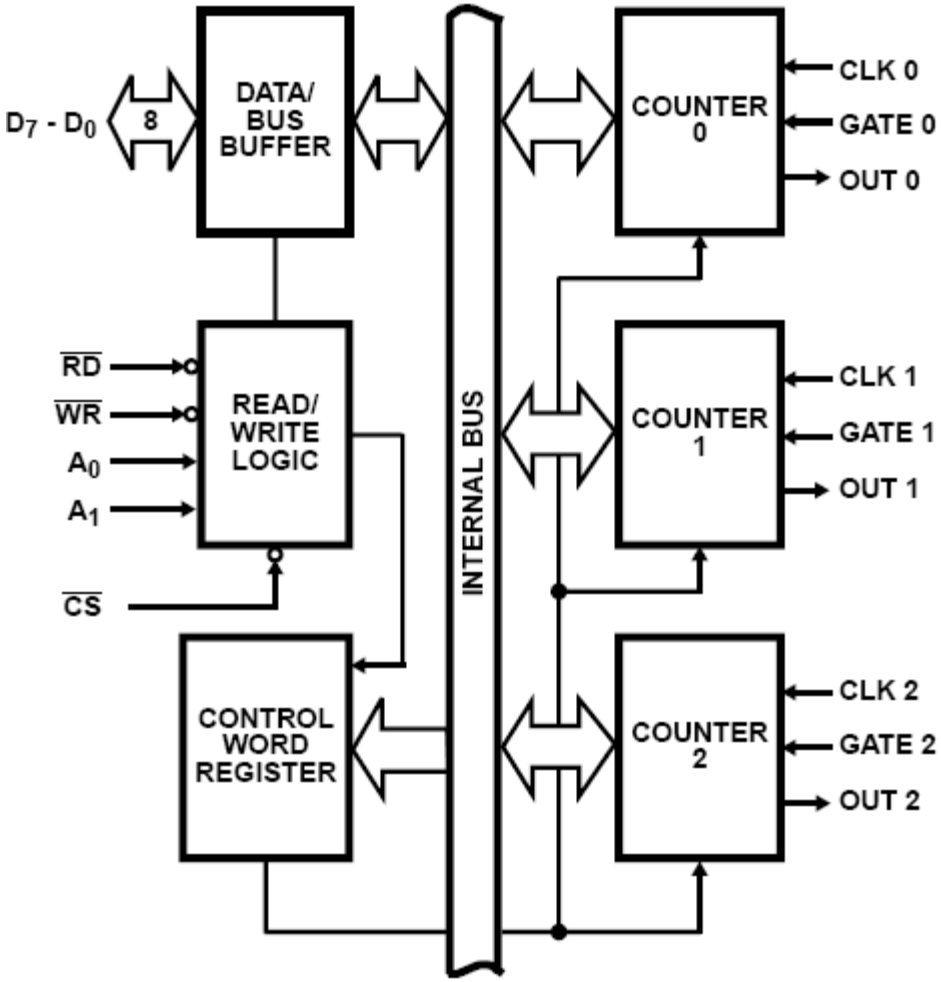
Functional Diagram





Control Word Format

A1, A0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC - Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

RW - Read/Write

RW1	RW0	
0	0	Counter Latch Command (See Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

M - Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD - Binary Coded Decimal

0	Binary Counter 16-bit
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE: Don't Care bits (X) should be 0 to insure compatibility with future products.

Modes of Operation

Mode 0: Interrupt on Terminal Count

Mode 1: Hardware ~~Retriggerable~~ One-Shot

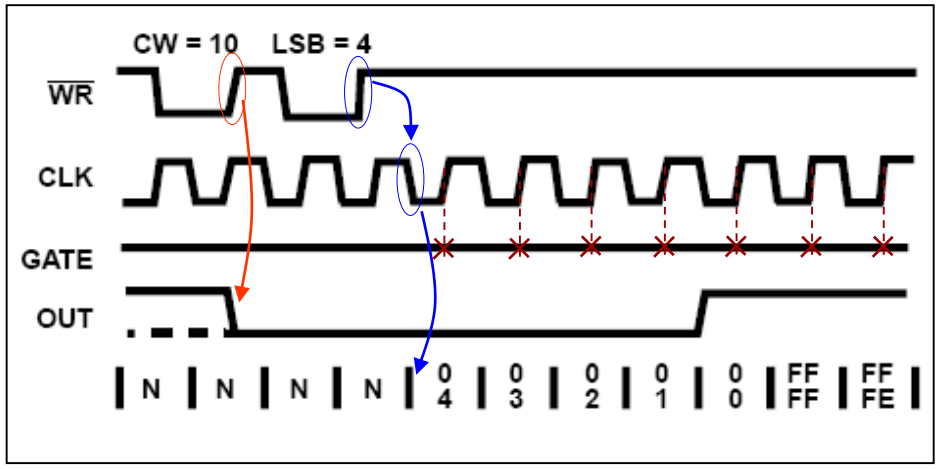
Mode 2: ~~Rate~~ pulse Generator

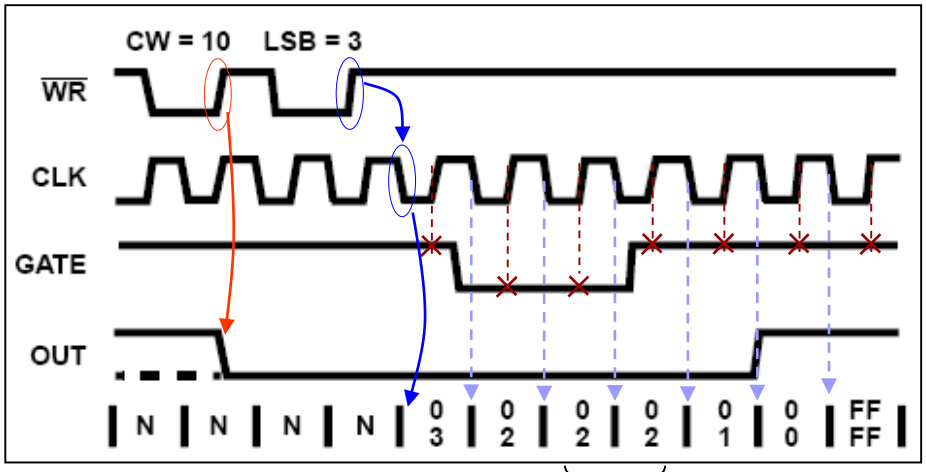
Mode 3: Square Wave ~~Mode~~ generator

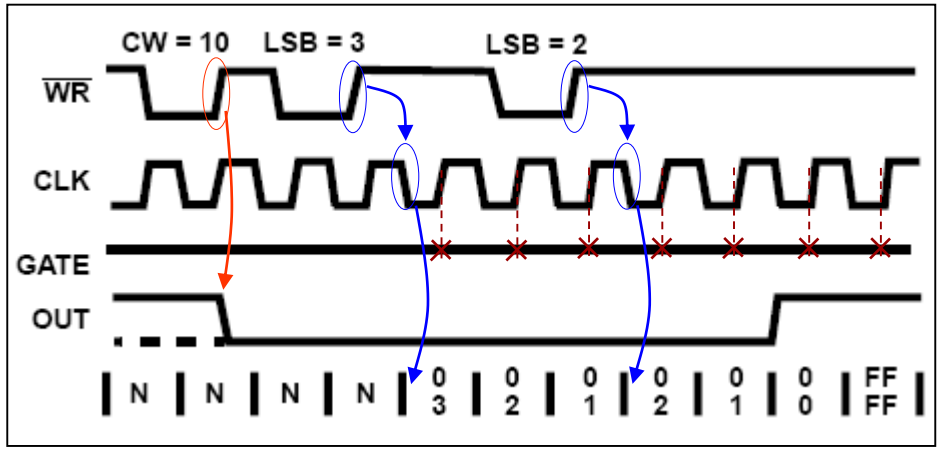
Mode 4: Software Triggered ~~Mode~~ strobe

Mode 5: Hardware Triggered ~~Mode~~ strobe

Mode 0: Interrupt on Terminal Count

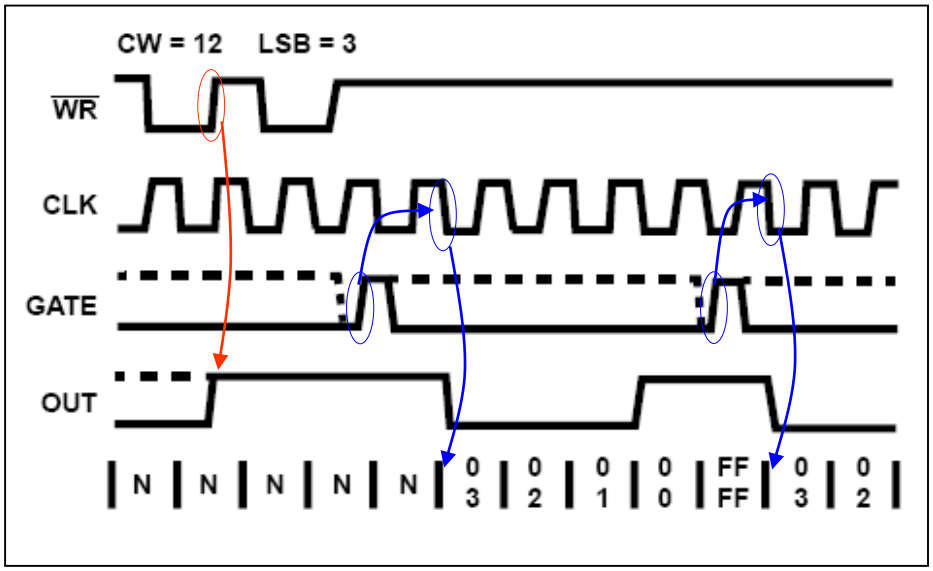


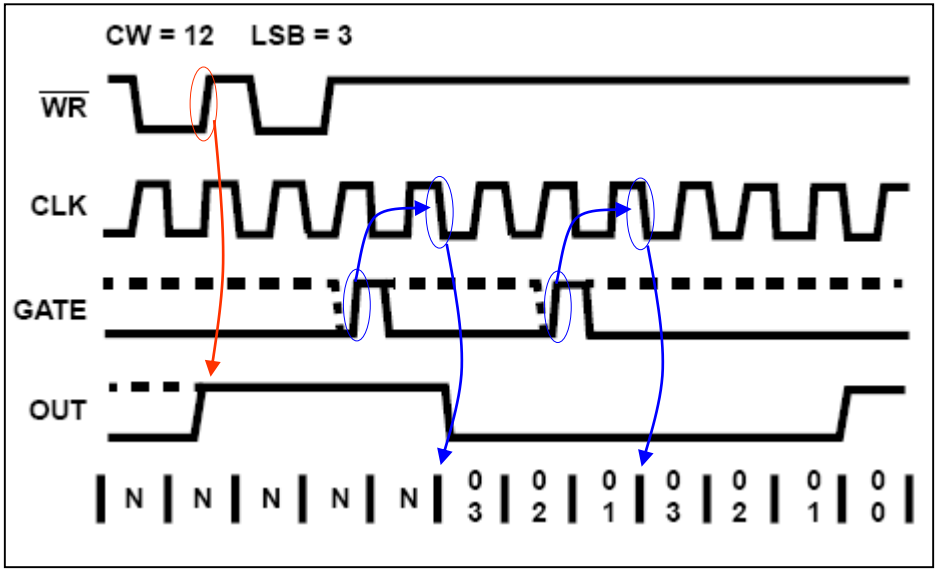


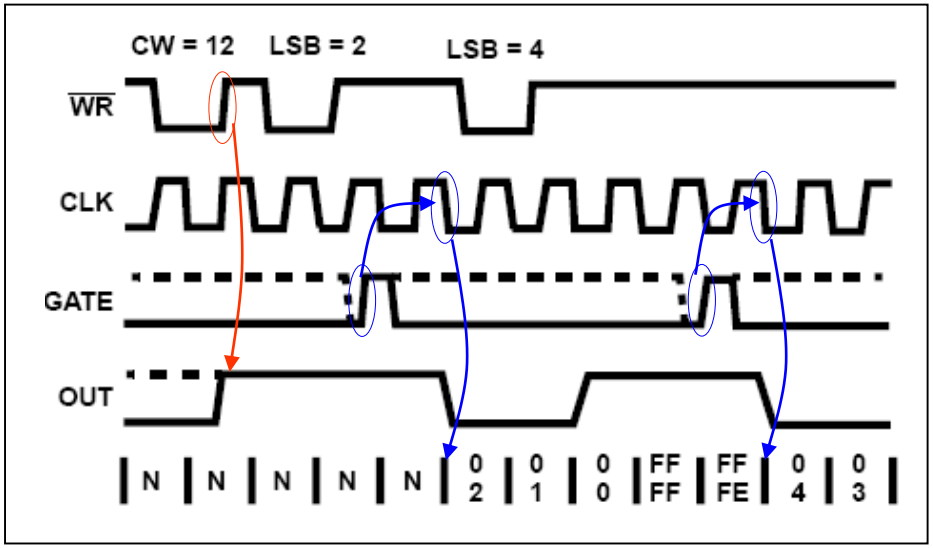


- At the rising edge of WR/ (Control Word), OUT = low.
- At the first falling edge of CLK after the rising edge of WR/ (LSB), CR→CE.
- GATE is level sensitive.
- GATE is sampled at the rising edge of CLK.
- Decrement the counter at the falling edge, if the sample of GATE is high. Otherwise, freeze.

Mode 1: Hardware Retriggerable One-Shot

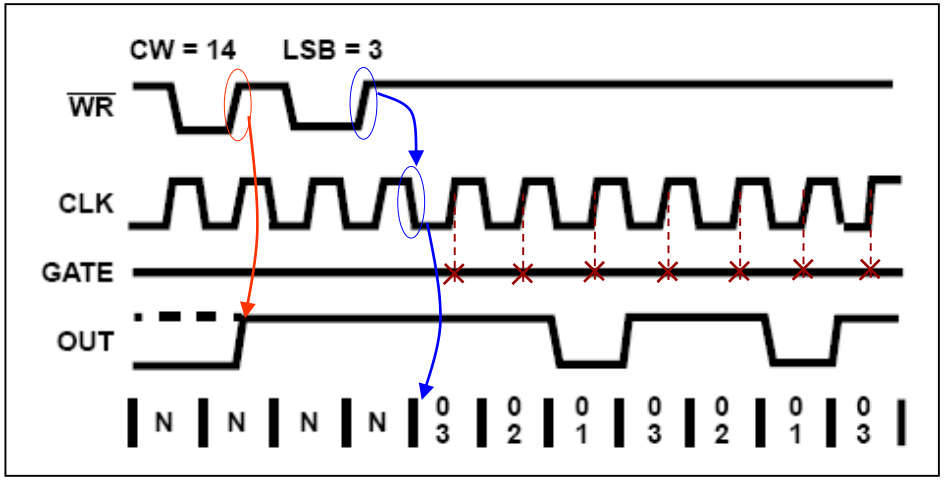


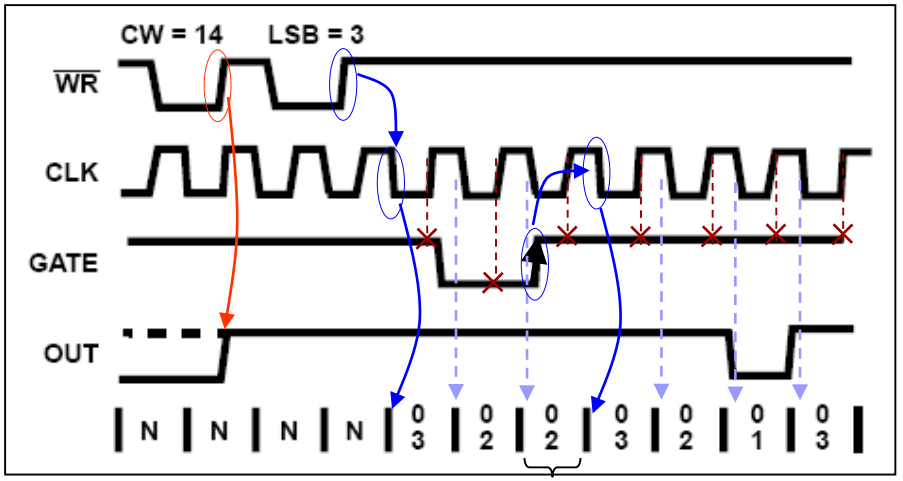


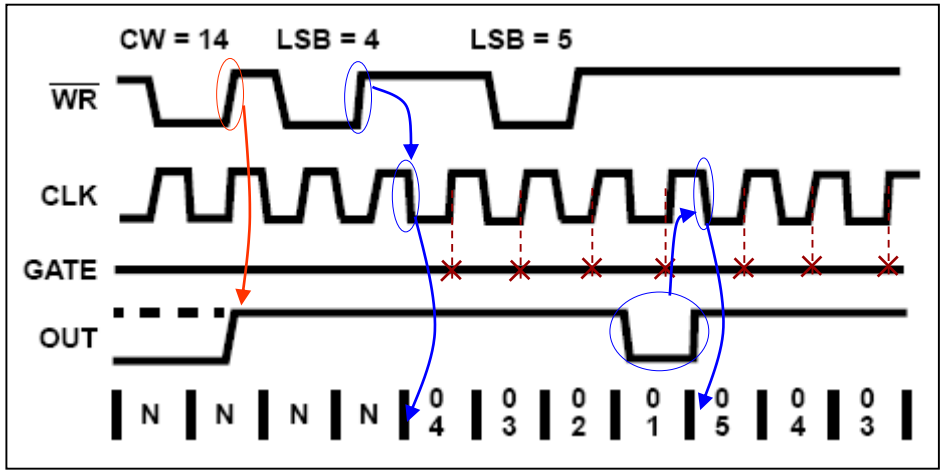


- At the rising edge of WR/ (Control Word), OUT = high.
- At the first falling edge of CLK after the rising edge of GATE, CR→CE.
- At the first falling edge of CLK after the rising edge of GATE, reinitialize CE with the last value written to CR.

Mode 2: Rate Generator

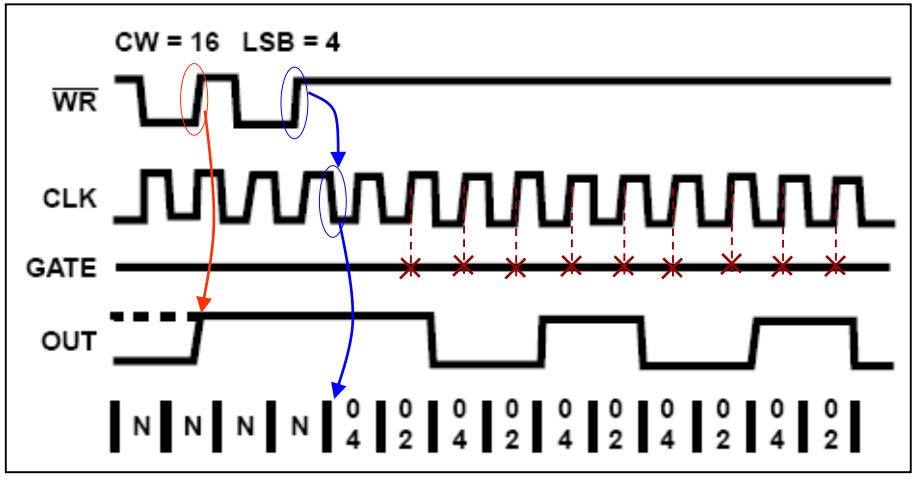


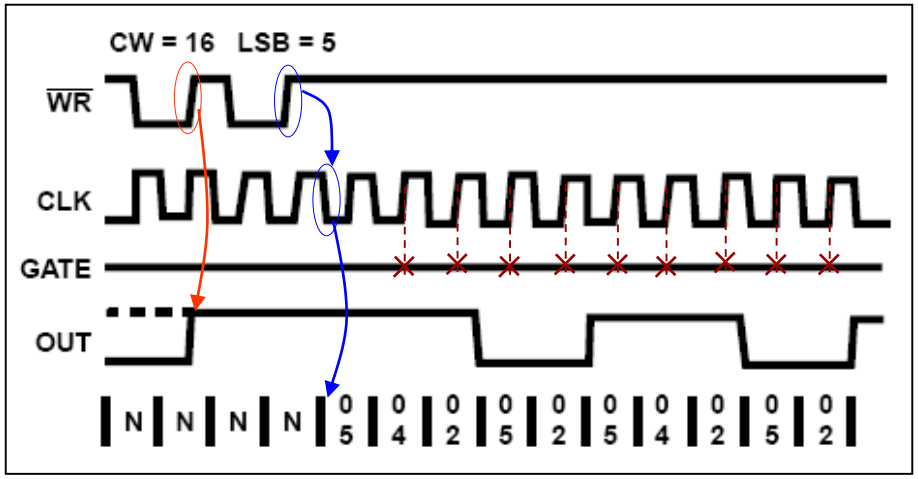


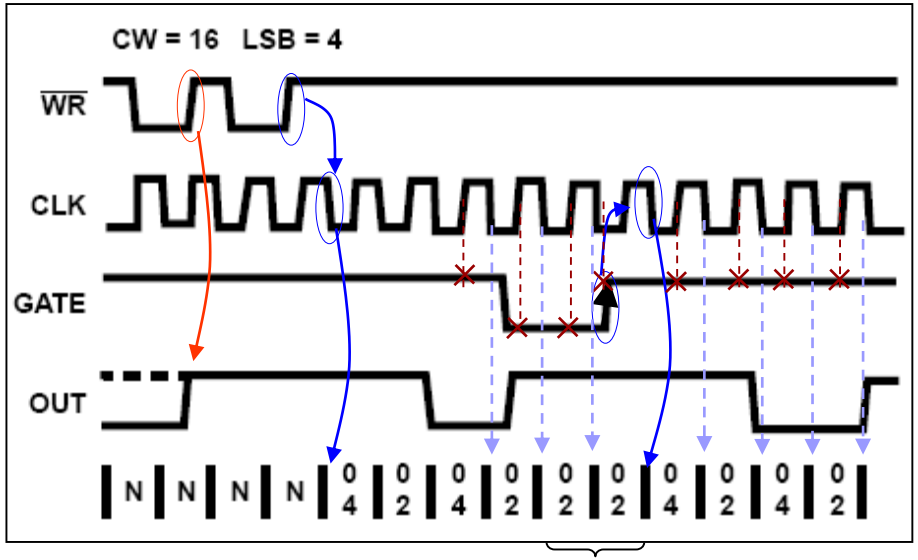


- At the rising edge of WR/ (Control Word), OUT = high.
- At the first falling edge of CLK after the rising edge of WR/ (LSB), CR→CE.
- When counter reaches to value 1, it is reloaded with the value of CR at the next falling edge of CLK.
- GATE is sampled at the rising edge of CLK.
- Decrement the counter at the falling edge, if the sample of GATE is high. Otherwise, freeze.
- At the first falling edge of CLK after the rising edge of the GATE, reinitialize CE.

Mode 3: Square Wave Mode

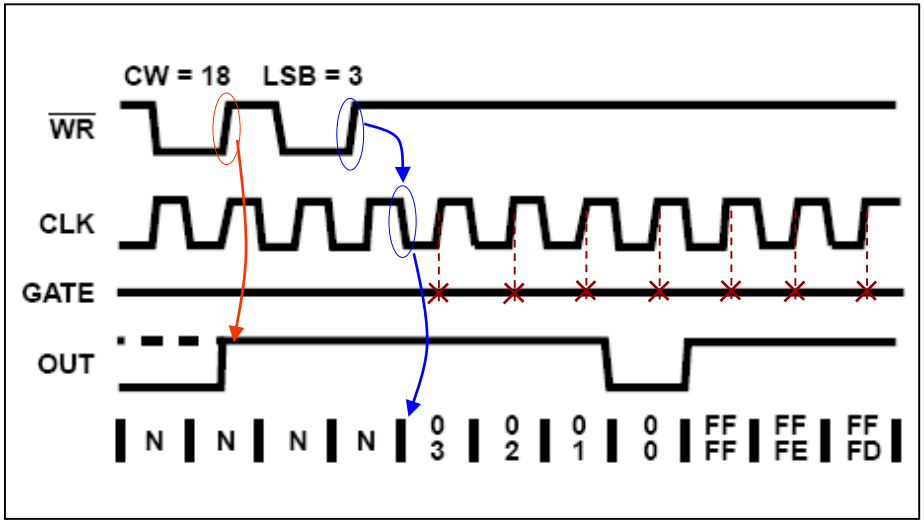


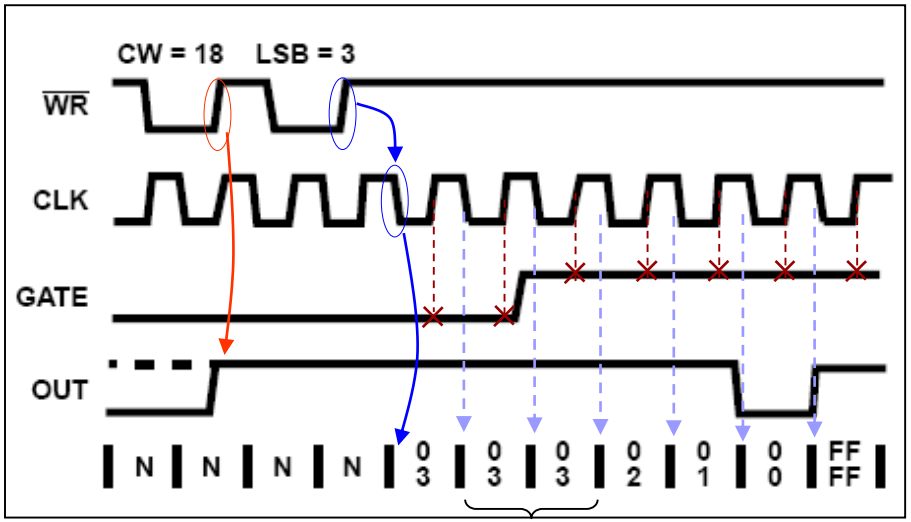


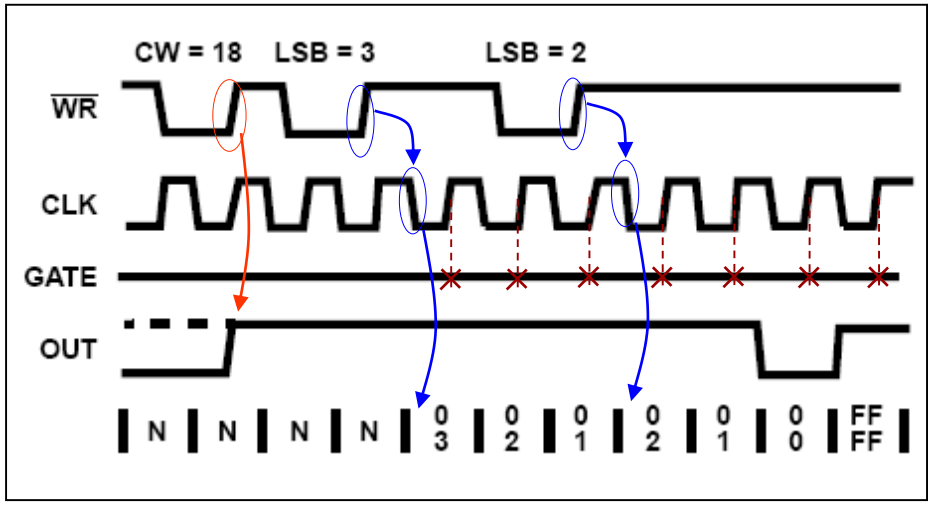


- At the rising edge of WR/ (Control Word), OUT = high.
- At the first falling edge of CLK after the rising edge of WR/ (LSB), CR→CE.
- GATE is sampled at the rising edge of CLK.
- At the first falling edge of CLK after the rising edge of the GATE, reinitialize CE.

Mode 4: Software Triggered Mode

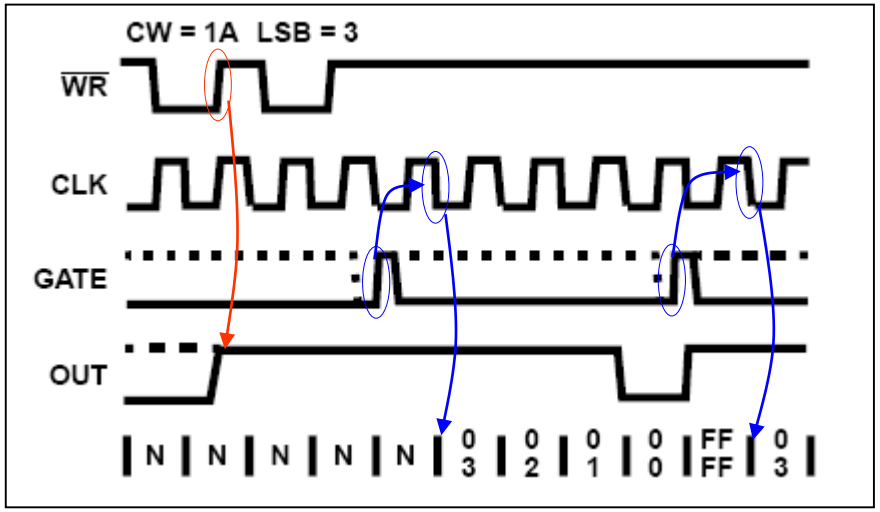


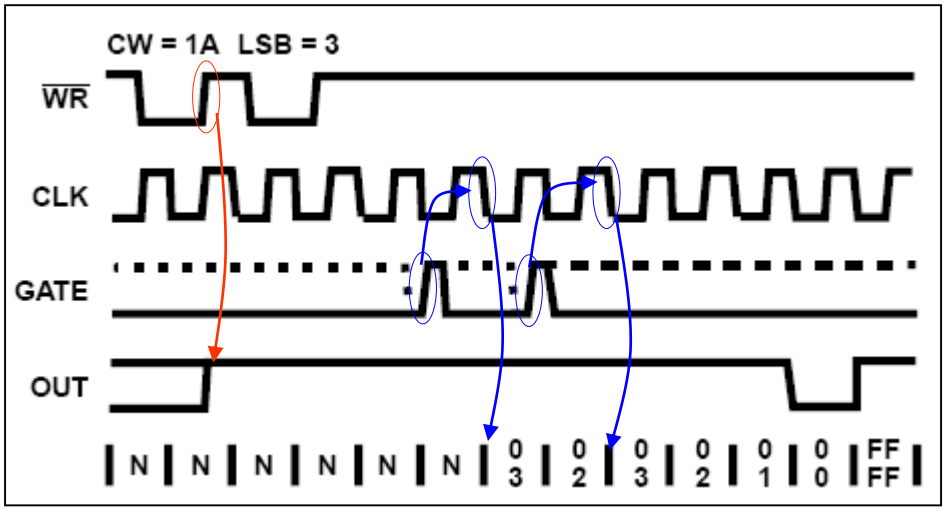


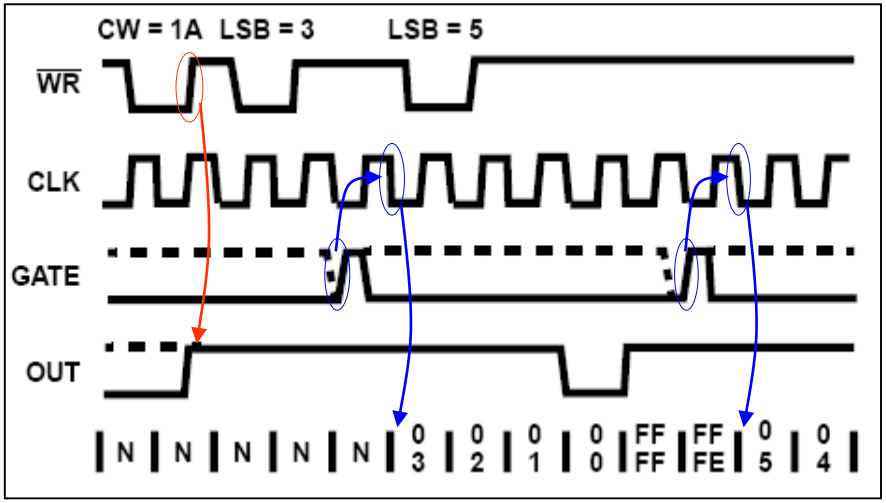


- At the rising edge of WR/ (Control Word), OUT = high.
- At the first falling edge of CLK after the rising edge of WR/ (LSB), CR→CE.
- GATE is level sensitive.
- GATE is sampled at the rising edge of CLK.
- Decrement the counter at the falling edge, if the sample of GATE is high. Otherwise, freeze.
- When counter reaches to zero, it wraps around to the highest value.

Mode 5: Hardware Triggered Mode

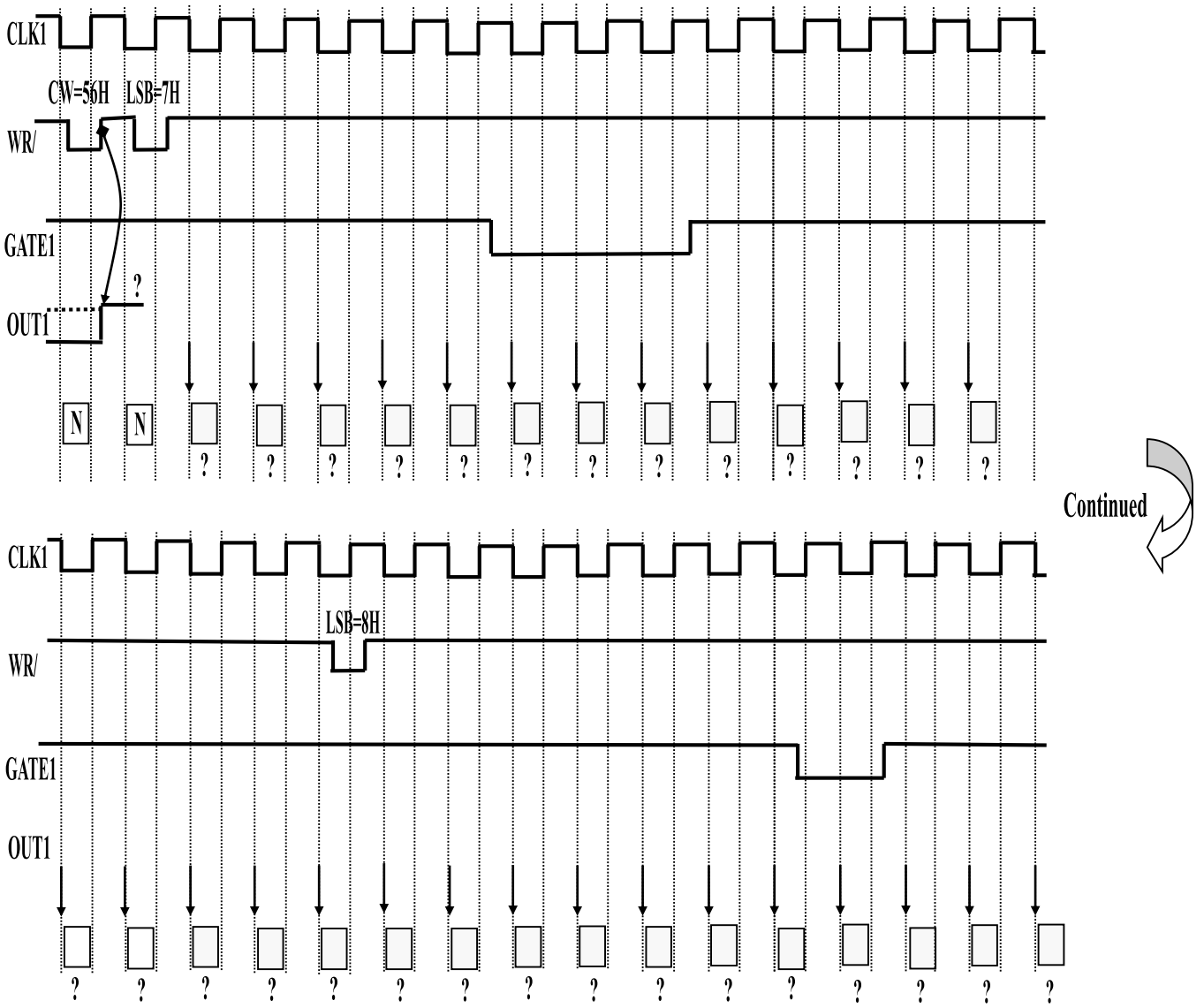






- At the rising edge of WR/ (Control Word), OUT = high.
- At the first falling edge of CLK after the rising edge of GATE, CR→CE.
- At the first falling edge of CLK after the rising edge of GATE, reinitialize CE with the last value written to CR.
- When counter reaches to zero, it wraps around to the highest value.

Example 15


CLK1
CW=56H
LSB=7H
WR/
GATE1
OUT1
?
N
N
Continued
CLK1
LSB=8H
WR/
GATE1
OUT1