Information Technology Institute

9 Month Program

Digital IC Design Track

Project (1)

“Design of 4:16 Decoder for Speed”

Instructor: Dr Hesham Omran

Objective: To design a 4:16 decoder as in Section 4.5.3 in the textbook (Weste and Harris) with a high speed (minimum delay) using Synopsys' Custom Compiler & 32 nm SAED PDK

Deliverables:

[1] Normalized delay vs h plot for each of the following gates (INV, NAND2, NAND4, NOR2, NOR4). Consider ONLY the worst-case input of the gate. Justify your selection.

This part can be easily implemented using the netlists of these gates. It is important to note that:

- In order to plot the delay vs h, a fanout circuit is needed, so every gate of these will be considered the design under test in a chain of gates of the same type for a FO4 to shape the inputs & outputs & get a useful plot.

- It is asked to consider the worst cases. The worst case for a NAND is the inner input (closest to the out node) arriving before the other inputs (Always = VDD), thus it will have to wait (delay) for them to arrive for the inner caps to discharge. As for NOR, It's for the inner input (Closest to Out) to be = GND, bec. NORs have series PMOS chains.

So one of the Ins of the NAND will always be connected to VDD & one of those of the NOR will always be to GND.

The Steps To Implement This Part:

1) Create a folder on your desktop top place your project
2) Create a directory (folder) named after each gate you'll implement.
3) Create a file for the netlist in every folder. Call it e.g. INV.sp
4) Write your netlist in it & save
5) Open the terminal in the directory of your file & run the command: hspice INV.sp.

6) Check the delays in the report that appears.

7) Run this command to open the waveform viewer:
/mnt/ext/synopsys/primewave/U-2023.03-SP2/linux64/swv/bin/swv &

8) Once it opens. Click File -> Open waveform -> Choose the file that ends with mt0 e.g. NAND.mt0. This is the measure output file that holds the results of the measure command.

9) Go to “utilities” choose parametric plot then click “select files” & choose tpd & h to plot and choose X-Y Panel. Click the “measurement tool” icon & choose: Difference (To get g) & “Data(x,y) to get the y intercept (p).

The results should be as follows:

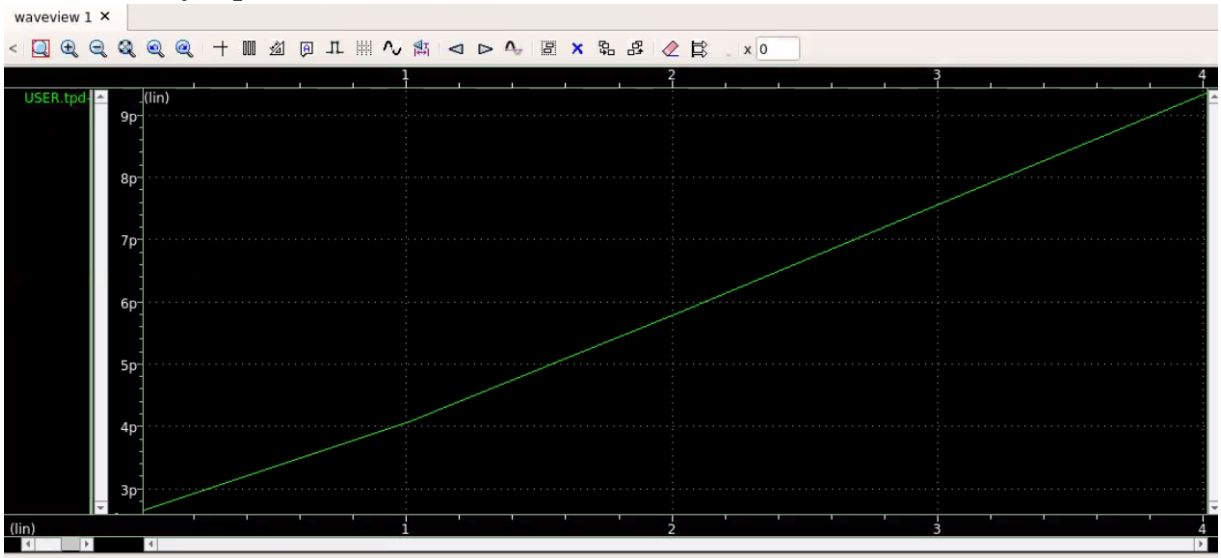
For The Inverter:

1) The Netlist:

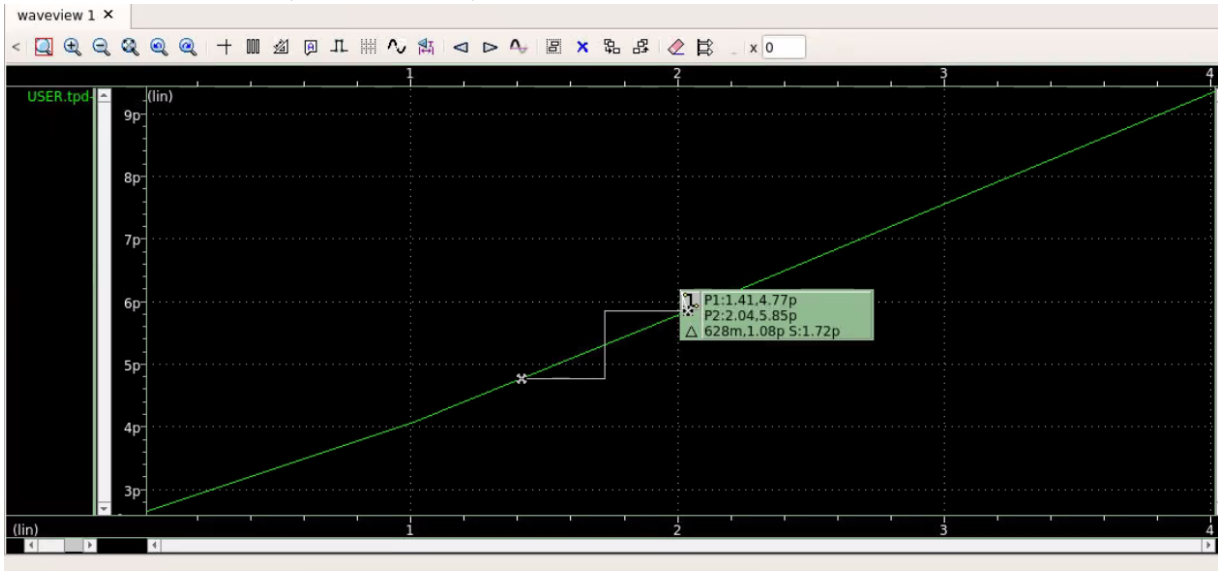
```
* inv.sp
*-----------------------------------------------------------------------
* Parameters and models
*-----------------------------------------------------------------------
.param SUPPLY=1.05
.param H=4
.option scale=15n
.lib '/mnt/ext/synopsys/pdks/32nm/install/pdk/SAED32nm_PDK_04152022/hspice/saed32nm.lib'TT
.temp 70
.option post

* Subcircuits
*-----------------------------------------------------------------------
.global vdd gnd
.subckt inv a y N=7 P=14
xm0 y a gnd gnd n105 w='N' l=2
+ AS='N*5' PS='2*N+10' AD='N*5' PD='2*N+10'
xm1 y a vdd vdd p105 w='P' l=2
+ AS='P*5' PS='2*P+10' AD='P*5' PD='2*P+10'
.ends
*-----------------------------------------------------------------------
* Simulation netlist
*-----------------------------------------------------------------------
Vdd vdd gnd 'SUPPLY'
Vin a gnd PULSE 0 'SUPPLY' 0ps 20ps 20ps 120ps 280ps
X1 a b inv * shape input waveform
X2 b c inv M='H' * reshape input waveform
X3 c d inv M='H**2' * device under test
X4 d e inv M='H**3' * load
X5 e f inv M='H**4' * load on load
*-----------------------------------------------------------------------
* Stimulus
*-----------------------------------------------------------------------
.tran 0.1ps 280ps SWEEP H 0.01 4.01 1
.MEASURE TRAN tpdr TRIG  v(c)=0.5 FALL=1 TARG  v(d)=0.5 RISE=1
.MEASURE TRAN tpdf TRIG  v(c)=0.5 RISE=1 TARG  v(d)=0.5 FALL=1
.MEASURE TRAN trise TRIG  v(d)='0.2*1.0' RISE=1 TARG  v(d)='0.8*1.0' RISE=1
.MEASURE TRAN tfall TRIG  v(d)='0.8*1.0' FALL=1 TARG  v(d)='0.2*1.0' FALL=1
.MEASURE tpd PARAM '(tpdr+tpdf)/2'
.end
```

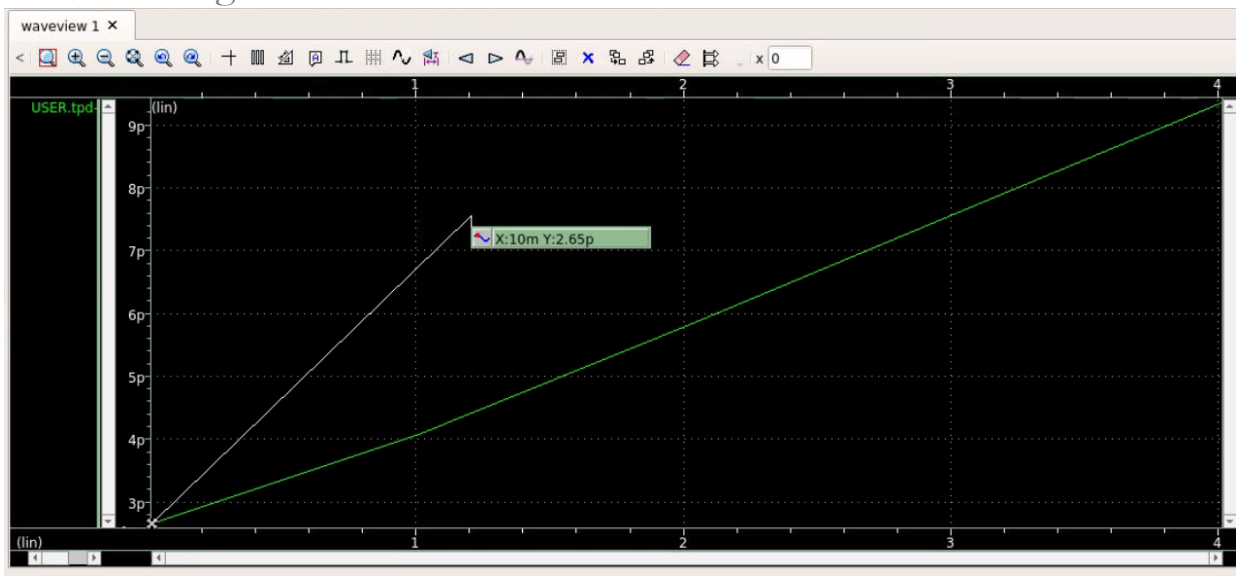
2) Delay (tpd) VS h



3) Getting g (Value of S)



4) Getting P



5) Normalization of g & P

g = 1.72/1.72 = 1

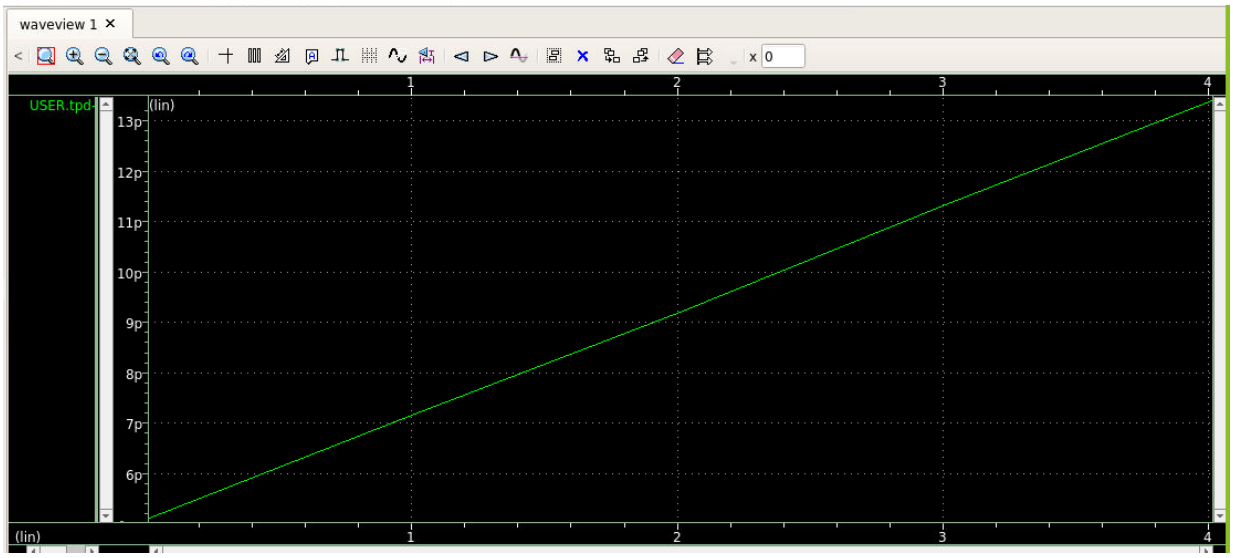
p = 2.65/1.72 = 1.54

For The NAND2:

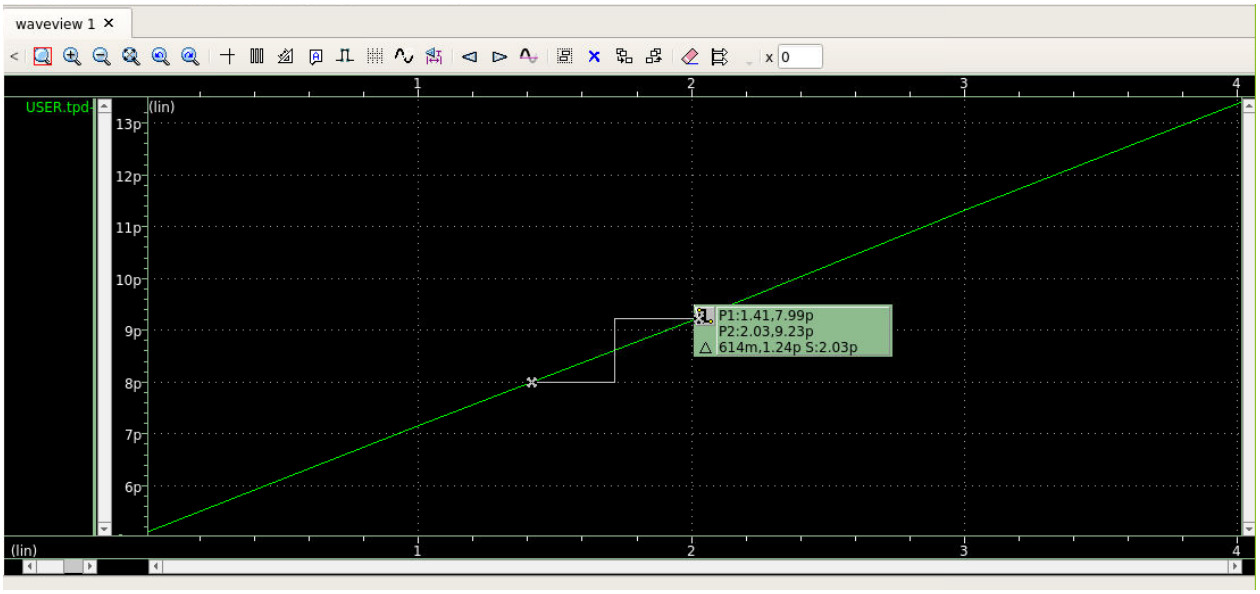
1) The Netlist:

```
* NAND2.sp
*-----------------------------------------------------------------------
* Parameters and models
*-----------------------------------------------------------------------
.param SUPPLY=1.05
.param H=4
.option scale=15n
.lib '/mnt/ext/synopsys/pdks/32nm/install/pdk/SAED32nm_PDK_04152022/hspice/saed32nm.lib'TT
.temp 70
.option post
*-----------------------------------------------------------------------
* Subcircuits
*-----------------------------------------------------------------------
.global vdd gnd
.subckt NAND a y N=7 P=14
xm0 y vdd x gnd n105 w='2*N' l=2
+ AS='2*N*5' PS='2*2*N+10' AD='2*N*5' PD='2*2*N+10'
xm1 x a gnd gnd n105 w='2*N' l=2
+ AS='2*N*5' PS='2*2*N+10' AD='2*N*5' PD='2*2*N+10'
xm2 y a vdd vdd p105 w='P' l=2
+ AS='P*5' PS='2*P+10' AD='P*5' PD='2*P+10'
xm3 y vdd vdd vdd p105 w='P' l=2
+ AS='P*5' PS='2*P+10' AD='P*5' PD='2*P+10'
.ends
*-----------------------------------------------------------------------
* Simulation netlist
*-----------------------------------------------------------------------
Vdd vdd gnd 'SUPPLY'
Vin1 a gnd PULSE 0 'SUPPLY' 0ps 20ps 20ps 120ps 280ps
X1 a b NAND * shape input waveform
X2 b c NAND M='H' * reshape input waveform
X3 c d NAND M='H**2' * device under test
X4 d e NAND M='H**3' * load
X5 e f NAND M='H**4' * load on load
*-----------------------------------------------------------------------
* Stimulus
*-----------------------------------------------------------------------
.tran 0.1ps 280ps SWEEP H 0.01 4.01 1
.MEASURE TRAN tpdr TRIG  v(c)=0.5 FALL=1 TARG  v(d)=0.5 RISE=1
.MEASURE TRAN tpdf TRIG  v(c)=0.5 RISE=1 TARG  v(d)=0.5 FALL=1
.MEASURE TRAN trise TRIG  v(d)='0.2*1.0' RISE=1 TARG  v(d)='0.8*1.0' RISE=1
.MEASURE TRAN tfall TRIG  v(d)='0.8*1.0' FALL=1 TARG  v(d)='0.2*1.0' FALL=1
.MEASURE tpd PARAM '(tpdr+tpdf)/2'
.end
```

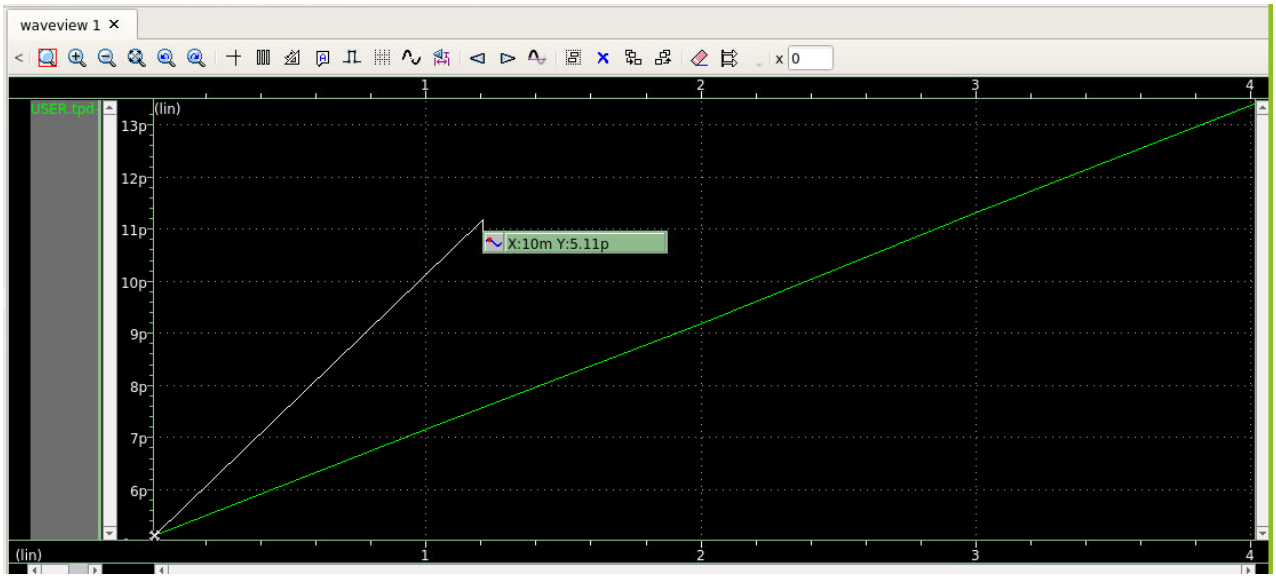
2) Delay (tpd) VS h



3) Getting g (Value of S)



4) Getting p



5) Normalization of g & p

g = 2.03/1.72 = 1.18

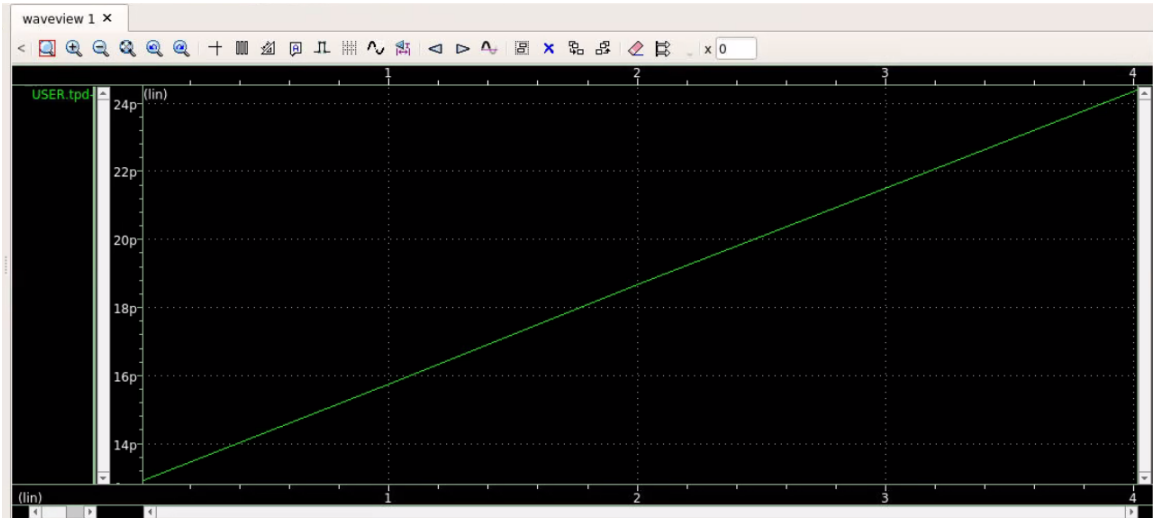
p = 5.11/1.72 = 2.97

For The NAND4:

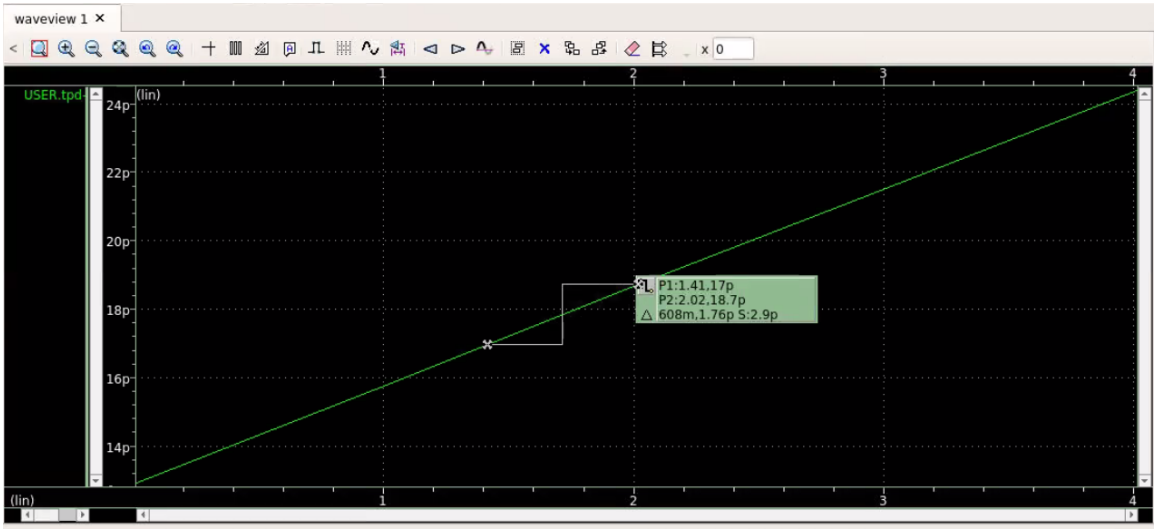
1) The Netlist:

```
* NAND4.sp
*---------------------------------------------------------------------
* Parameters and models
*---------------------------------------------------------------------
.param SUPPLY=1.05
.param H=4
.option scale=15n
.lib '/mnt/ext/synopsys/pdks/32nm/install/pdk/SAED32nm_PDK_04152022/hspice/saed32nm.lib'TT
.temp 70
.option post
*---------------------------------------------------------------------
* Subcircuits
*---------------------------------------------------------------------
.global vdd gnd
.subckt NAND a y N=7 P=14
----------------NMOS-----------------
xm0 y vdd x gnd n105 w='4*N' l=2
+ AS='4*N*5' PS='2*4*N+10' AD='4*N*5' PD='2*4*N+10'
xm1 x vdd z gnd n105 w='4*N' l=2
+ AS='4*N*5' PS='2*4*N+10' AD='4*N*5' PD='2*4*N+10'
xm2 z vdd r gnd n105 w='4*N' l=2
+ AS='4*N*5' PS='2*4*N+10' AD='4*N*5' PD='2*4*N+10'
xm3 r a gnd gnd n105 w='4*N' l=2
+ AS='4*N*5' PS='2*4*N+10' AD='4*N*5' PD='2*4*N+10'
----------------PMOS-----------------
xm4 y a vdd vdd p105 w='P' l=2
+ AS='P*5' PS='2*P+10' AD='P*5' PD='2*P+10'
xm5 y vdd vdd vdd p105 w='P' l=2
+ AS='P*5' PS='2*P+10' AD='P*5' PD='2*P+10'
xm6 y vdd vdd vdd p105 w='P' l=2
+ AS='P*5' PS='2*P+10' AD='P*5' PD='2*P+10'
xm7 y vdd vdd vdd p105 w='P' l=2
+ AS='P*5' PS='2*P+10' AD='P*5' PD='2*P+10'
.ends
*---------------------------------------------------------------------
* Simulation netlist
*---------------------------------------------------------------------
Vdd vdd gnd 'SUPPLY'
Vin1 a gnd PULSE 0 'SUPPLY' 0ps 20ps 20ps 120ps 280ps
X1 a b NAND * shape input waveform
X2 b c NAND M='H' * reshape input waveform
X3 c d NAND M='H**2' * device under test
X4 d e NAND M='H**3' * load
X5 e f NAND M='H**4' * load on load
*---------------------------------------------------------------------
* Stimulus
*---------------------------------------------------------------------
.tran 0.1ps 280ps SWEEP H 0.01 4.01 1
.MEASURE TRAN tpdr TRIG  v(c)=0.5 FALL=1 TARG  v(d)=0.5 RISE=1
.MEASURE TRAN tpdf TRIG  v(c)=0.5 RISE=1 TARG  v(d)=0.5 FALL=1
.MEASURE TRAN trise TRIG  v(d)='0.2*1.0' RISE=1 TARG  v(d)='0.8*1.0' RISE=1
.MEASURE TRAN tfall TRIG  v(d)='0.8*1.0' FALL=1 TARG  v(d)='0.2*1.0' FALL=1
.MEASURE tpd PARAM '(tpdr+tpdf)/2'
.end
```

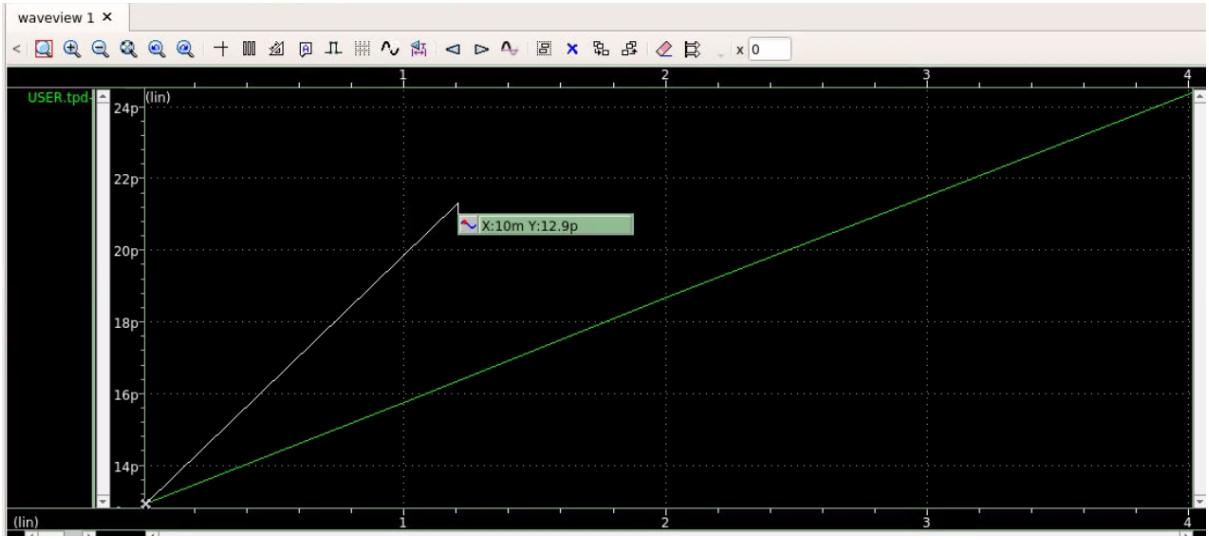
2) Delay (tpd) VS h



3) Getting g



4) Getting p



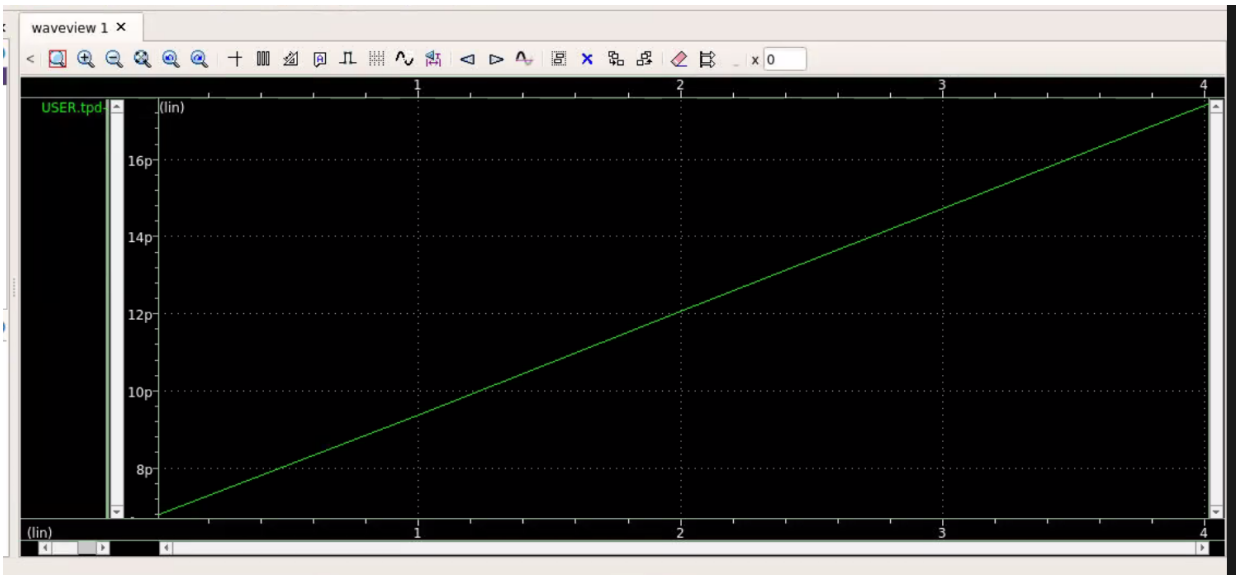
5) Normalized g & p
   g = 2.9/1.72 = 1.68
   p = 12.9/1.72 = 7.5

For The NOR2:

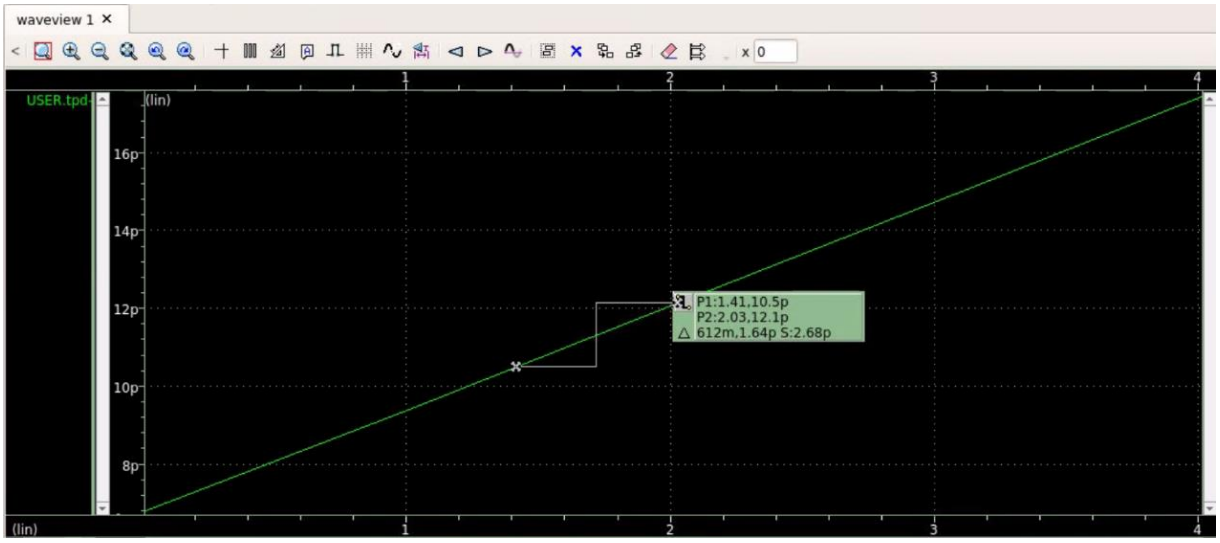
1) The Netlist:

```
* NOR2.sp
*-----------------------------------------------------------------------
* Parameters and models
*-----------------------------------------------------------------------
.param SUPPLY=1.05
.param H=4
.option scale=15n
.lib '/mnt/ext/synopsys/pdks/32nm/install/pdk/SAED32nm_PDK_04152022/hspice/saed32nm.lib'TT
.temp 70
.option post
*-----------------------------------------------------------------------
* Subcircuits
*-----------------------------------------------------------------------
.global vdd gnd
.subckt NOR a y N=7 P=14
*-----------------NMOS----------------------
xm0 y gnd gnd gnd n105 w='N' l=2
+ AS='N*5' PS='2*N+10' AD='N*5' PD='2*N+10'
xm1 y a gnd gnd n105 w='N' l=2
+ AS='N*5' PS='2*N+10' AD='N*5' PD='2*N+10'
*----------------PMOS----------------------
xm2 x a vdd vdd p105 w='2*P' l=2
+ AS='2*P*5' PS='2*2*P+10' AD='2*P*5' PD='2*2*P+10'
xm3 y gnd x vdd p105 w='2*P' l=2
+ AS='2*P*5' PS='2*2*P+10' AD='2*P*5' PD='2*2*P+10'
.ends
*-----------------------------------------------------------------------
* Simulation netlist
*-----------------------------------------------------------------------
Vdd vdd gnd 'SUPPLY'
Vin1 a gnd PULSE 0 'SUPPLY' 0ps 20ps 20ps 120ps 280ps
X1 a b NOR * shape input waveform
X2 b c NOR M='H' * reshape input waveform
X3 c d NOR M='H**2' * device under test
X4 d e NOR M='H**3' * load
X5 e f NOR M='H**4' * load on load
*-----------------------------------------------------------------------
* Stimulus
*-----------------------------------------------------------------------
.tran 0.1ps 280ps SWEEP H 0.01 4.01 1
.MEASURE TRAN tpdr TRIG  v(c)=0.5 FALL=1 TARG  v(d)=0.5 RISE=1
.MEASURE TRAN tpdf TRIG  v(c)=0.5 RISE=1 TARG  v(d)=0.5 FALL=1
.MEASURE TRAN trise TRIG  v(d)='0.2*1.0' RISE=1 TARG  v(d)='0.8*1.0' RISE=1
.MEASURE TRAN tfall TRIG  v(d)='0.8*1.0' FALL=1 TARG  v(d)='0.2*1.0' FALL=1
.MEASURE tpd PARAM '(tpdr+tpdf)/2'
.end
```

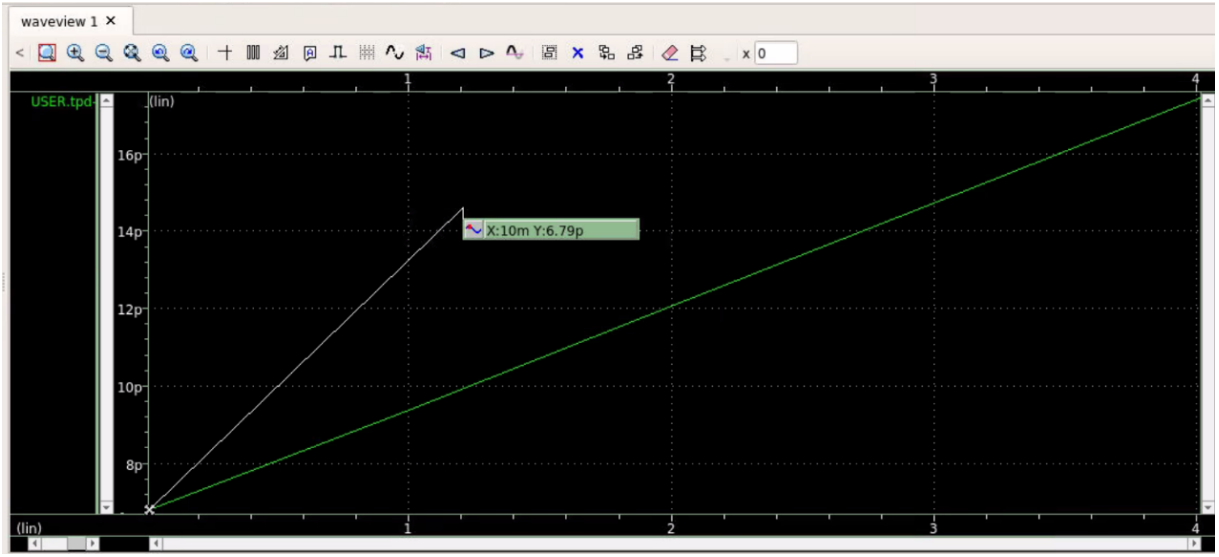
2) Delay VS h Plot



3) Getting g



4) Getting p



5) Normalization of g & p

g = 2.68/1.72 = 1.55

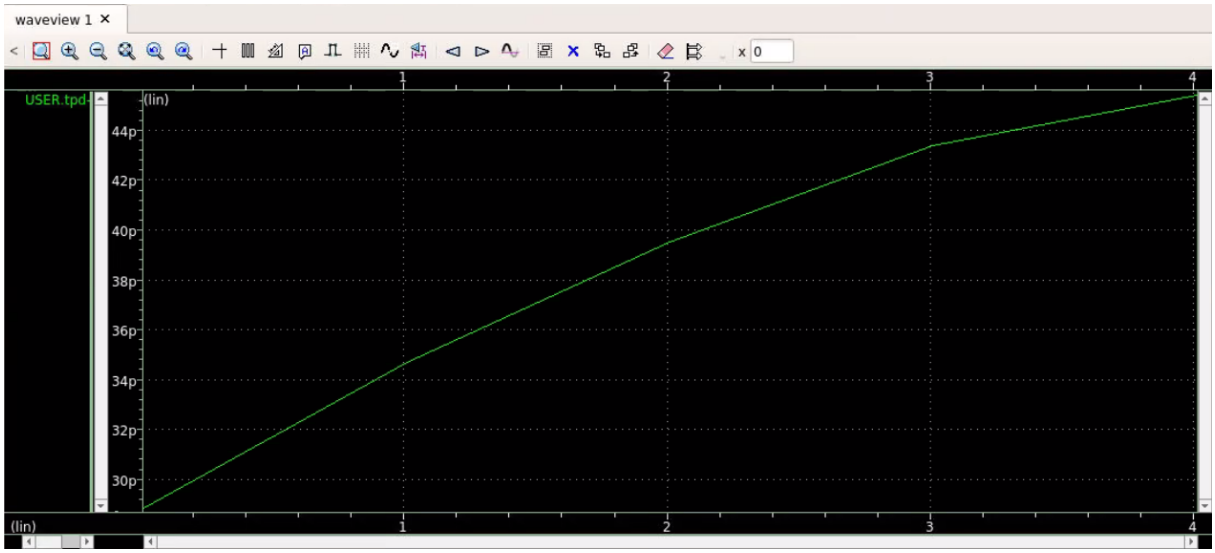
p = 6.84/1.72 = 3.97

For The NOR4:

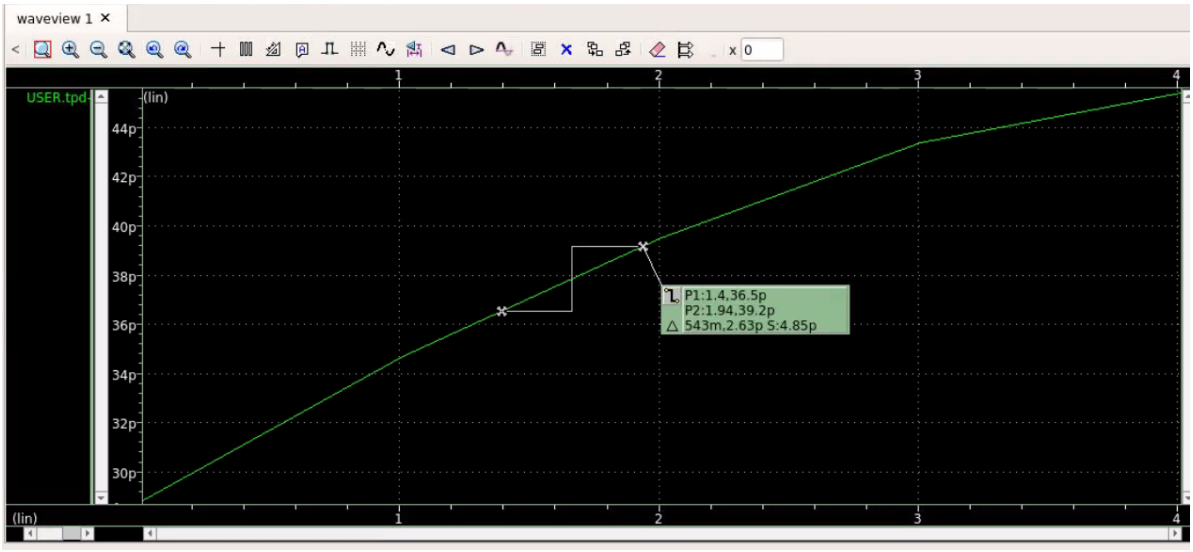
1) The Netlist:

```
* NOR4.sp
*-----------------------------------------------------------------------
* Parameters and models
*-----------------------------------------------------------------------
.param SUPPLY=1.05
.param H=4
.option scale=15n
.lib '/mnt/ext/synopsys/pdks/32nm/install/pdk/SAED32nm_PDK_04152022/hspice/saed32nm.lib'TT
.temp 70
.option post
*-----------------------------------------------------------------------
* Subcircuits
*-----------------------------------------------------------------------
.global vdd gnd
.subckt NOR a y N=7 P=14
----------------NMOS-----------------
xm0 y a gnd gnd n105 w='N' l=2
+ AS='N*5' PS='2*N+10' AD='N*5' PD='2*N+10'
xm1 y gnd gnd gnd n105 w='N' l=2
+ AS='N*5' PS='2*N+10' AD='N*5' PD='2*N+10'
xm2 y gnd gnd gnd n105 w='N' l=2
+ AS='N*5' PS='2*N+10' AD='N*5' PD='2*N+10'
xm3 y gnd gnd gnd n105 w='N' l=2
+ AS='N*5' PS='2*N+10' AD='N*5' PD='2*N+10'
----------------PMOS-----------------
xm4 r a vdd vdd p105 w='8*P' l=2
+ AS='8*P*5' PS='2*8*P+10' AD='8*P*5' PD='2*8*P+10'
xm5 z gnd r vdd p105 w='8*P' l=2
+ AS='8*P*5' PS='2*8*P+10' AD='8*P*5' PD='2*8*P+10'
xm6 x gnd z vdd p105 w='8*P' l=2
+ AS='8*P*5' PS='2*8*P+10' AD='8*P*5' PD='2*8*P+10'
xm7 y gnd x vdd p105 w='8*P' l=2
+ AS='8*P*5' PS='2*8*P+10' AD='8*P*5' PD='2*8*P+10'
.ends
*-----------------------------------------------------------------------
* Simulation netlist
*-----------------------------------------------------------------------
Vdd vdd gnd 'SUPPLY'
Vin1 a gnd PULSE 0 'SUPPLY' 0ps 20ps 20ps 120ps 280ps
X1 a b NOR * shape input waveform
X2 b c NOR M='H' * reshape input waveform
X3 c d NOR M='H**2' * device under test
X4 d e NOR M='H**3' * load
X5 e f NOR M='H**4' * load on load
*-----------------------------------------------------------------------
* Stimulus
*-----------------------------------------------------------------------
.tran 0.1ps 280ps SWEEP H 0.01 4.01 1
.MEASURE TRAN tpdr TRIG  v(c)=0.5 FALL=1 TARG  v(d)=0.5 RISE=1
.MEASURE TRAN tpdf TRIG  v(c)=0.5 RISE=1 TARG  v(d)=0.5 FALL=1
.MEASURE TRAN trise TRIG  v(d)='0.2*1.0' RISE=1 TARG  v(d)='0.8*1.0' RISE=1
.MEASURE TRAN tfall TRIG  v(d)='0.8*1.0' FALL=1 TARG  v(d)='0.2*1.0' FALL=1
.MEASURE tpd PARAM '(tpdr+tpdf)/2'
.end
```

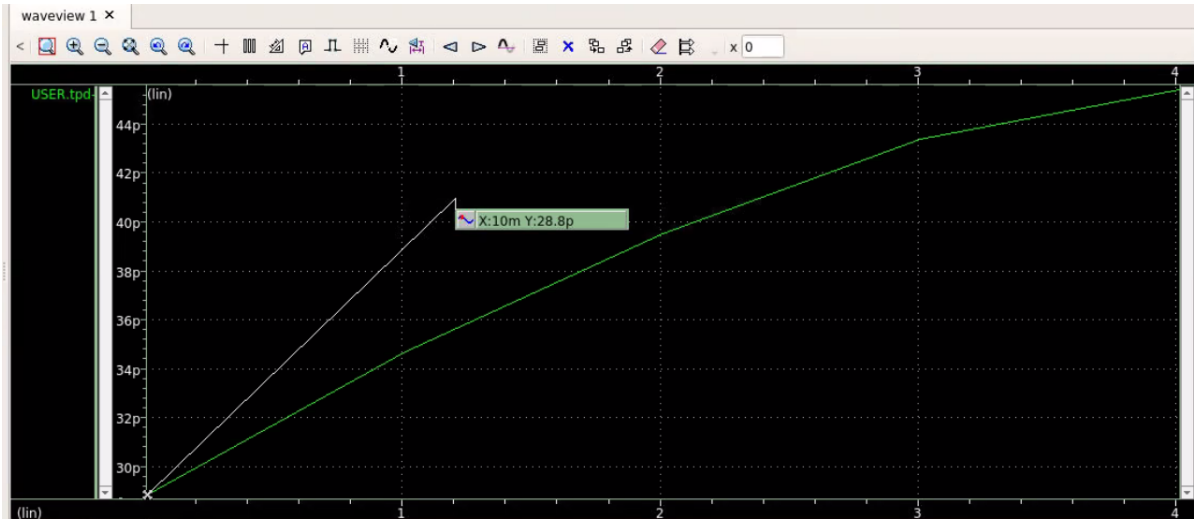
2) Delay (tpd) VS h



3) Getting g



4) Getting p



5) Normalized g & p
g = 4.85/1.72 = 2.8
p = 28.8/1.72 = 16.7

[2] & [3] Comparison Between g & p

Gate	Logical effort(g)	Parasitic delay(p)
inv	1	1.54
Nand2	1.18	2.97
Nand4	1.68	7.5
Nor2	1.55	3.97
Nor4	2.8	16.7

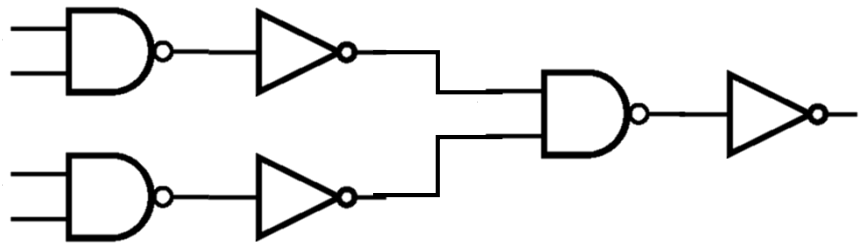
It can clearly be noticed that NOR gates, which have large PMOS chains in series have the largest logical effort & parasitic delay.

[4] Compare the design alternatives in a table calculating N, G, P, fopt, D for each alternative.

	A	B	C	D	E	F	G	H
1	Design	N	G	P	BH	F=GBH	fopt=F^(1/N)	D = P + N*fopt
2	NOR4	1	3	4	76.8	230.4	230.4	234.4
3	NAND4-INV	2	2	5	76.8	153.6	12.39354671	29.78709342
4	NAND2-NOR2	2	2.222222	4	76.8	170.6667	13.06394529	30.12789059
5	INV-NAND4-INV	3	2	6	76.8	153.6	5.355463601	22.0663908
6	NAND4-INV-INV-INV	4	2	7	76.8	153.6	3.520446947	21.08178779
7	NAND2-NOR2-INV-INV	4	2.222222	6	76.8	170.6667	3.614408014	20.45763206
8	NAND2-INV-NAND2-INV	4	1.777778	6	76.8	136.5333	3.418296051	19.6731842
9	INV-NAND2-INV-NAND2-INV	5	1.777778	7	76.8	136.5333	2.673300248	20.36650124
10	NAND2-INV-NAND2-INV-INV-INV	6	1.777778	8	76.8	136.5333	2.26920178	21.61521068

Accordingly, the highlighted design (design 8) is the best decoder choice as it has the least delay a.k.a. The most speedy design.

[5] In order to size the gates correctly, we have to look at the circuit schematic that makes the decoded word as shown below:



To start sizing each gate, we have to get the load cap & cin so as to get H thus going backwards & sizing every gate. Given: Every word consists of 32 bits & every bit presents a load of 3 unit-sized transistors. Then: Cload = 32 * 3 = 96 fF. Also given, each input may drive 10 unit-sized transistors. H = Cload/Cin = 9.6 , B = 8 = 2* 2*2, G=(4/3)*1*(4/3)*1= 1.78. Now get F = GBH = 136.7. *fopt*= $F^{1/4}$ = 3.419

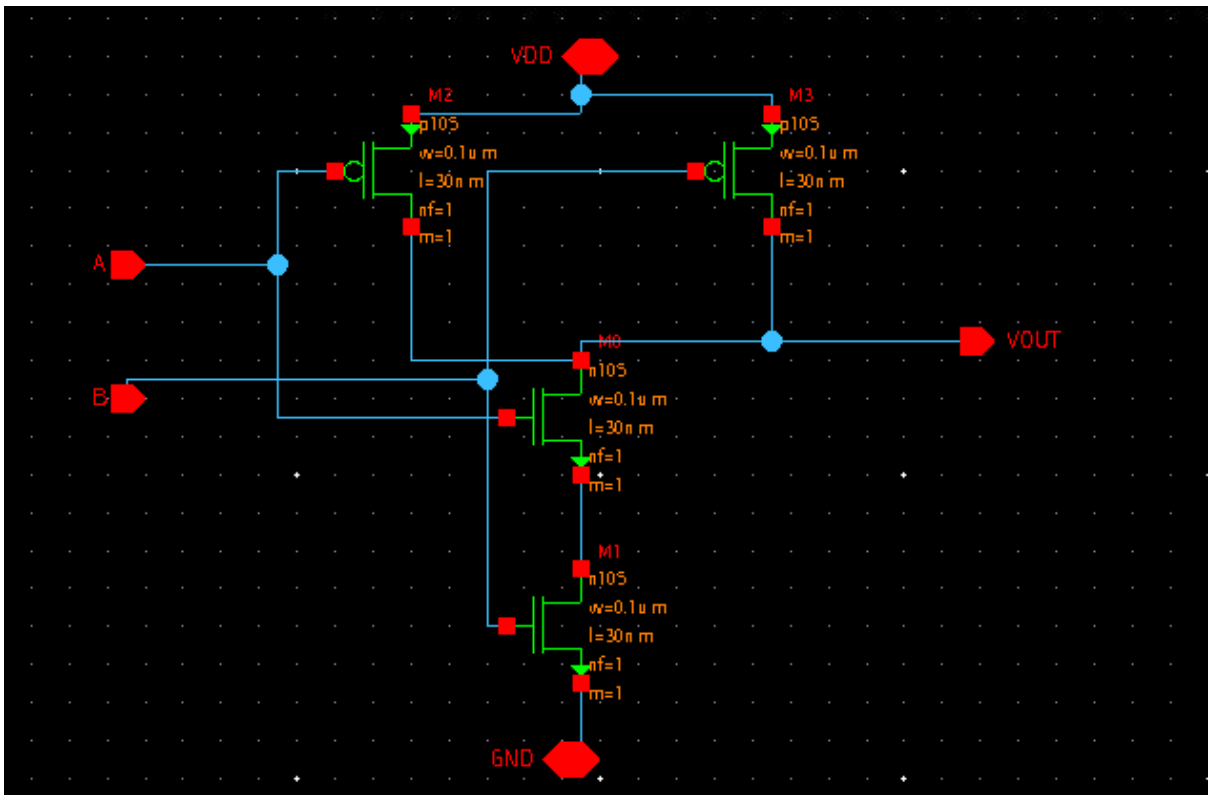
Now Cin of 4th stage inverter = (1*96)/3.419 = 28 approx. = 30 (To get a whole number). Now that's Cin for the 4th stage & cout for the 3rd. We go similarly for the rest. So Cin for 3rd stage = 12, for 2nd = 3 & for 1st = 1.5.

Now To get the transistor sizes we look into the input of every gate: For the inverter we have 1 pmos of 2k & 1 nmos of 1k then 2k+1k = 3k = Cin = 30. Then k = 10. As for NAND gates they have 2 parallel pmos then each will be 2k & 2 series Nmos so each for 2k as well so every input will look at 4k, then 4k = Cin(nand 3rd stage) = 12 then k =3 and so on.

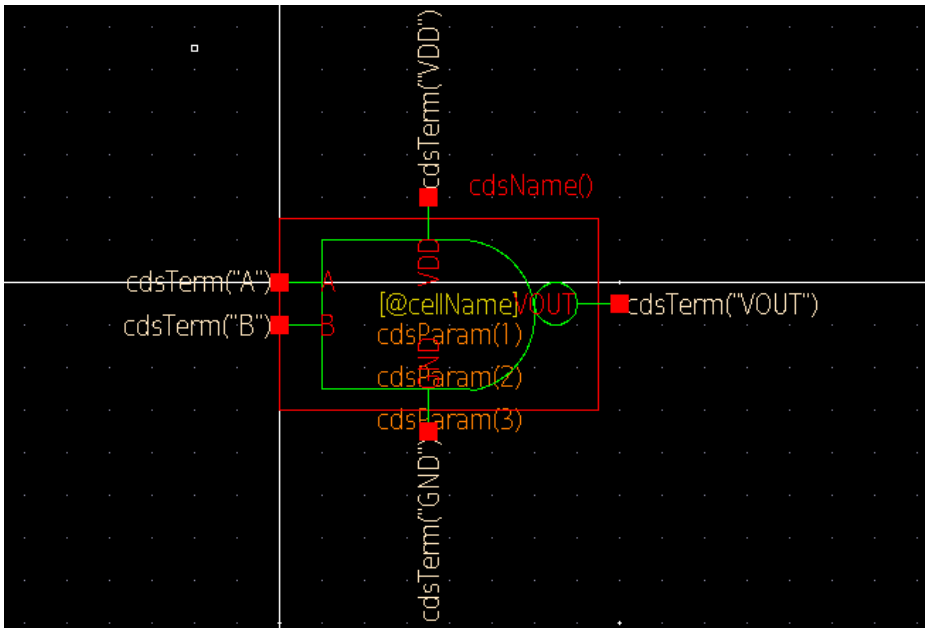
The results for every stage showed the sizes that will be shown in every screenshot to come.

[6] Schematics of each stage (gate) showing sizing of transistors.

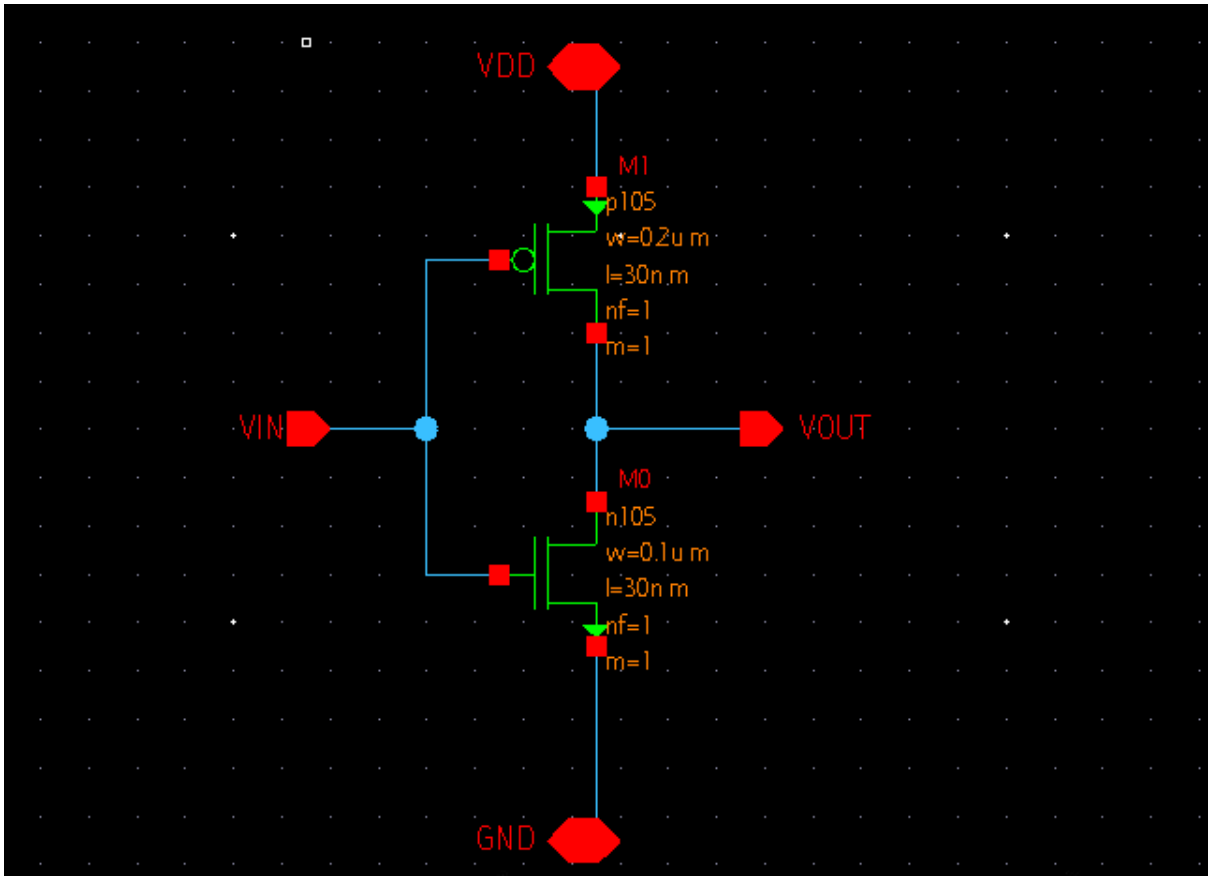
The 1st stage NAND gates schematic & sizing: All transistor widths are 0.1u m



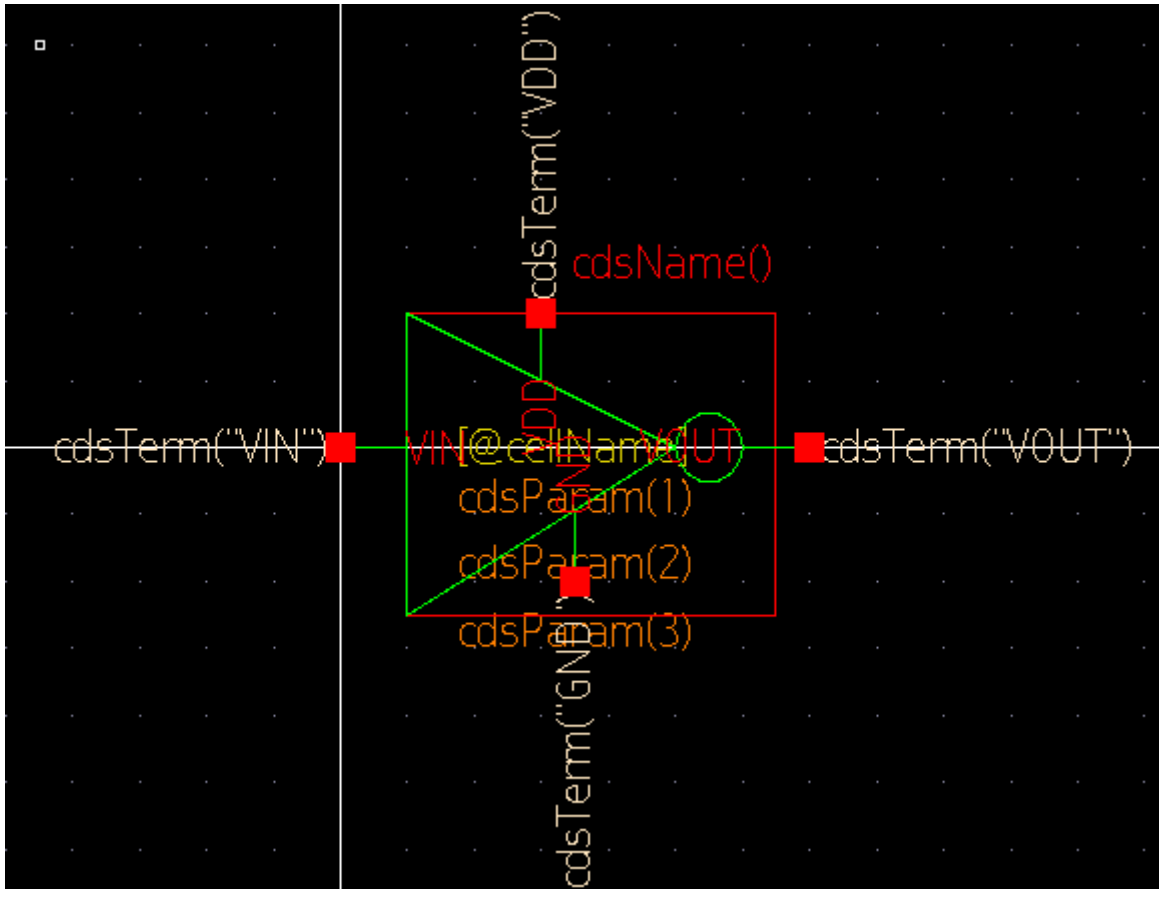
The NAND gate symbol:



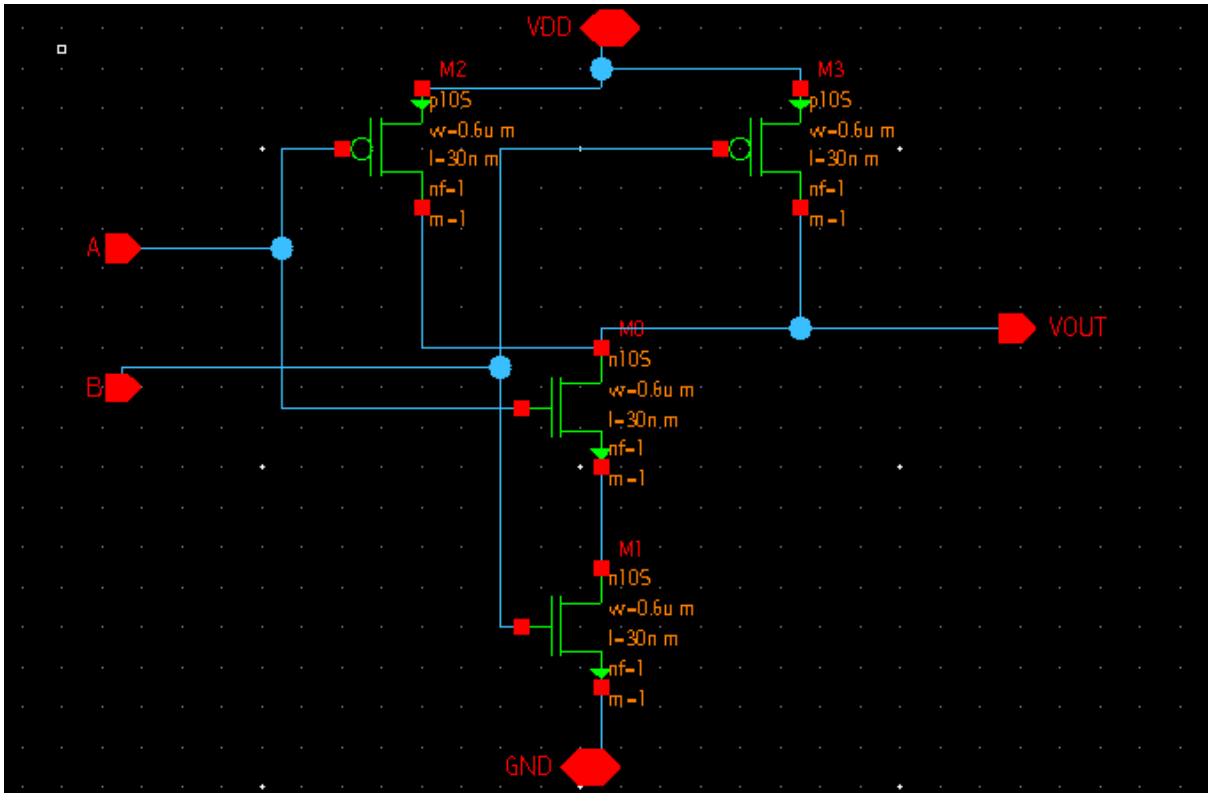
The 2nd Stage: Inverter Schematic & Sizing:



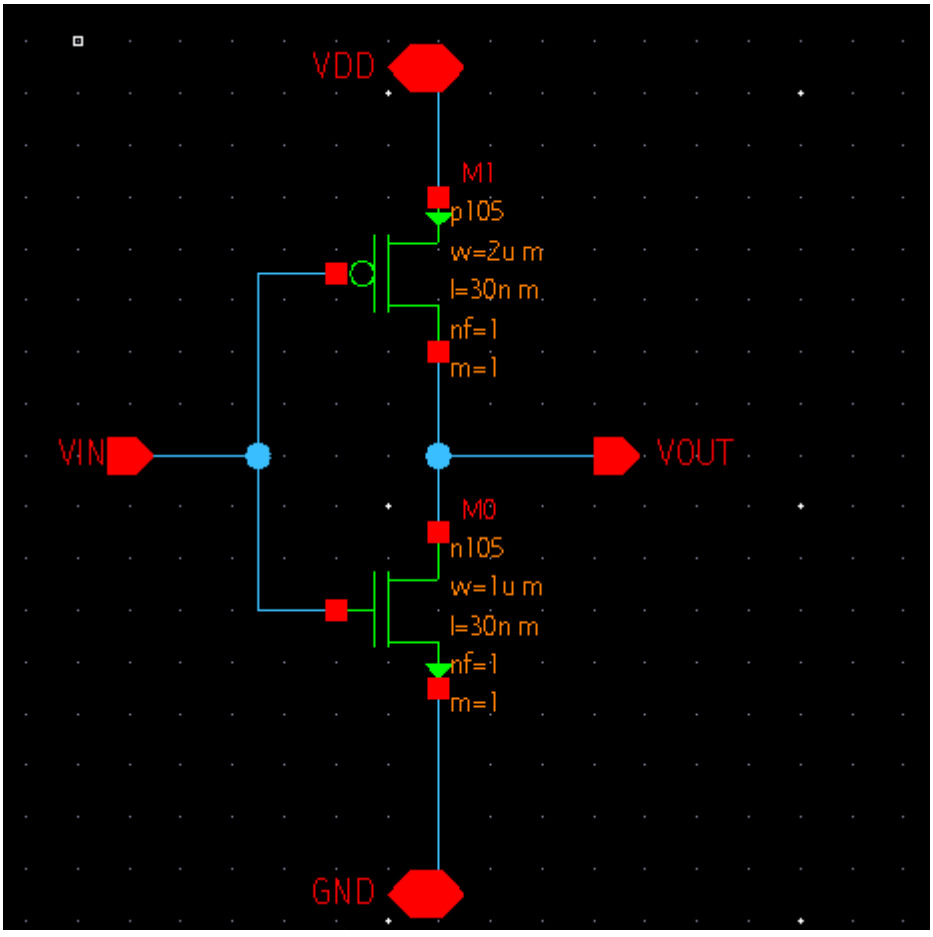
The Inverter Symbol (Also Used for FO4 INV)



The 3rd Stage: NAND2 Schematic & Sizing:



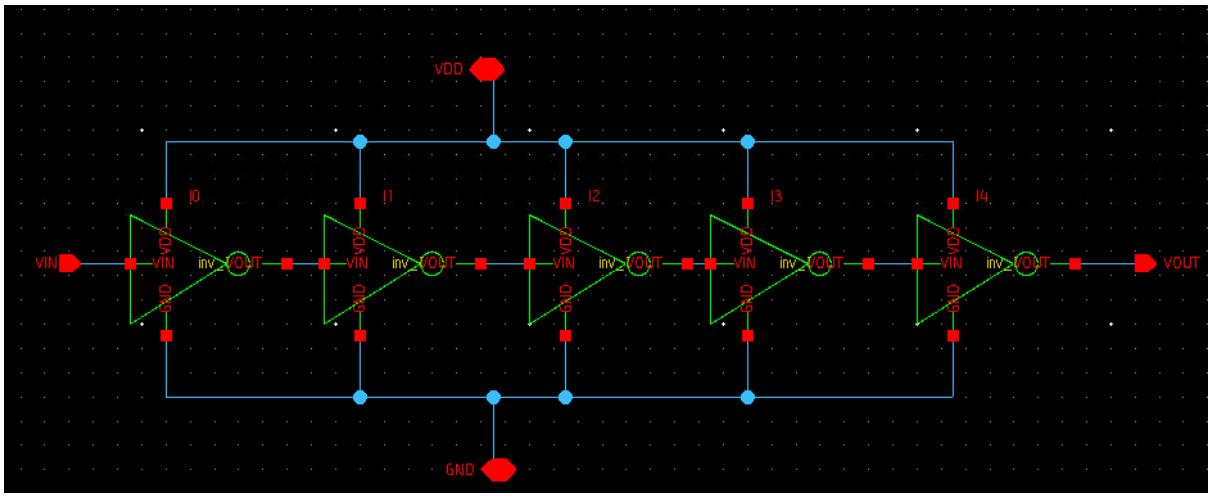
The 4th Stage: Inverter Schematic & Sizing:



Note: In order to create a symbol for a gate: Open its schematic then click Tools -> New Cell View -> From Cell View.

Note: In order to change the parameters of a transistor or a component press "Q" on your keyboard.

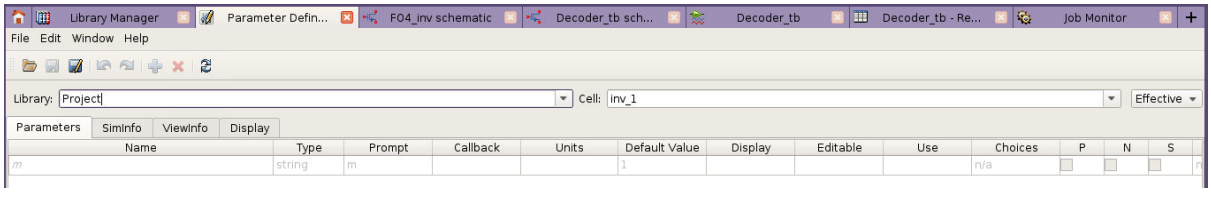
Now In order to shape & drive the decoder's inputs & outputs you'll need a FO4 inverter chain. So you'll add a schematic view for the following FO4 chain of inverters.



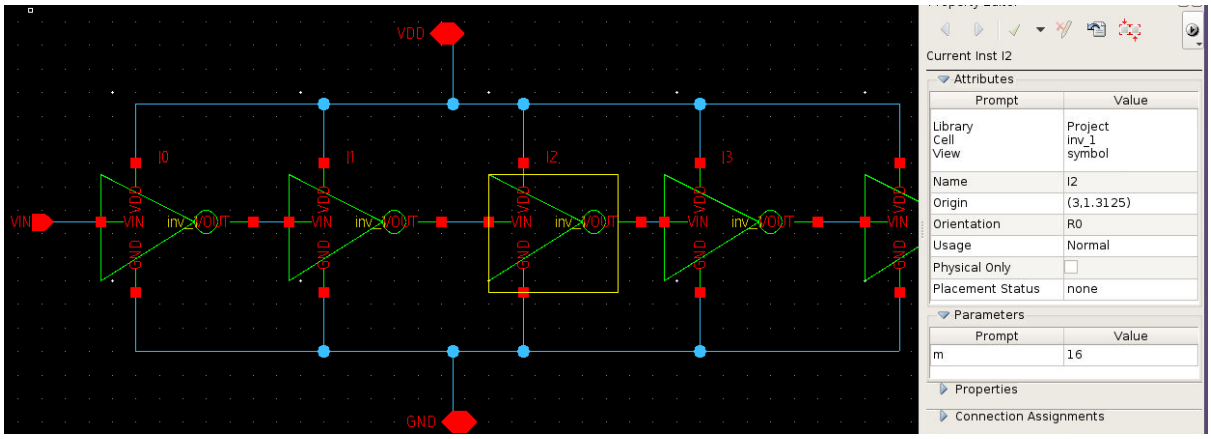
We then give this chain a symbol (It looks exactly like an inv symbol) as it will act as one.

Now we need to define a parameter for this FO4 cell so that it takes the values $4^{stage\ number}$ e.g. for stage 0 it'll be $4^0 = 1$ etc….

The Inverter used in this FO4 cell is the inv with size (0.2u & 0.1um) a.k.a inv1. So we go to the library manager, right click on inv1 -> edit parameter definitions -> change effective to base -> click the + sign & write your parameter. Give it a value as shown below:



Now return to the F04 schematic. Press Q & start giving parameter m its values as shown:



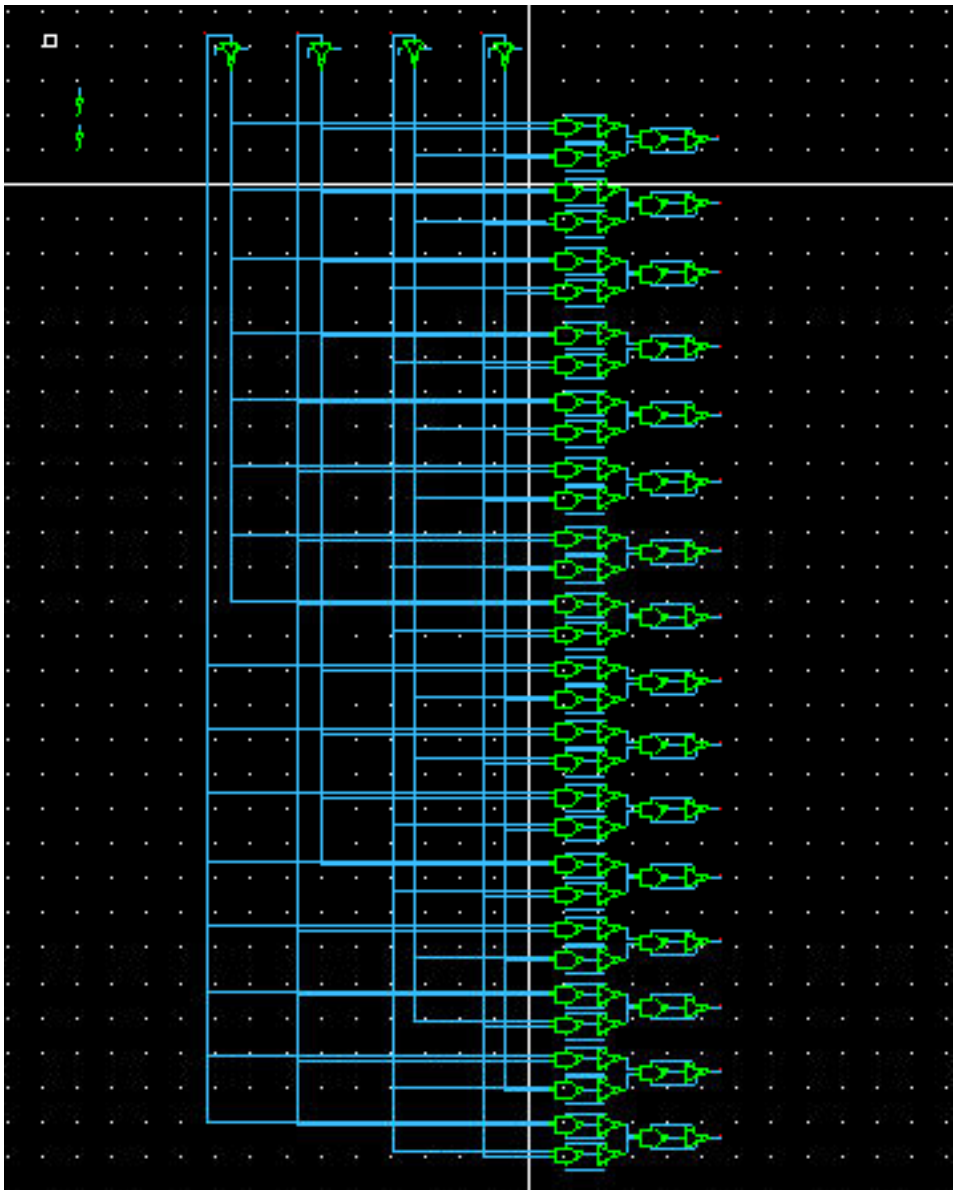
To Start Implementing your 4:16 decoder schematic you have to know its truth table (To be able to route) & to know how it should look like.

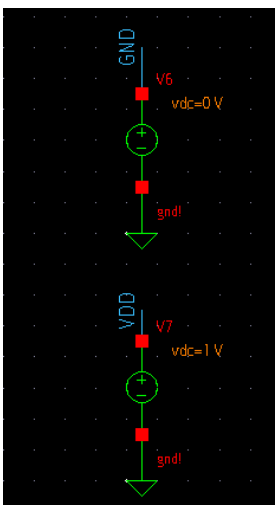
INPUTS				OUTPUTS														
A_3	A_2	A_1	A_0	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

We're not looking at the outputs now we're just looking at the inputs to be able to route them. So for example for the 1st word we

have the 4 inputs = 0 & so on. We should get the following result:

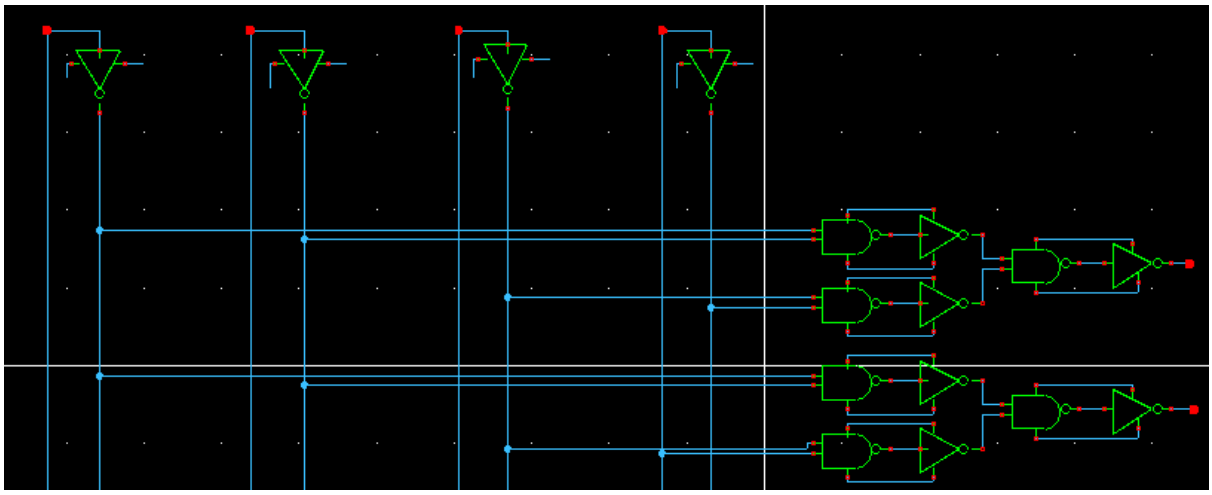
By implementing this on Custom Compiler, the decoder schematic should look like this:



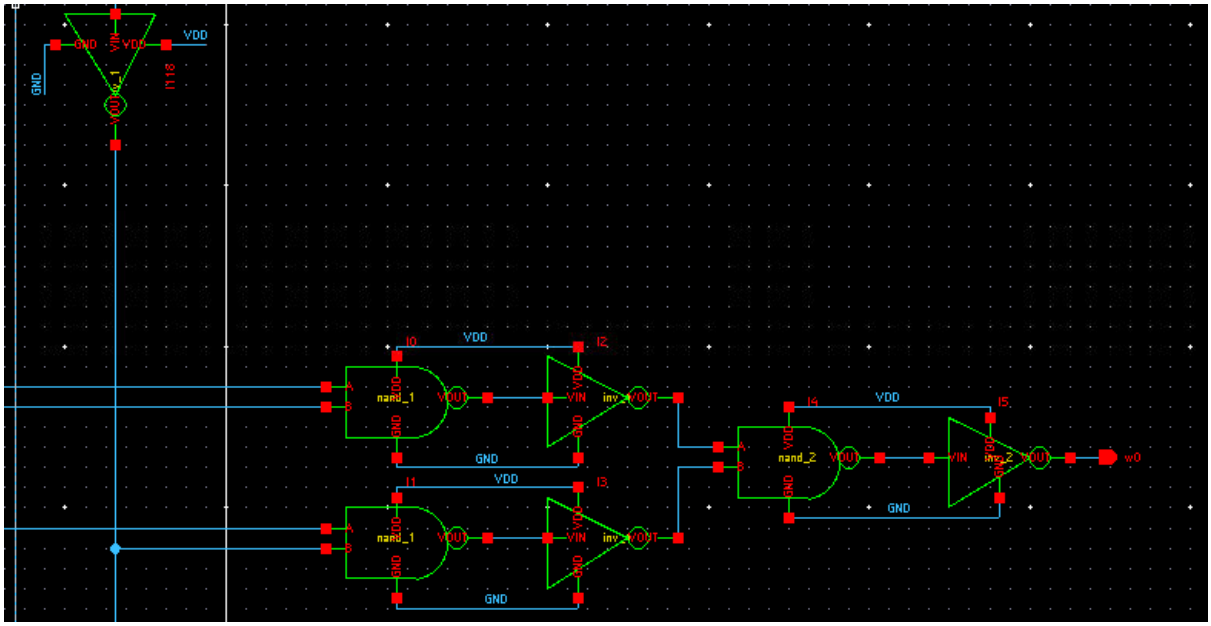


Here are the supply voltages that supply all of the decoder gates with VDD & GND. They're connected to them by Labels

A closer view would be:

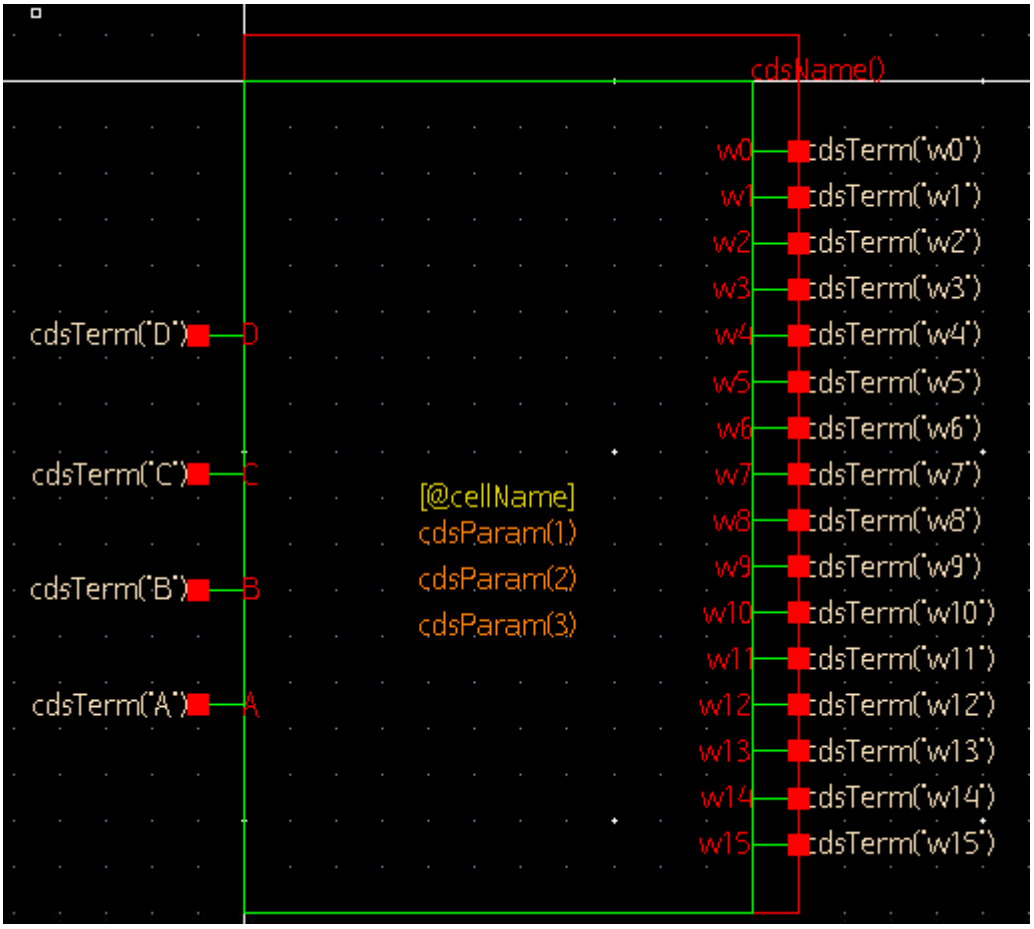


And a closer one would be:



Note: you can put your source a bit far (for a cleaner look) & use a label (shortcut “L”) to connect it to all the VDDs & GNDs in your schematic.

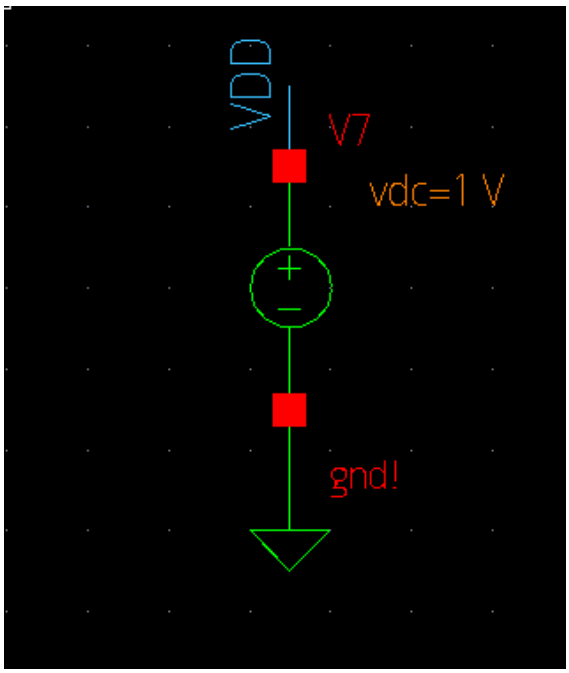
Creating a Symbol for your decoder is necessary as it’ll be used in the testbench. It shall look like this:

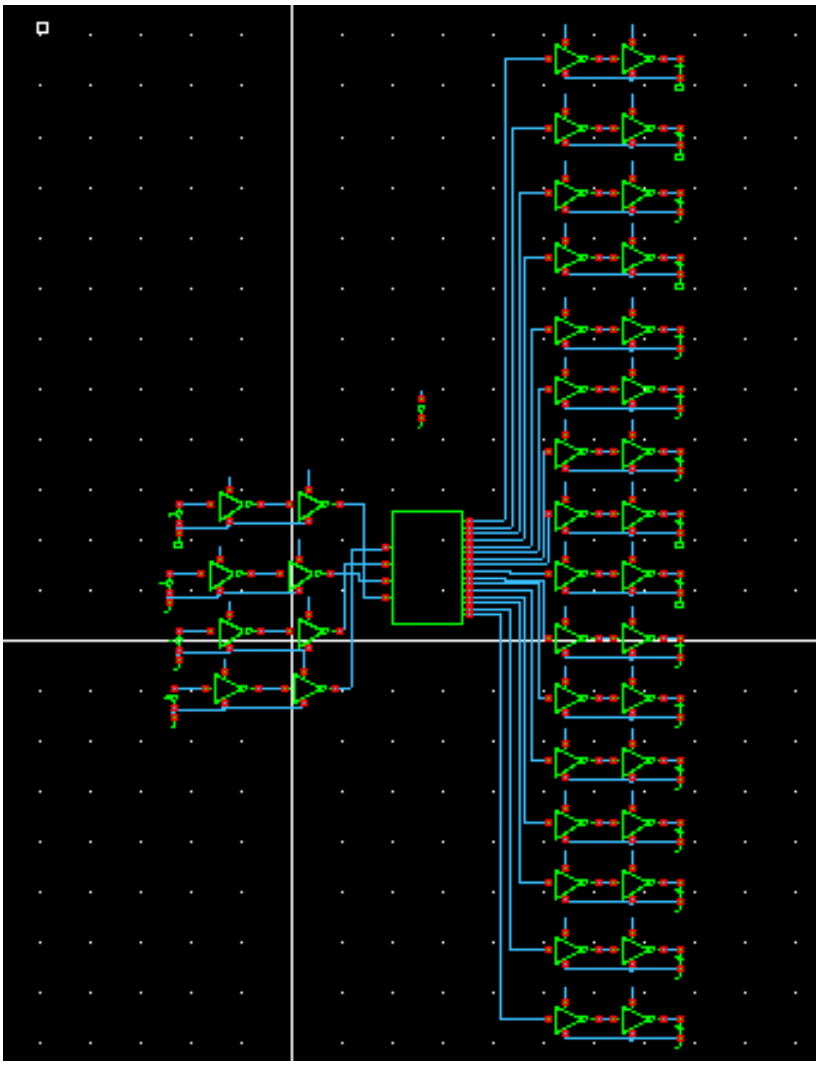


Your Decoder is Ready to be used!

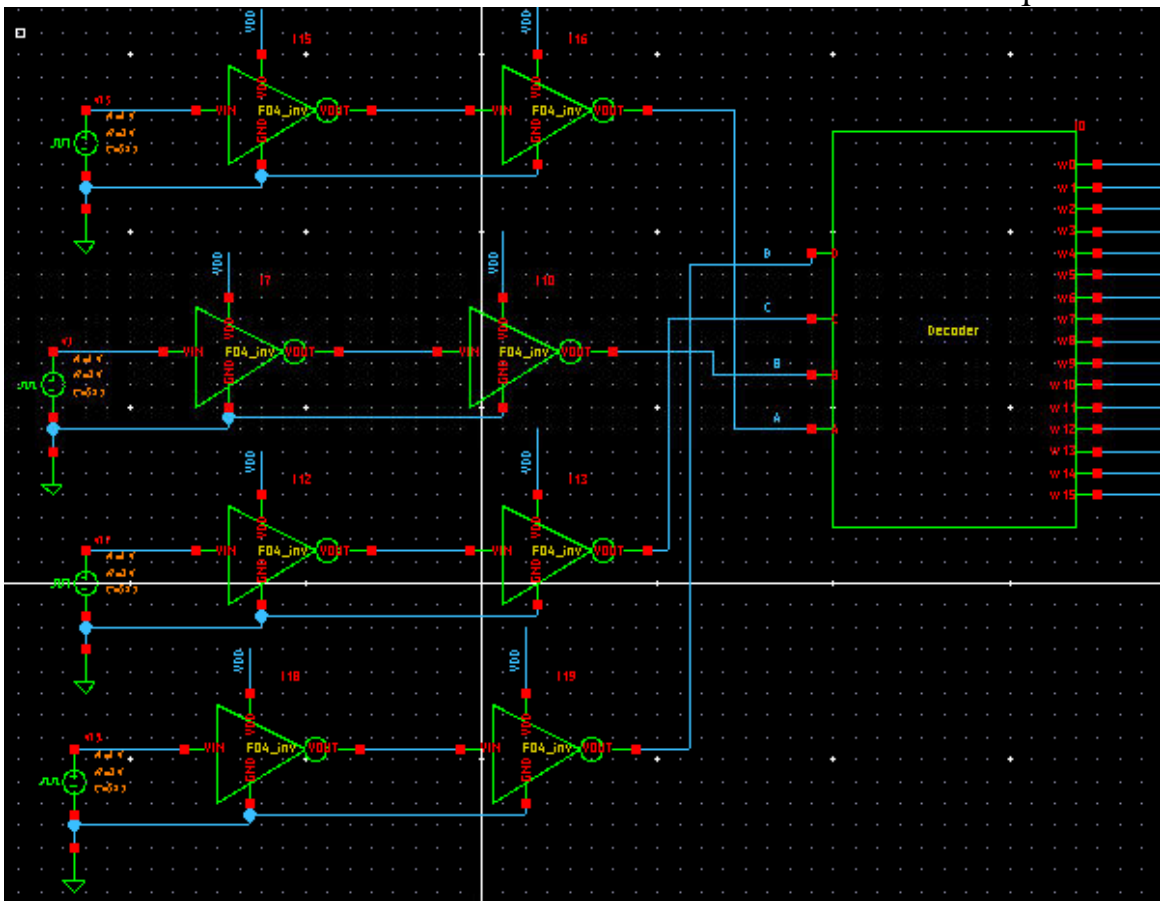
Creating the Testbench……

Open a new cell view in your library & call it Decoder_tb. Now you can use your FO4 symbol to drive the inputs & the loads & you can connect your decoder circuit as follows: with a DC Source vdc

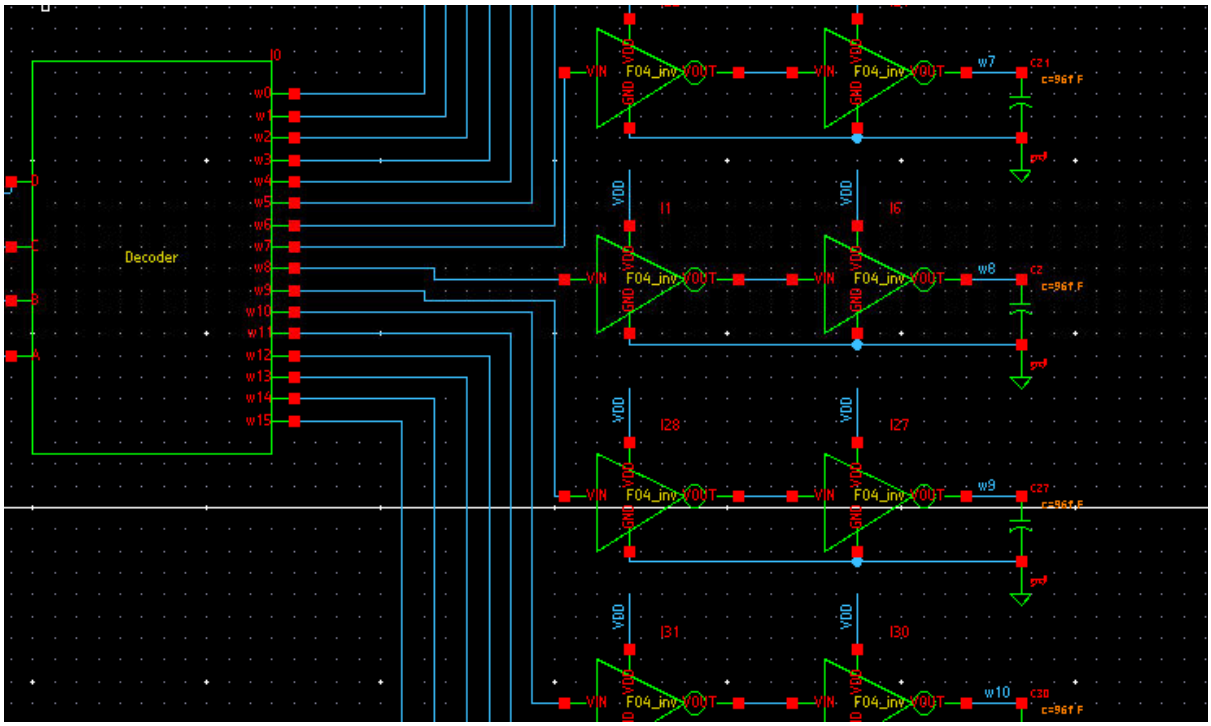




The Decoder Testbench Schematic. For a closer look at its inputs:



Notice the inverters used (FO4 inv). For a closer look at the outputs:

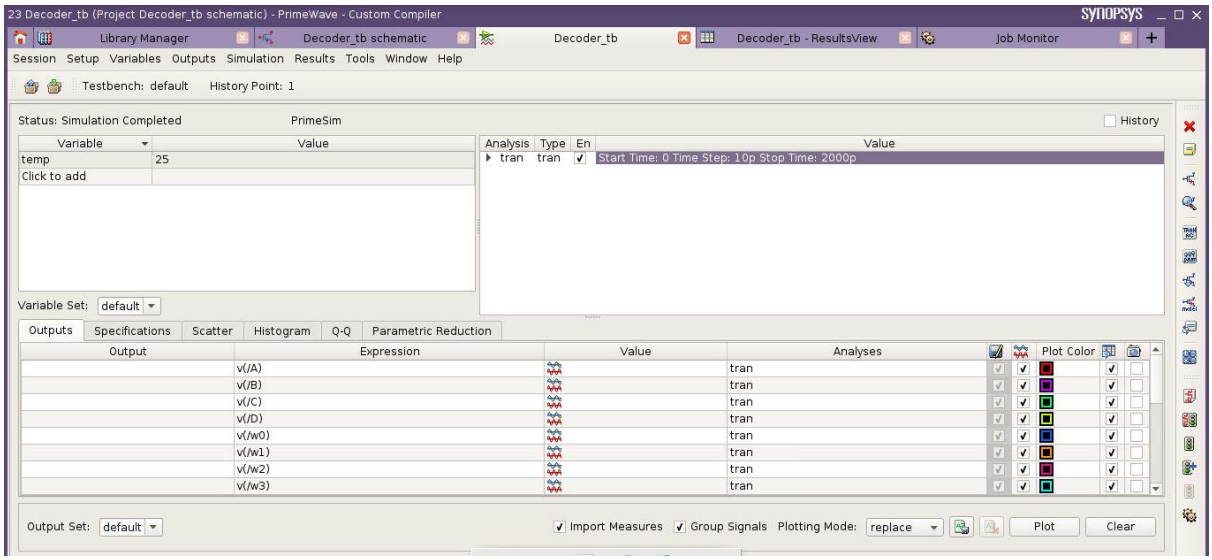


Notice how the words are driven. Also notice that pur loads, thus our outputs, are taken near the capacitors not directly at the out of the decoder. Finally, look at the capacitive loads. They're set to 96 fF.

Now to run the transient simulation for this testbench you open the tb schematic & go to TOOLS -> Primewave. Primewave will open. You then need to go to setup -> Model Files & you choose the path to SAED32 PDK & in the next space you write "TT" (Typical Typical).

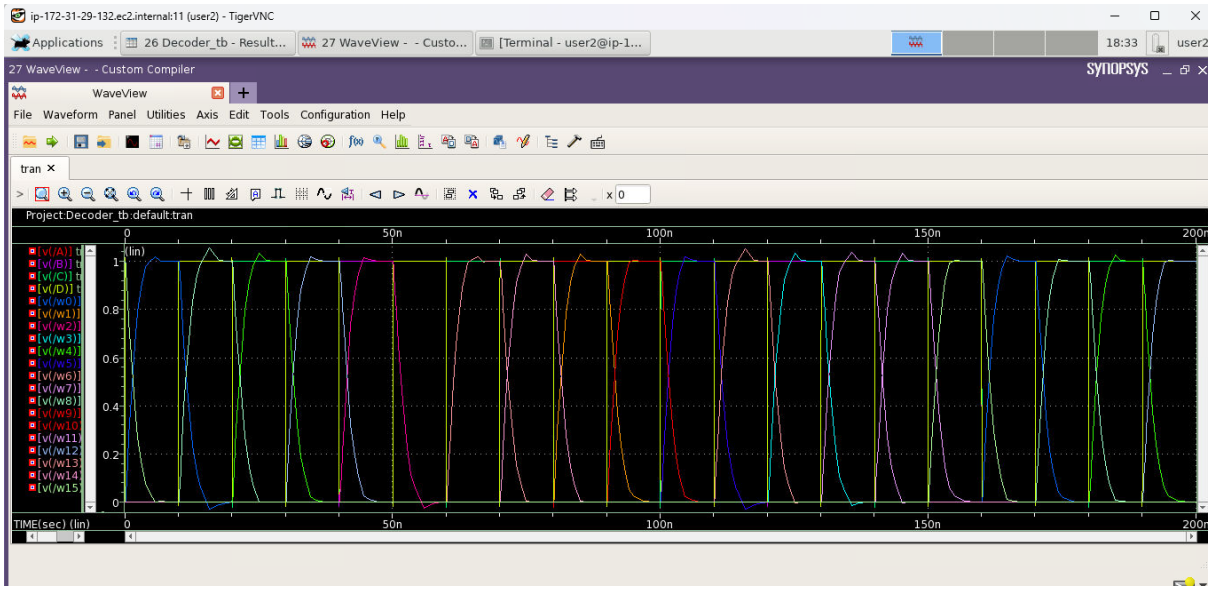
The go to simulation -> Options & choose Primesim Hspice. Now you are ready to add your analysis type. Right click on the analysis window & choose Edit. Set your transient analysis choices. We set it for the decoder as shown in the figure below.

Now go down to expressions & double click -> choose from schematic. Select the signals you want to see on your analysis. Finally, click Netlist & Run.

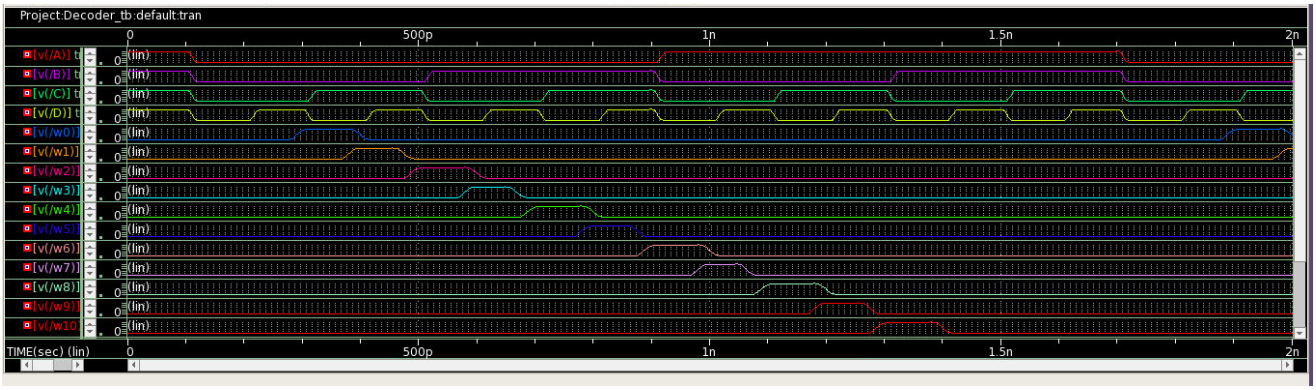


Primewave window with our chosen values.

The output waveform should look like this at first:

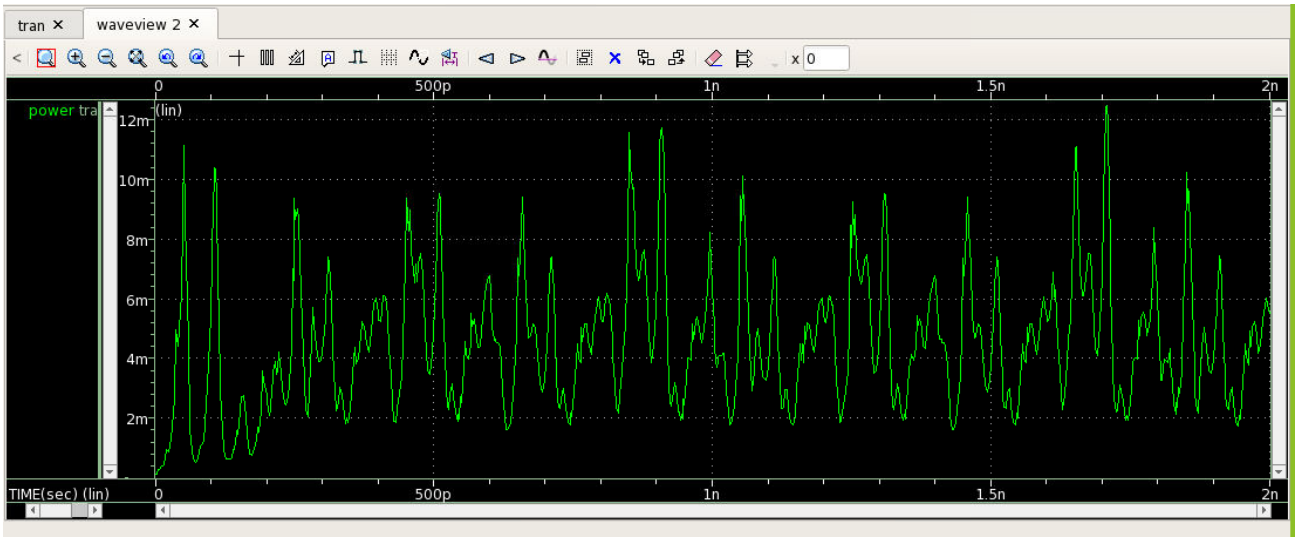


You can then select the signals & ungroup them making them look like this:



In order to get the power plot: In primewave we go to Outputs -> save options -> choose “save: all” & tick on “save all power” -> ok.

Now go to your signals waveform -> choose the third icon from the right under help to get your file -> choose your file “toplevel” -> in the signals below, right click on power -> plot waveform to -> new waveview.



To get the average power click on the “Measurement Tool” -> Level -> Average.

[15] Estimate the area of the design. Just consider the area of the transistors for simplicity: $\sum W * (2 * LD + L)$.

Given are: W = Wmin =100nm and L= Lmin = 30nm. Lambda = 0.5* Lmin. = 15nm. So LD = 5*15nm = 75nm.

To calculate this we’ll need to calc. the area of every gate alone then we’ll add them and multiply by 16 (for 16 words) finally we’ll add the result to the area of 4 of inv_1 (the 4 inverters at the inputs).

- NAND2 Stage One Area:

PMOS Area = 2 $[(0.1*10^{-6})(2*75*10^{-9} + 30*10^{-9})]$= 0.000036 nm

NMOS Area = 2 $[(0.1*10^{-6})(2*75*10^{-9} + 30*10^{-9})]$= 0.000036 nm

Since we have 2 NAND2 gates of the same size then their area = 2 *[0.000036 nm + 0.000036 nm] = 0.000144 nm

- INV1 Stage 2 Area :

PMOS Area = $[(0.2*10^{-6})(2*75*10^{-9} + 30*10^{-9})]$ = 0.000006 nm

NMOS Area = $[(0.1*10^{-6})(2*75*10^{-9} + 30*10^{-9})]$ = 0.000018 nm

Total INV1 Area = 0.000006 nm + 0.000018 nm = 0.000024 nm

- NAND2 Stage 3 Area:

PMOS Area = 2 $[(0.6*10^{-6})(2*75*10^{-9} + 30*10^{-9})]$= 0.000216 nm

NMOS Area = 2 $[(0.6*10^{-6})(2*75*10^{-9} + 30*10^{-9})]$= 0.000216 nm

Total NAND2 Area = 0.000216 nm + 0.000216 nm = 0.000432 nm

- INV2 Stage 4 Area:

PMOS Area = $[(2*10^{-6})(2*75*10^{-9} + 30*10^{-9})]$ = 0.00036 nm

NMOS Area = $[(1*10^{-6})(2*75*10^{-9} + 30*10^{-9})]$ = 0.00018 nm

Total INV2 Area = 0.00036 nm + 0.00018 nm = 0.00054 nm

Total Area For One Word = 0.000144 nm + 0.000024 nm + 0.000432 nm + 0.00054 nm = 0.00114 nm

Total Area For 16 Words = 16 * 0.00114 nm = 0.01824 nm

Adding 4 Inverters at the Inputs:

Total Design Area = [4 * 0.000024 nm] + 0.01824 nm = 0.018336 nm2

Appendix

Before Starting Your Design it is important to create a directory & give it a name then find the path for the SAED32 nm pdk files. copy the SOURCEME & lib.def files and paste them in your new directory. These files should include these lines:

- Lib.defs File:

```
INCLUDE $SAED32_28_PDK/sym_libs/lib.defs

DEFINE SAED_PDK_32_28 $SAED32_28_PDK/SAED_PDK_32_28

ASSIGN SAED_PDK_32_28 libMode shared

ASSIGN SAED_PDK_32_28 PDKLib true

DEFINE reference $SAED32_28_PDK//reference

DEFINE test_32 $SAED32_28_PDK//test_32

DEFINE res_test $SAED32_28_PDK//res_test

DEFINE mylib ./mylib

DEFINE schematicsgate ./schematicsgate

DEFINE invfo4 ./invfo4
```

- Sourceme File:

```
export
SAED32_28_PDK=/remote/SCRATCH_fs01/edbab/SAED32_PDK_dev/release/rel11052016/SAED_PDK32nm
```