Information
Technology
Institute

9 Month Program

Digital IC Design Track

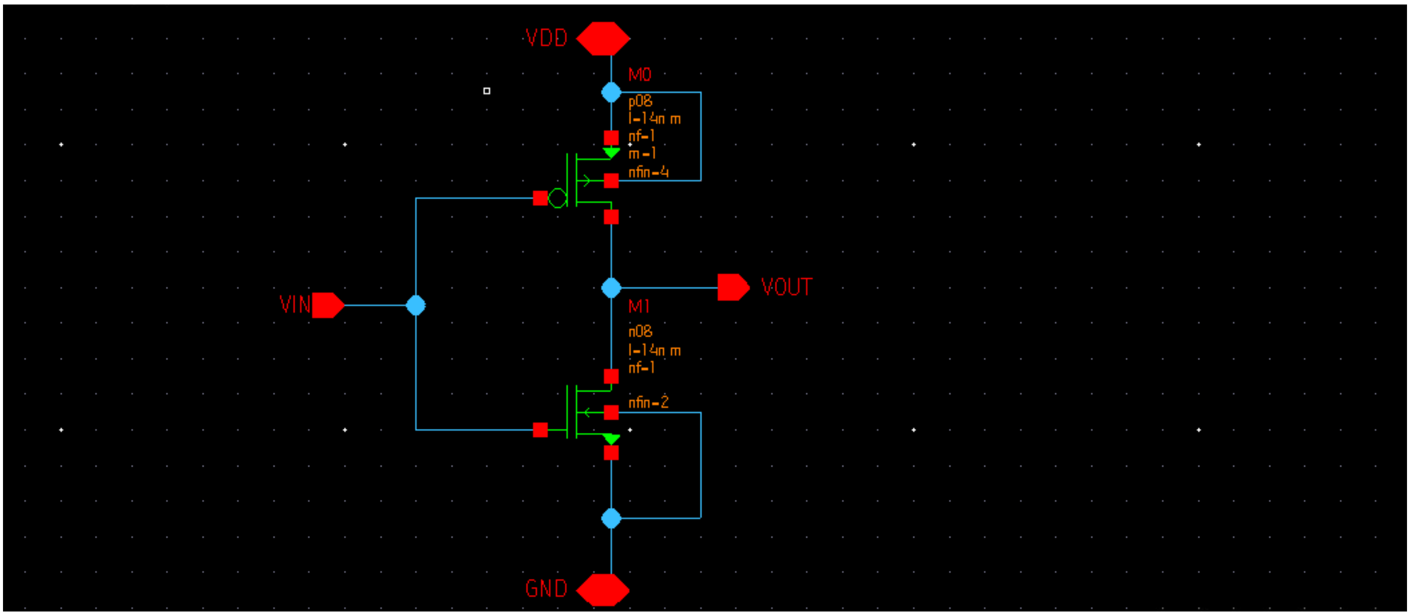
Project (2)

“Flip-Flop Design and Characterization”

Instructor: Dr Hesham Omran

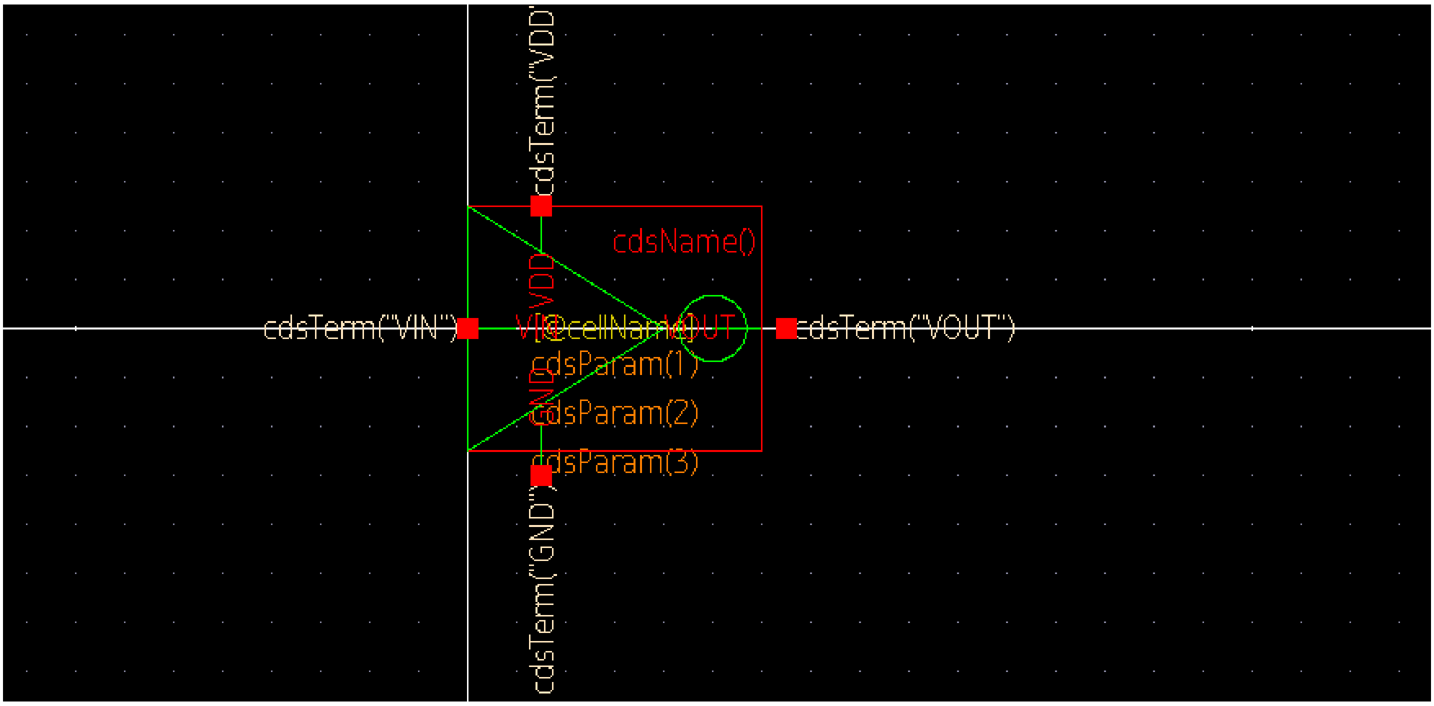
Part One: Flip-Flop Component Schematics:

Inverter Schematic:

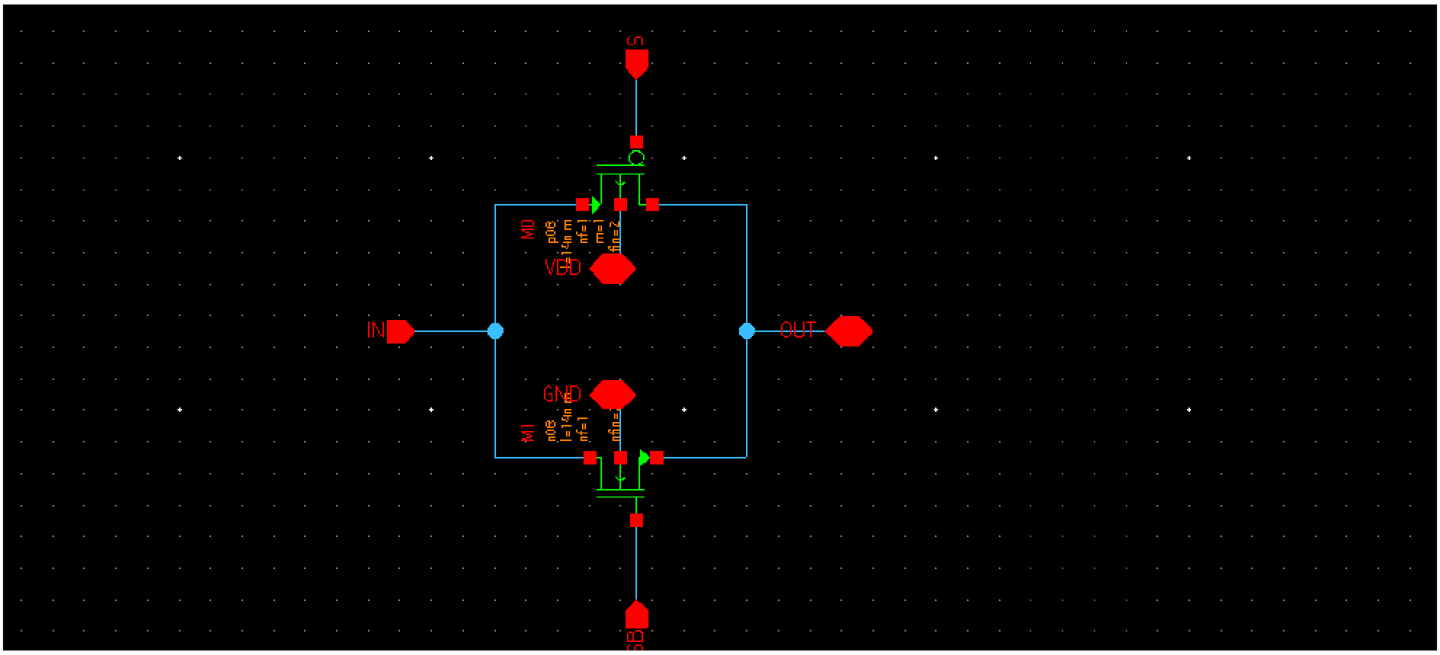


By cpressing Q: we set nfin of pfet to 4 & nfet to2.

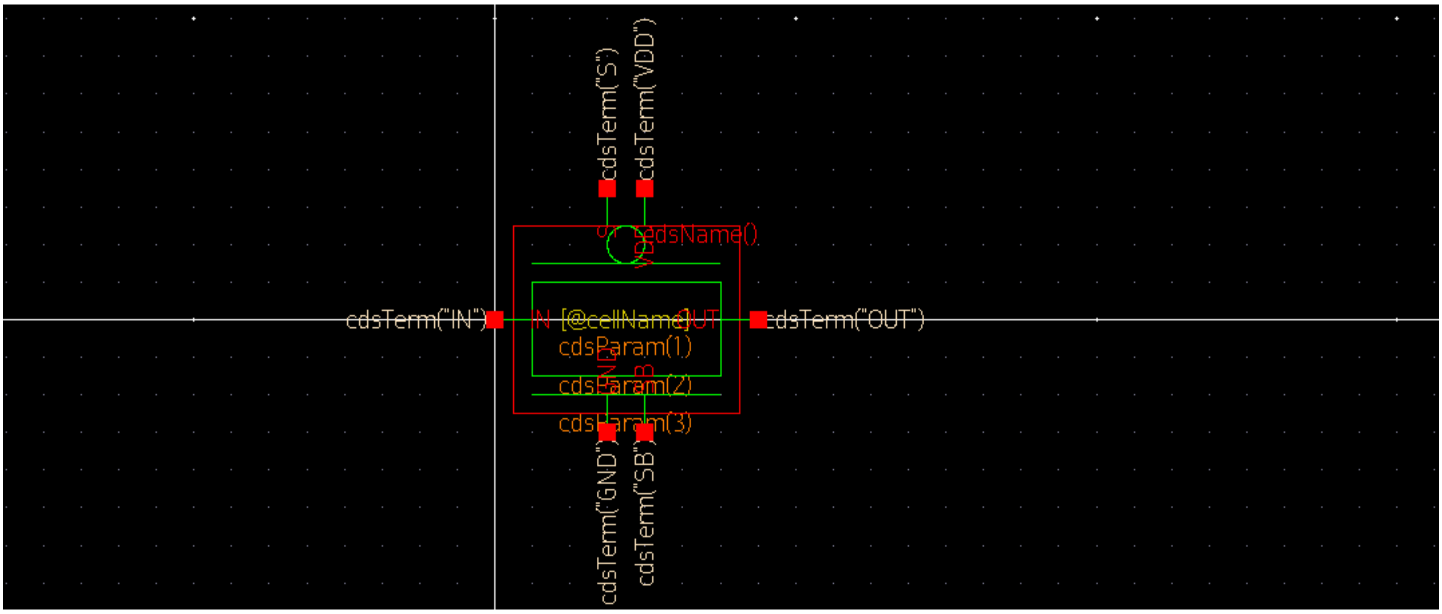
Inverter Symbol:



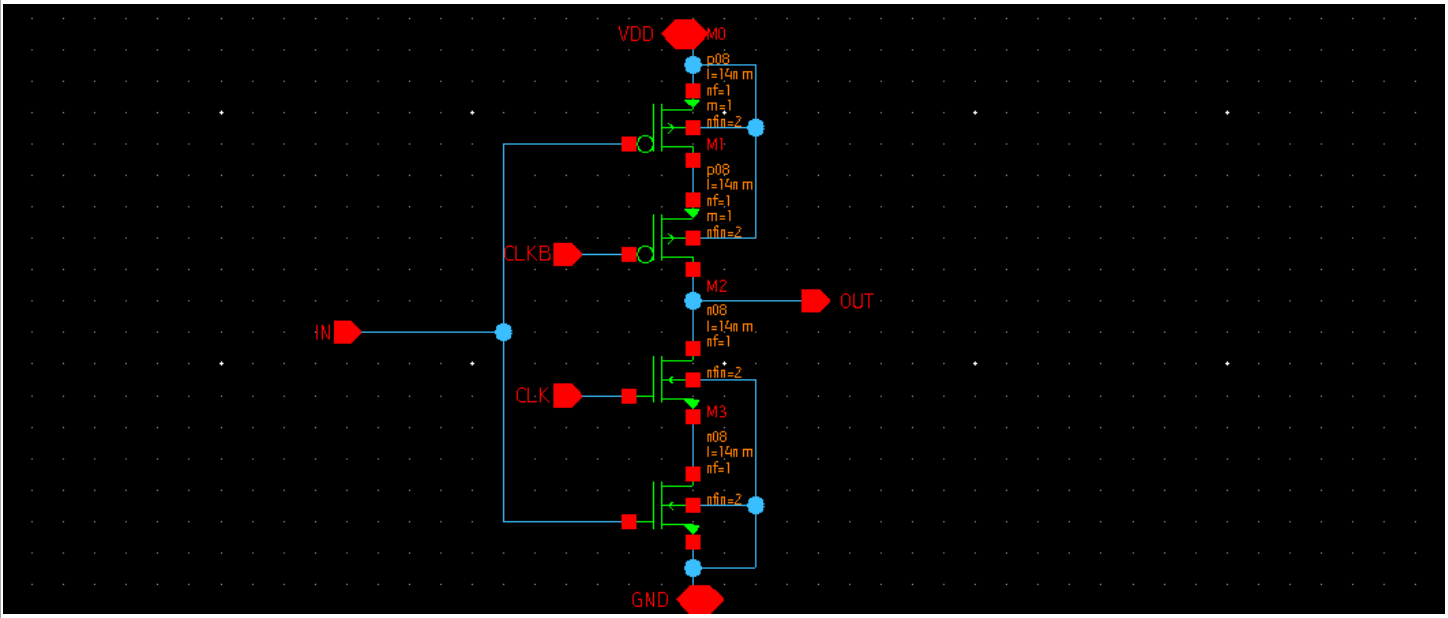
Transmission Gate Schematic:



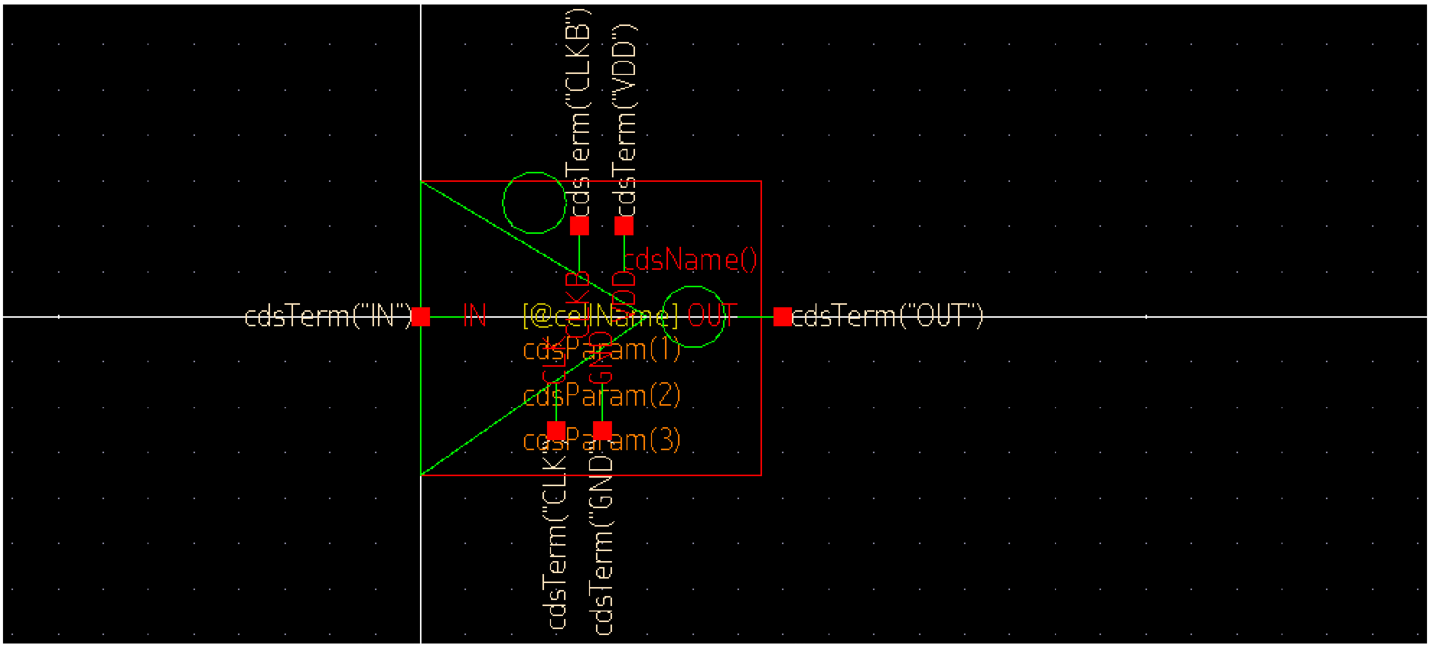
Transmission Gate Symbol:



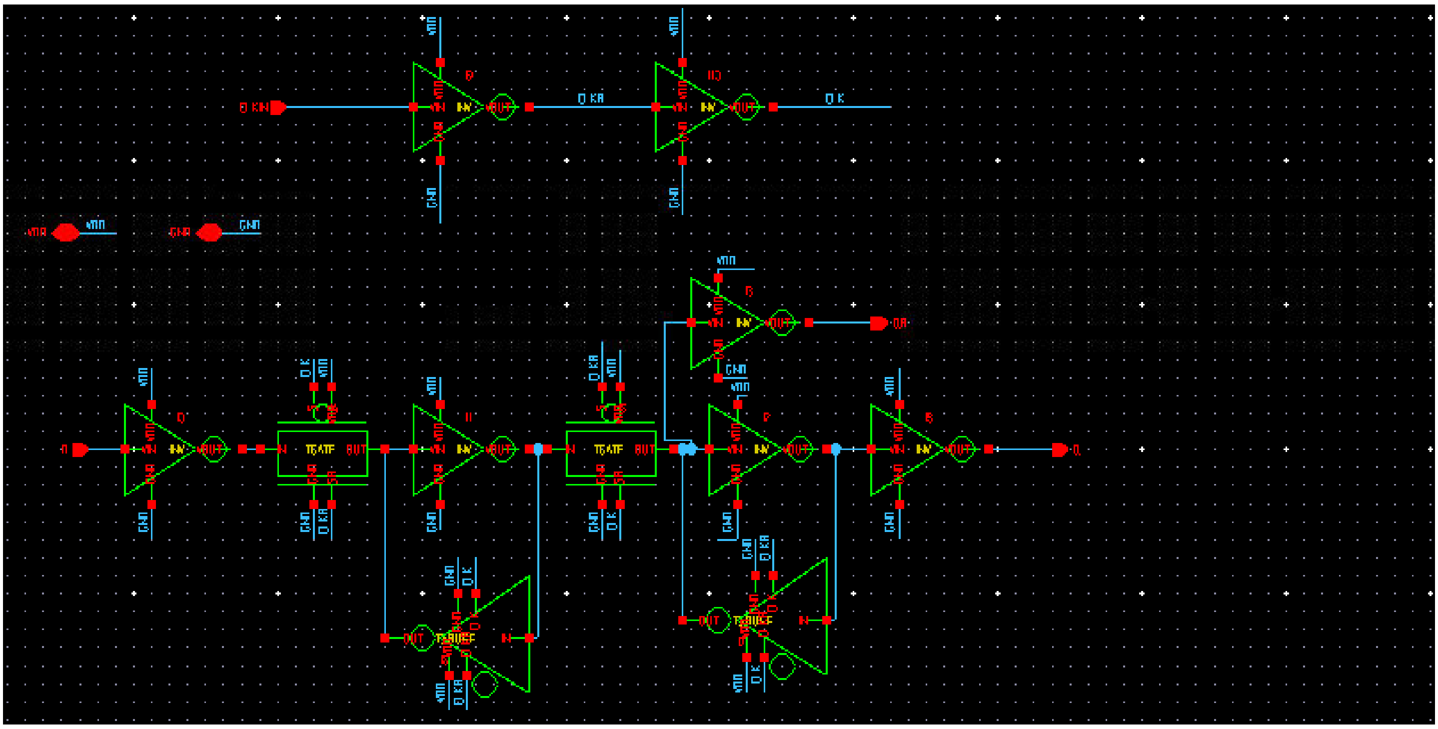
Tri-State Buffer Schematic:

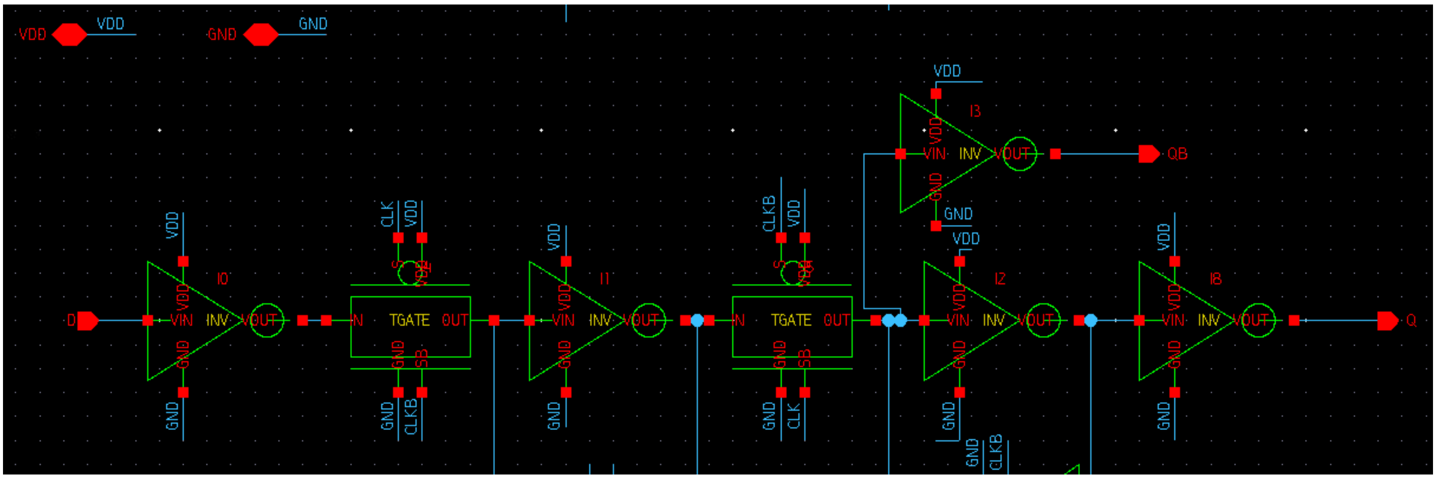


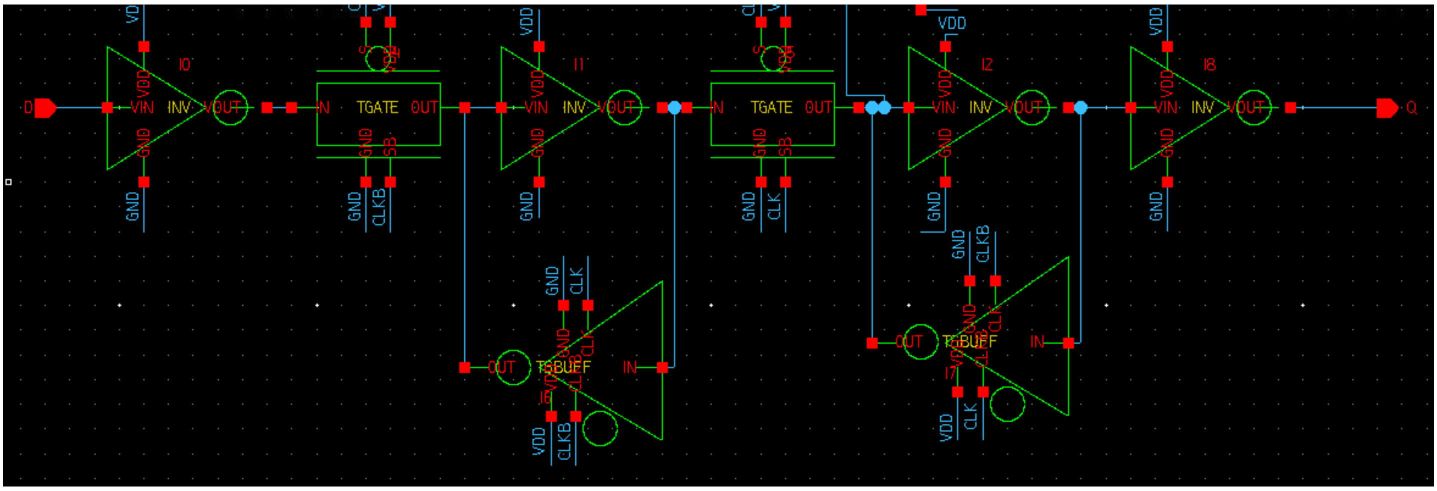
Tri-State Buffer Symbol:



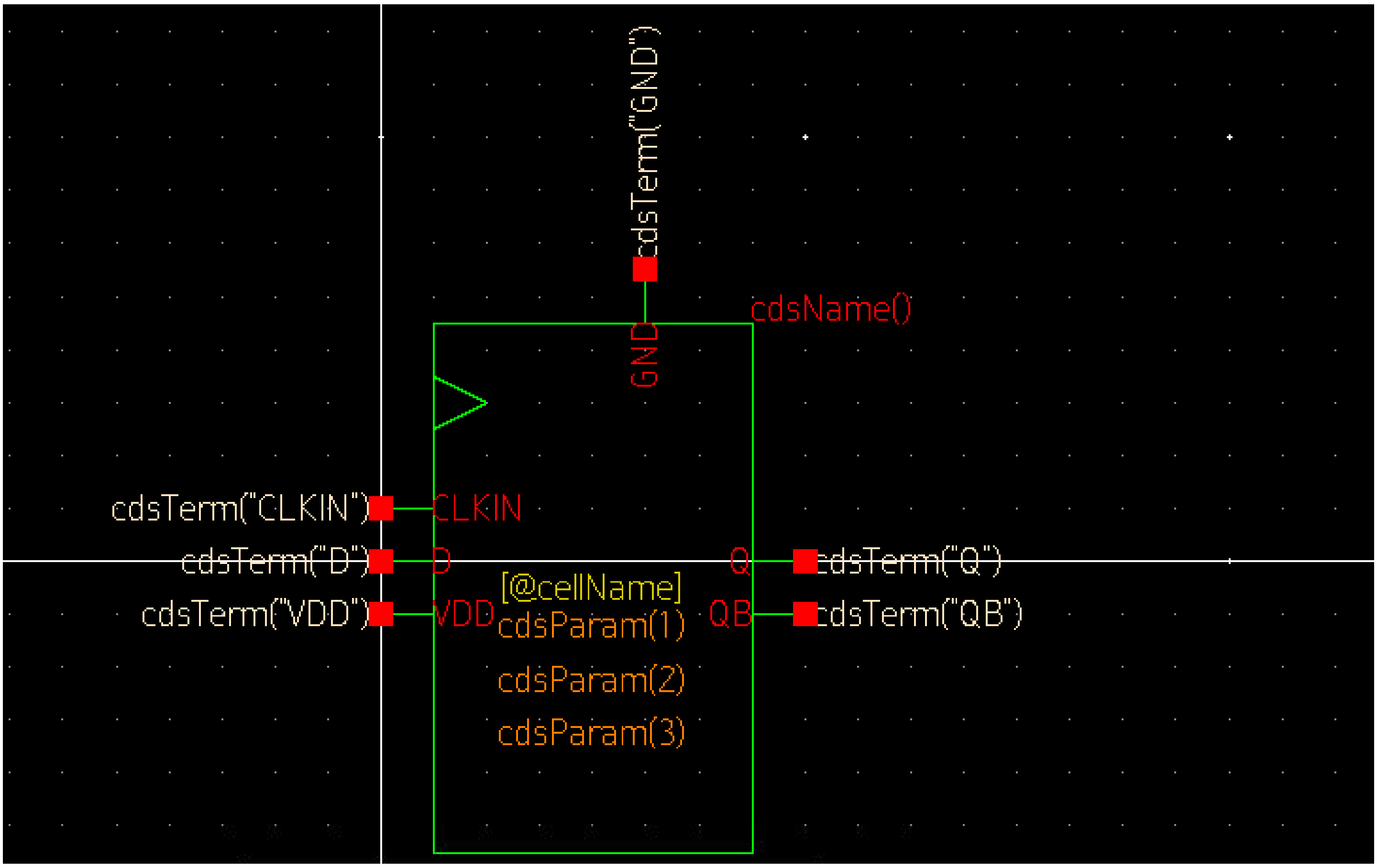
Flip-Flop Schematic:



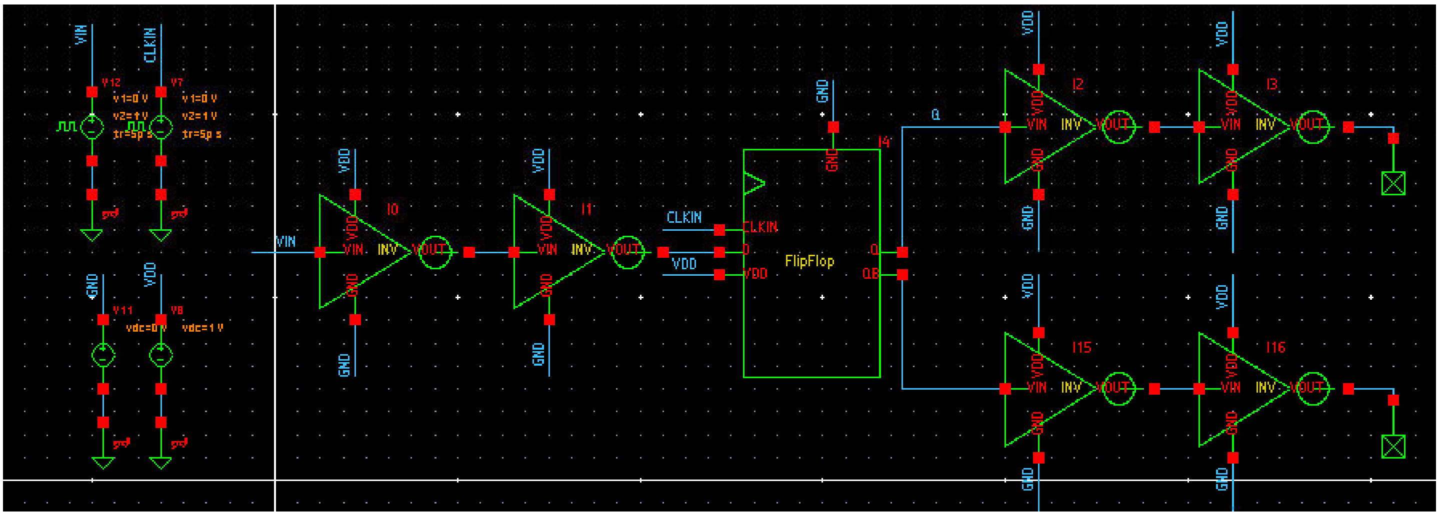




Flip-Flop Symbol:



Part Two: Flip-Flop Testbench:



Here we were asked to shape the input & the output, thus two inverters were used for every input & output.

Now for setting the vpulse sources for the input & clock:

Clock Pulse: The period was set to 70p s because we were asked to set the clock pulse to 10*FO4 & FO4 is = Lmin/2. Since we're working on 14nm tech so FO4 = 7. The pulse width = Period/2.

Trise & Tfall were set to 5p s as a reasonable value that we usually use.

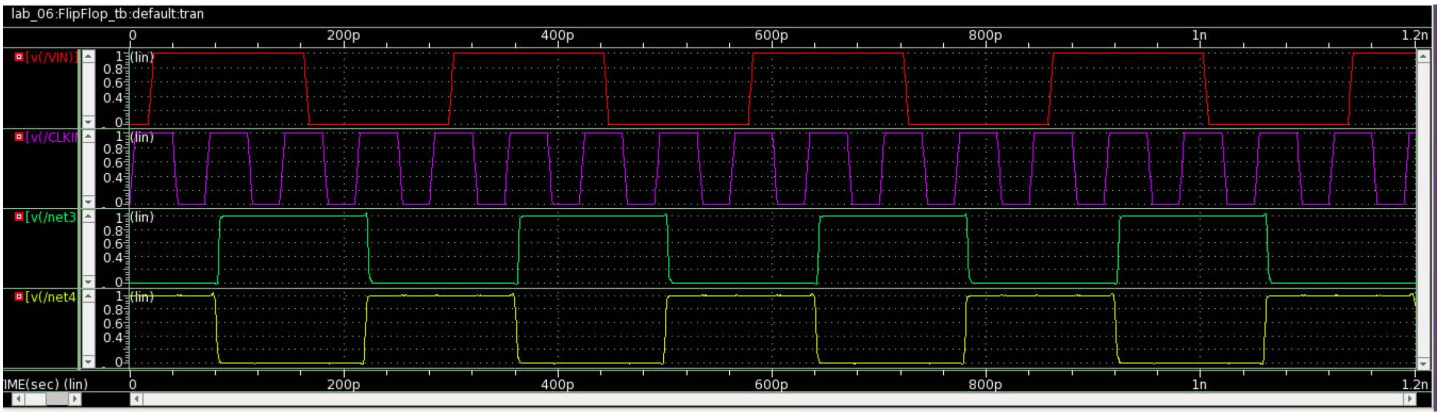
The Input signal pulse was set according to the lab requirements in the sheet.

Transient Analysis:

tran tran ✓ Start Time: 0 Time Step: 1p Stop Time: 140p

Note: Stop time in the results is set to 1200p s to see 4 input pulses in the plot.

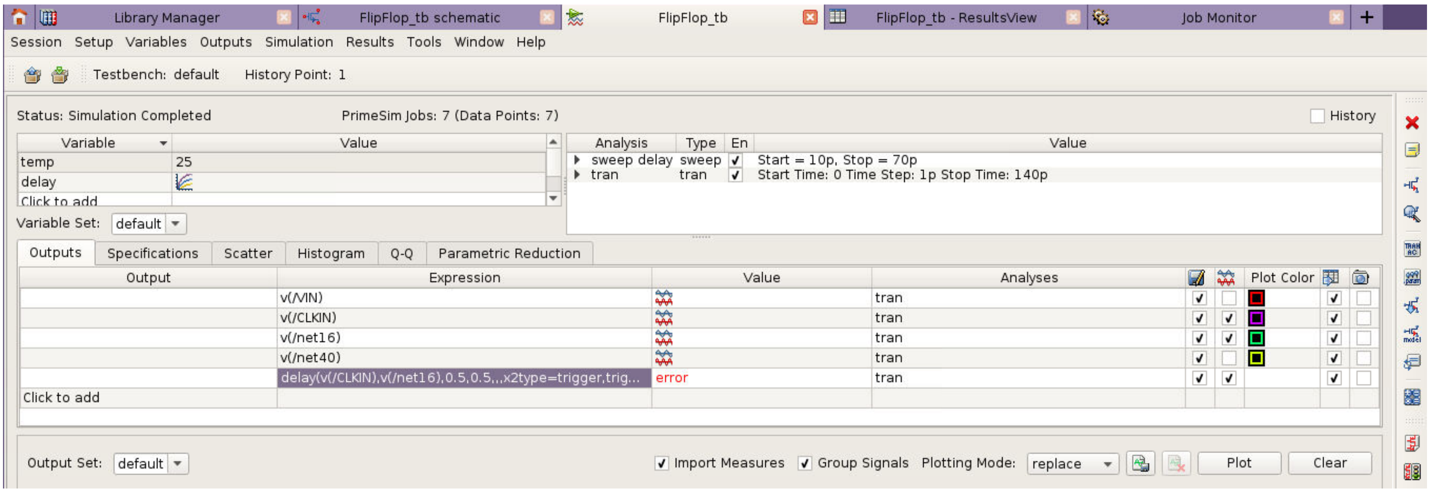
The Resulting Waveform:



Note: Net3 Represents Q & Net4 Represents Q_Bar. Notice that in every positive clock edge after the input rises to 1, the output Q rises to 1 & Q_Bar falls to 0.

Part Three: Delay

First Trial: Setting the delay equation in the “Ëxpression” part & running a parametric sweep on a delay parameter set to the input pulse: 10p:10p:70p.



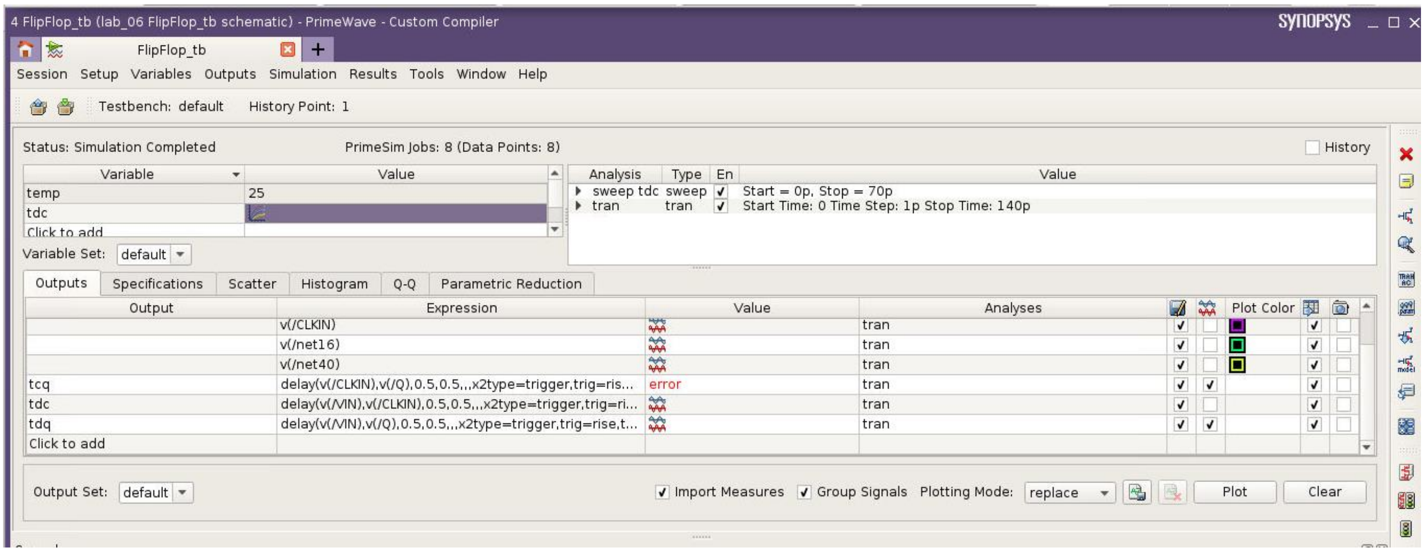
The resulting delay values were as follows:

Violations	Min	Max	delay 10p	delay 20p	delay 30p	delay 40p	delay 50p	delay 60p	
< Filter	< Filter	< Filter	< Filter	< Filter	< Filter	< Filter	< Filter	< Filter	<
1	12.2185p	12.2599p	12.2538p	12.2541p	12.2599p	12.2315p	12.2495p	12.2185p	er

But it was more reasonable to set the delay variable for the clock, so next I set a delay variable called tdc to the clock & set that of the input to 0. The tdc variable was sweeped to 10p:10p:70p as well.

Next I added the tdc expression to primewave.

Moreover, I added two variables to the output & set their expressions as well (The same expression but with changing the evaluated terms). As shown below:



The expressions are shown here:

tcq:

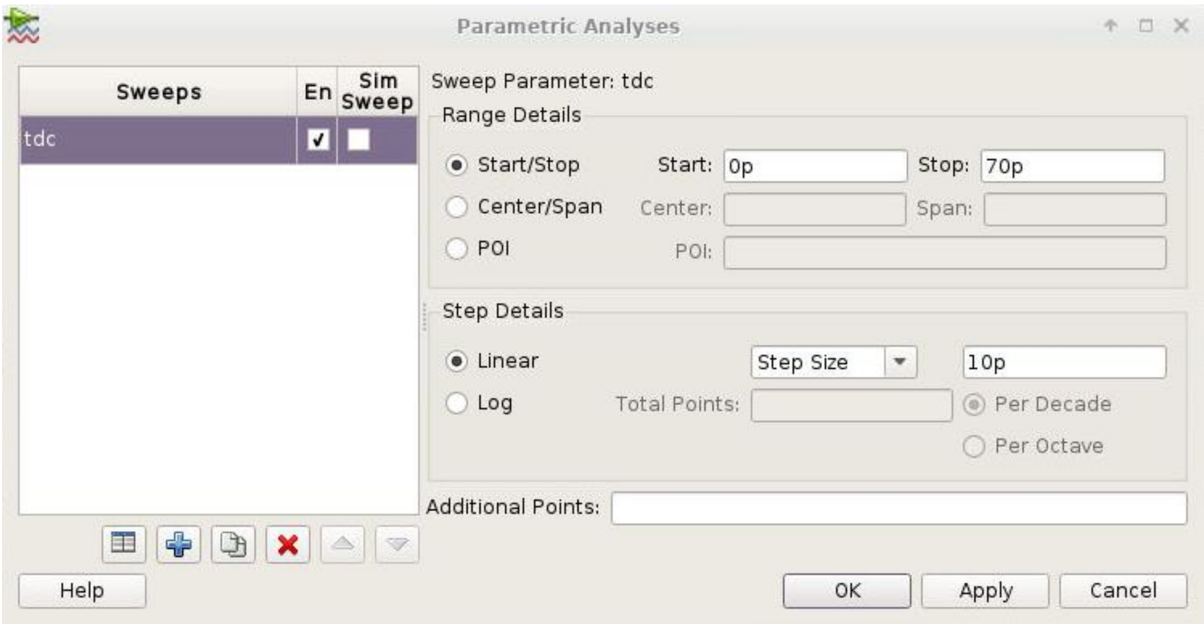
delay(v(/CLKIN),v(/Q),0.5,0.5,,,x2type=trigger,trig=rise,target=either,occu=multiple)

tdc:

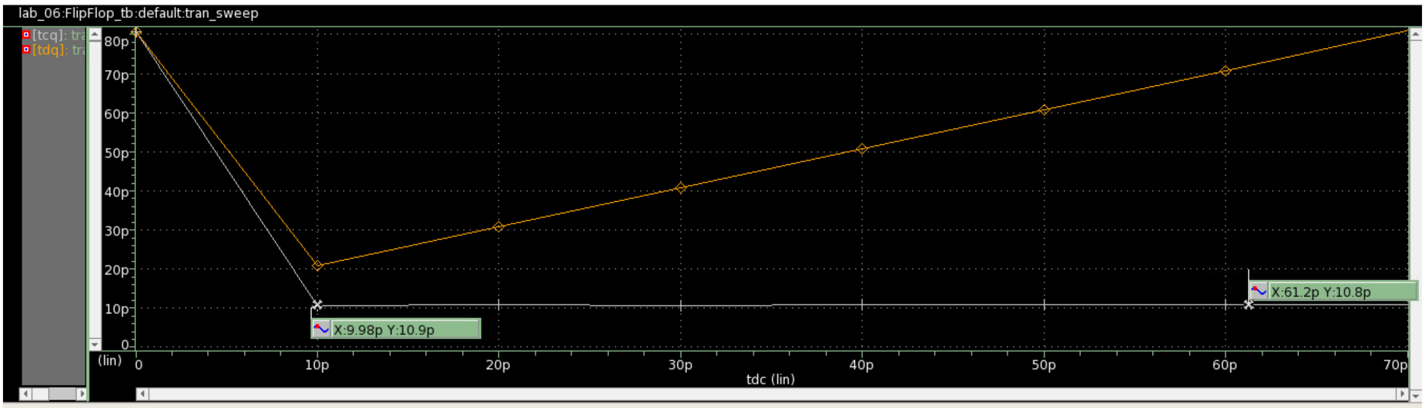
delay(v(/VIN),v(/CLKIN),0.5,0.5,,,x2type=trigger,trig=rise,target=either,occu=multiple)

tdq:

delay(v(/VIN),v(/Q),0.5,0.5,,,x2type=trigger,trig=rise,target=either,occu=multiple)



This was the resulting plot: It seems reasonable and close to what we've happened to study in the lecture.



Now using the measurement tool & Data(x,y) to get the delay values which happened to be:

Tccq = 10.8p s & to get it in terms of FO4 we divide this value by 7.

Tpcq = 10.9 ps

Tsetup (The point on x at which the slope = -1) = 9.98 p s.

If it's needed, here are the delay values for different points in the plot:

Consolidated | Pass/Fail

Testbench	Equations	Specification	Violations	Min	Max	tdc 0	tdc 10p	tdc 20p	tdc 30p	tdc 40p	tdc 50p	tdc 60p	tdc 70p
default	tcq:tran		0	10.7453p	80.7861p	80.7861p	10.7453p	10.7905p	10.7651p	10.7969p	10.7845p	10.7933p	10.7872p
	tdc:tran		0	0	70p	0	10p	20p	30p	40p	50p	60p	70p
	tdq:tran		0	20.7453p	80.7872p	80.7861p	20.7453p	30.7905p	40.7651p	50.7969p	60.7845p	70.7933p	80.7872p