5. I/O Multiplexing and Considerations

5.1 Multiplexed Signals

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions A, B, C, D, E, F, G or H. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0-31) in the PORT must be written to one. The selection of peripheral function A to H is done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) in the PORT.

Table 5-1 on page 11 describes the peripheral signals multiplexed to the PORT I/O pins.

Table 5-1. PORT Function Multiplexing

Pin			I/O Pin	Supply	Type	A	B[1][2]					C	D	E	F	G	H
SAMD21E	SAMD21G	SAMD21J				EIC	REF	ADC	AC	PTC	DAC	SERCOM[1][2]	SERCOM-ALT	TC[3]/TCC	TCC	COM	AC/GCLK
1	1	1	PA00	VDDANA		EXTINT[0]							SERCOM1/ PAD[0]	TCC2/WO[0]			
2	2	2	PA01	VDDANA		EXTINT[1]							SERCOM1/ PAD[1]	TCC2/WO[1]			
3	3	3	PA02	VDDANA		EXTINT[2]		AIN[0]		Y[0]	VOUT						
4	4	4	PA03	VDDANA		EXTINT[3]	ADC/VREFA DAC/VREFP	AIN[1]		Y[1]							
		5	PB04	VDDANA		EXTINT[4]		AIN[12]		Y[10]							
		6	PB05	VDDANA		EXTINT[5]		AIN[13]		Y[11]							
		9	PB06	VDDANA		EXTINT[6]		AIN[14]		Y[12]							
		10	PB07	VDDANA		EXTINT[7]		AIN[15]		Y[13]							
	7	11	PB08	VDDANA		EXTINT[8]		AIN[2]		Y[14]			SERCOM4/ PAD[0]	TC4/WO[0]			
	8	12	PB09	VDDANA		EXTINT[9]		AIN[3]		Y[15]			SERCOM4/ PAD[1]	TC4/WO[1]			
5	9	13	PA04	VDDANA		EXTINT[4]	ADC VREFP	AIN[4]	AIN[0]	Y[2]			SERCOM0/ PAD[0]	TCC0/WO[0]			
6	10	14	PA05	VDDANA		EXTINT[5]		AIN[5]	AIN[1]	Y[3]			SERCOM0/ PAD[1]	TCC0/WO[1]			
7	11	15	PA06	VDDANA		EXTINT[6]		AIN[6]	AIN[2]	Y[4]			SERCOM0/ PAD[2]	TCC1/WO[0]			
8	12	16	PA07	VDDANA		EXTINT[7]		AIN[7]	AIN[3]	Y[5]			SERCOM0/ PAD[3]	TCC1/WO[1]		I2S/SD[0]	
11	13	17	PA08	VDDIO	I^2C	NMI		AIN[16]		X[0]		SERCOM0/ PAD[0]	SERCOM2/ PAD[0]	TCC0/WO[0]	TCC1/ WO[2]	I2S/SD[1]	
12	14	18	PA09	VDDIO	I^2C	EXTINT[9]		AIN[17]		X[1]		SERCOM0/ PAD[1]	SERCOM2/ PAD[1]	TCC0/WO[1]	TCC1/ WO[3]	I2S/ MCK[0]	
13	15	19	PA10	VDDIO		EXTINT[10]		AIN[18]		X[2]		SERCOM0/ PAD[2]	SERCOM2/ PAD[2]	TCC1/WO[0]	TCC0/ WO[2]	I2S/ SCK[0]	GCLK_IO[4]
14	16	20	PA11	VDDIO		EXTINT[11]		AIN[19]		X[3]		SERCOM0/ PAD[3]	SERCOM2/ PAD[3]	TCC1/WO[1]	TCC0/ WO[3]	I2S/FS[0]	GCLK_IO[5]

Table 5-1. PORT Function Multiplexing (Continued)

Pin			I/O Pin	Supply	Type	A	B[1][2]					C	D	E	F	G	H
SAMD21E	SAMD21G	SAMD21J				EIC	REF	ADC	AC	PTC	DAC	SERCOM[1][2]	SERCOM-ALT	TC[3]/TCC	TCC	COM	AC/GCLK
	19	23	PB10	VDDIO		EXTINT[10]							SERCOM4/PAD[2]	TC5/WO[0]	TCC0/WO[4]	I2S/MCK[1]	GCLK_IO[4]
	20	24	PB11	VDDIO		EXTINT[11]							SERCOM4/PAD[3]	TC5/WO[1]	TCC0/WO[5]	I2S/SCK[1]	GCLK_IO[5]
		25	PB12	VDDIO	I2C	EXTINT[12]				X[12]		SERCOM4/PAD[0]		TC4/WO[0]	TCC0/WO[6]	I2S/FS[1]	GCLK_IO[6]
		26	PB13	VDDIO	I2C	EXTINT[13]				X[13]		SERCOM4/PAD[1]		TC4/WO[1]	TCC0/WO[7]		GCLK_IO[7]
		27	PB14	VDDIO		EXTINT[14]				X[14]		SERCOM4/PAD[2]		TC5/WO[0]			GCLK_IO[0]
		28	PB15	VDDIO		EXTINT[15]				X[15]		SERCOM4/PAD[3]		TC5/WO[1]			GCLK_IO[1]
	21	29	PA12	VDDIO	I2C	EXTINT[12]						SERCOM2/PAD[0]	SERCOM4/PAD[0]	TCC2/WO[0]	TCC0/WO[6]		AC/CMP[0]
	22	30	PA13	VDDIO	I2C	EXTINT[13]						SERCOM2/PAD[1]	SERCOM4/PAD[1]	TCC2/WO[1]	TCC0/WO[7]		AC/CMP[1]
15	23	31	PA14	VDDIO		EXTINT[14]						SERCOM2/PAD[2]	SERCOM4/PAD[2]	TC3/WO[0]	TCC0/WO[4]		GCLK_IO[0]
16	24	32	PA15	VDDIO		EXTINT[15]						SERCOM2/PAD[3]	SERCOM4/PAD[3]	TC3/WO[1]	TCC0/WO[5]		GCLK_IO[1]
17	25	35	PA16	VDDIO	I2C	EXTINT[0]				X[4]		SERCOM1/PAD[0]	SERCOM3/PAD[0]	TCC2/WO[0]	TCC0/WO[6]		GCLK_IO[2]
18	26	36	PA17	VDDIO	I2C	EXTINT[1]				X[5]		SERCOM1/PAD[1]	SERCOM3/PAD[1]	TCC2/WO[1]	TCC0/WO[7]		GCLK_IO[3]
19	27	37	PA18	VDDIO		EXTINT[2]				X[6]		SERCOM1/PAD[2]	SERCOM3/PAD[2]	TC3/WO[0]	TCC0/WO[2]		AC/CMP[0]
20	28	38	PA19	VDDIO		EXTINT[3]				X[7]		SERCOM1/PAD[3]	SERCOM3/PAD[3]	TC3/WO[1]	TCC0/WO[3]	I2S/SD[0]	AC/CMP[1]
		39	PB16	VDDIO	I2C	EXTINT[0]						SERCOM5/PAD[0]		TC6/WO[0]	TCC0/WO[4]	I2S/SD[1]	GCLK_IO[2]
		40	PB17	VDDIO	I2C	EXTINT[1]						SERCOM5/PAD[1]		TC6/WO[1]	TCC0/WO[5]	I2S/MCK[0]	GCLK_IO[3]
	29	41	PA20	VDDIO		EXTINT[4]				X[8]		SERCOM5/PAD[2]	SERCOM3/PAD[2]	TC7/WO[0]	TCC0/WO[6]	I2S/SCK[0]	GCLK_IO[4]
	30	42	PA21	VDDIO		EXTINT[5]				X[9]		SERCOM5/PAD[3]	SERCOM3/PAD[3]	TC7/WO[1]	TCC0/WO[7]	I2S/FS[0]	GCLK_IO[5]
21	31	43	PA22	VDDIO	I2C	EXTINT[6]				X[10]		SERCOM3/PAD[0]	SERCOM5/PAD[0]	TC4/WO[0]	TCC0/WO[4]		GCLK_IO[6]
22	32	44	PA23	VDDIO	I2C	EXTINT[7]				X[11]		SERCOM3/PAD[1]	SERCOM5/PAD[1]	TC4/WO[1]	TCC0/WO[5]	USB/SOF 1kHz	GCLK_IO[7]
23	33	45	PA24	VDDIO		EXTINT[12]						SERCOM3/PAD[2]	SERCOM5/PAD[2]	TC5/WO[0]	TCC1/WO[2]	USB/DM	
24	34	46	PA25	VDDIO		EXTINT[13]						SERCOM3/PAD[3]	SERCOM5/PAD[3]	TC5/WO[1]	TCC1/WO[3]	USB/DP	

Table 5-1. PORT Function Multiplexing (Continued)

Pin			I/O Pin	Supply	Type	A	B[1][2]					C	D	E	F	G	H
SAMD21E	SAMD21G	SAMD21J				EIC	REF	ADC	AC	PTC	DAC	SERCOM[1][2]	SERCOM-ALT	TC[3]/TCC	TCC	COM	AC/GCLK
	37	49	PB22	VDDIO		EXTINT[6]							SERCOM5/PAD[2]	TC7/WO[0]			GCLK_IO[0]
	38	50	PB23	VDDIO		EXTINT[7]							SERCOM5/PAD[3]	TC7/WO[1]			GCLK_IO[1]
25	39	51	PA27	VDDIO		EXTINT[15]											GCLK_IO[0]
27	41	53	PA28	VDDIO		EXTINT[8]											GCLK_IO[0]
31	45	57	PA30	VDDIO		EXTINT[10]							SERCOM1/PAD[2]	TCC1/WO[0]		CORTEX_M0P/SWCLK	GCLK_IO[0]
32	46	58	PA31	VDDIO		EXTINT[11]							SERCOM1/PAD[3]	TCC1/WO[1]			
		59	PB30	VDDIO	I^2C	EXTINT[14]							SERCOM5/PAD[0]	TCC0/WO[0]	TCC1/WO[2]		
		60	PB31	VDDIO	I^2C	EXTINT[15]							SERCOM5/PAD[1]	TCC0/WO[1]	TCC1/WO[3]		
		61	PB00	VDDANA		EXTINT[0]		AIN[8]		Y[6]			SERCOM5/PAD[2]	TC7/WO[0]			
		62	PB01	VDDANA		EXTINT[1]		AIN[9]		Y[7]			SERCOM5/PAD[3]	TC7/WO[1]			
	47	63	PB02	VDDANA		EXTINT[2]		AIN[10]		Y[8]			SERCOM5/PAD[0]	TC6/WO[0]			
	48	64	PB03	VDDANA		EXTINT[3]		AIN[11]		Y[9]			SERCOM5/PAD[1]	TC6/WO[1]			

Notes:
1. All analog pin functions are on peripheral function B. Peripheral function B must be selected to disable the digital control of the pin.
2. Only some pins can be used in SERCOM I^2C mode. See the Type column for using a SERCOM pin in I^2C mode.
3. Note that TC6 and TC7 are not supported on the SAM D21G. Refer to "Configuration Summary" on page 3 for details.