20116063

NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR
DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION
Analog IC Design and Simulation (Code: EC108203EC)

Semester 8th

Time: 2.00 PM – 5.00 PM | April. 2024 | Max. Marks: 50

INSTRUCTIONS TO THE CANDIDATES

1) Attempt any Five questions only.
2) Use only pencil HB, B or Pen for diagrams.
3) Numerical question solution should be corrected up to two decimal points.
4) Assume suitable data whenever necessary.

Que 1. (a). Draw and derive I-V characteristics of MOSFETs for different regions of operation. 05

(b). what do you understand by common gate configuration and derive gain with suitable diagram. 05

Que 2. (a). What is differential amplifier explain in detail with equations 05

(b). Explain Gilbert Cell. 05

Que 3. (a). Explain active current with input-output characteristics. 05

(b). Write the difference between active and passive current mirror. 05

Que 4. Write a brief overview of term related to op-amp (2x5=10)

a. Gain boosting

b. Small signal bandwidth

c. Output swing

d. Linearity

e. CMMR

Que 5. Write performance comparison of various op amp configurations. 10

Que 6. Explain and drive gain of CS stage with Resistive load and diode connected load. 10

Que 7. What is common mode rejection ratio? Explain common mode response of differential amplifier. 10

Que 8. What is headroom in current mirror? How cascode current mirror gives minimum headroom explain with design. 10

5/6/8/1

4/3/2/7/1

NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR
DEPARTMENT OF ELECTRONICS AND COMMUNICATION
Analog IC Design and Simulation
(Subject Code EC108203EC)

Time: March. 2024 Max. Marks: 30

INSTRUCTIONS TO THE CANDIDATES

1) Attempt any five questions only.
2) Use onlypencil HB, B or Pen for diagrams.
3) Numerical question solution should be corrected up to two decimal points.
4) Assume suitable data whenever necessary.

Q 1. Derive gain (A_V) equation ofdiode connected load for CS amplifier in terms of Aspect ratio?
Q 2. Derive A_V for CS stage with source degeneration input to CG stage?
Q 3. Derive the voltage gain of the circuit shown in Figure1 if $\lambda \neq 0$ and $\Upsilon \neq 0$?\

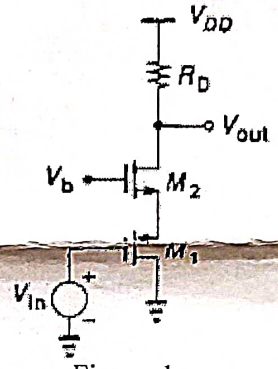

Figure 1

Q 4. Derive the voltage gain equation for source follower with $\lambda \neq 0$.
Q 5. For the circuit of Figure2, Calculate the small signal voltage gain if $(W/L)_1 = 50/0.5$, $(W/L)_2 = 10/0.5$, and $I_{D1} = I_{D2} = 0.5$ mA. What is the gain, if M_2 is implemented is a diode connected PMOS device in Figure2.

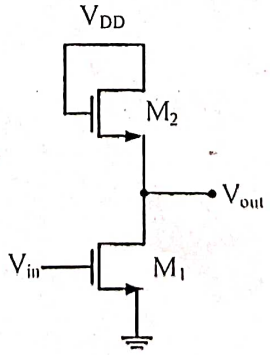

Figure 2

Q 6. Explain PMOS current mirror and establisede relation between I_{ref} and I_{out}?
Q 7. Brief describe Gilbert Cell?
Q 8. Calculate small signal voltage gain with Active load of differential pair amplifier?

Table Level 1 SPICE Models for NMOS and PMOS Devices.

NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e−6	UO = 350	LAMBDA = 0.1
TOX = 9e−9	PB = 0.9	CJ = 0.56e−3	CJSW = 0.35e−11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e−9	JS = 1.0e−8
PMOS Model			
LEVEL = 1	VTO = −0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e−6	UO = 100	LAMBDA = 0.2
TOX = 9e−9	PB = 0.9	CJ = 0.94e−3	CJSW = 0.32e−11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e−9	JS = 0.5e−8

Roll No. 20116063

NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR

Department of Electronics and Communication

End Semester Examination (Apr–2024)

SEM: VIII (CBCS) Subject: Semiconductor Device Modelling CODE: EC108202EC

Time: 3 hours Maximum Marks: 50

Note: 1) Attempts of all the questions are compulsory.
2) Assume suitable data wherever necessary. (Given ϵ_r for SiO_2 is 3.9)
3) Use a neat and clean HB pencil/black pen to draw the figures.

Q.1	(a) Consider an n^+ polysilicon-silicon dioxide –n-type silicon MOS structure. Let $N_d = 4 \times 10^{15}\ cm^{-3}$. The ideal flat-band voltage is -0.42V for $t_{ox} = 20nm$, determine the shift in flat-band voltage for (i) fixed oxide charge $Q'_{ss} = 4 \times 10^{10}\ cm^{-2}$ and (ii) $Q'_{ss} = 10^{11}\ cm^{-2}$. (iii) Repeat parts (i) and (ii) for an oxide thickness of $t_{ox} = 12nm$. OR (a) (i)An ideal n-channel MOSFET has parameters $t_{ox} = 18nm$, $\mu_n = 450\ cm^2/V-s$, and $V_T = 0.4$ V. The measured current in saturation region is $I_{D(sat)} = 0.8$ mA when biased at $V_{GS} = 2.0$ V. Determine the process conduction parameter and width-to-length ratio. (ii) An ideal p-channel MOSFET has parameters $t_{ox} = 18nm$, $\mu_p = 210\ cm^2/V-s$, and a threshold voltage of $V_T = -0.4$ V. The measured current in saturation region is also $I_{D(sat)} = 0.8$ mA when biased at $V_{SG} = 2.0$ V. Determine the process conduction parameter and width-to-length ratio. (b) Differentiate the lift-off and etching method in terms of process steps with suitable diagram.	6+4
Q. 2	(a) Sketch the energy-band diagrams in a MOS capacitor with an n-type substrate in accumulation, depletion, and inversion modes with proper justification. (b). The substrate doping and body effect coefficient of an n-channel MOSFET are $N_a = 10^{16}\ cm^{-3}$ and $\gamma = 0.12\ V^{1/2}$, respectively. The threshold voltage is found to be $V_{TN} = 0.5$ V when biased at $V_{SB} = 2.5$ V. What is the threshold voltage at $V_{SB} = 0$ V ?	6+4
Q. 3	(a). Sketch cross-section and side view a fabrication flow of development of HEMT device. (b). What is the advantage of a HEMT compared to a MESFET?	5+5
Q. 4	(a). Consider an abrupt $N - Al_{0.3}Ga_{0.7}As$ – intrinsic GaAs heterojunction. The N-AlGaAs is doped to $N_d = 2 \times 10^{18}\ cm^{-3}$. The schottky barrier height is 0.85 V and the heterojunction conduction-band edge discontinuity is $\Delta E_C = 0.22$ eV. Determine the thickness of AlGaAs layer so that $V_{off} = -0.3$ V. (Given ϵ_r for $Al_{0.3}Ga_{0.7}As$ is 12.2). OR Consider an $N - Al_{0.3}Ga_{0.7}As$ – intrinsic GaAs abrupt heterojunction. Assume that AlGaAs is doped to $N_d = 3 \times 10^{18}\ cm^{-3}$ and has a thickness of 350Å. Let the $\emptyset_{Bn} = 0.89$ V, and assume that $\Delta E_C = 0.24$ eV. (a) Calculate V_{off} and (b) calculate n_s for $V_g = 0$. (Given ϵ_r for $Al_{0.3}Ga_{0.7}As$ is 12.2 and correction factor (Δd) is 80 Å). (b). Explain the crystal lattice. Write the significance of Miller indices in device fabrications.	6+4
Q. 5	(a). Describe the meaning of degenerate and nondegenerate semiconductor materials. Discuss the concept of charge neutrality (b). Sketch a fabrication process flow of development of homo-junction p-n device.	5+5

NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR
DEPARTEMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

B.Tech, 8th Sem, Sub-SDM (EC108202 EC)

Time: 2 hours **Maximum Marks: 30**

Note: 1) Attempts of all the questions are compulsory.
2) Assume suitable data wherever necessary.
3) Use a neat and clean HB pencil/black pen to draw the figures.

Q1. Answer the following questions.

(a) How do we modify the density of electron/holes in semiconductors? 2

(b) What happens to majority and minority carriers in n-type Si as temperature increases? 2

(c) Justify net current in P-N junction is zero under open circuited condition. 2

(d) If saturation current is 10^{-16} A and we measure a forward current of 1mA, what voltage is applied to the diode? 2

(e) Draw ideal and practical I-V characteristic of diode 2

Q2 Draw charge density, E-field, potential, potential energy and energy band diagram of heterostructure n-p junctions assuming n-GaAs and p-AlGaAs with x=0.30. [Hint-Electron affinity 3.6eV ($Al_xGa_{1-x}As$); 4.07eV (GaAs) and bandgap 2.67eV ($Al_xGa_{1-x}AS$); 1.42eV (GaAs) are given]. 5

OR

Q3. Draw charge density, E-field, potential, potential energy and energy band diagram of double heterostructure n^+-n-p junctions assuming n^+-GaAs, n-GaAs and p-AlGaAs with x=0.30. 5

Q4. A Silicon PN junction is formed with doping levels $N_A = 3*10^{16}$ cm $^{-3}$and $N_D = 2*10^{15}$ cm^{-3}. a) Determine the hole and electron concentration on both sides of the PN junction assuming 100% ionization. b) Built in potential voltage at 250K and 300K. 5

OR

Q5. Analyses depletion region width in energy band diagram of a PN junction when (i) it is short circuited (applied voltage =0) and (ii) forward biasing is changed 1V to 2.5V with detailed justification regarding change in depletion width and formation of depletion layer. 5

Q6. Illustrate the sources of electron hole pair generation in semiconductors. Explain various recombination mechanisms with suitable diagram– SHR, Auger, Radiative. 5

Q7. What is the meaning of the density of states function? What was the mathematical model used in deriving the density of states function? In general, what is the relation between density of states and energy? 5

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NIT Code : EC108301EC

B. Tech. (8th Sem.) End-Semester Examination, April 2024

Subject: Computer Vision

Branch: Electronics & Communication Engineering

Time: Three Hours | **Max Marks: 50** | **Min Pass Marks: 18**

NOTE:

- **All questions are compulsory.**
- **Associated marks are mentioned at the end of each question within [ ].**
- **Write all parts of one question in one place only.**
- **Answer must be to the point and justify the marks allotted.**

Q. 1 Consider the following image shown in below figure. Apply 5x5 LoG operator for $\sigma = 1.4$ in on the highlighted pixels of the given image. **[05]**

9	9	9	9	9	9	9	9	9	9	9
9	9	9	9	9	9	9	9	9	9	9
9	9	9	9	9	9	9	9	9	9	9
4	4	4	4	4	4	4	4	4	4	4
6	6	6	6	6	6	6	6	6	6	6
6	6	6	6	6	6	6	6	6	6	6
6	6	6	6	6	6	6	6	6	6	6

Q. 2 a) Consider a projection matrix $P = \begin{bmatrix} 8 & 51 & 4 & 0 \\ 7 & 8 & 19 & 0 \\ 10 & -5 & 8 & 1 \end{bmatrix}$, compute the camera center C in world coordinates. **[05]**

b) Consider a pixel p in RGB space given by $\begin{bmatrix} 100 \\ 150 \\ 90 \end{bmatrix}$. What is the corresponding value of the pixel p in CMY and HSV space? **[05]**

Q. 3 a) Consider a plane induced homography **[05]**

$$H = \begin{bmatrix} 4 & 3 & 1 \\ 4 & 5 & 6 \\ 2 & 8 & 2 \end{bmatrix}$$

of a stereo imaging set up. Epipole e′(5, 3) in right image plane and a point x(4, 8) in left image plane are given. Compute the epipolar line (l′) on which the corresponding point of x will lie in right image plane.

b) Compute the essential matrix E, provided calibration matrices of two cameras in stereo set up as **[05]**

K (left camera) $= \begin{bmatrix} 4 & 1 & 2 \\ 2 & 3 & 3 \\ 1 & 1 & 1 \end{bmatrix}$ and K′ (right camera) $= \begin{bmatrix} 5 & 1 & 2 \\ 2 & 2 & 3 \\ 1 & 4 & 1 \end{bmatrix}$ along with fundamental matrix $F = \begin{bmatrix} 4 & 2 & 3 \\ 1 & 1 & 1 \\ 4 & 2 & 3 \end{bmatrix}$.

c) Consider a stereo imaging set up with two cameras $P = \begin{bmatrix} 2 & 0 & 0 & 0 \\ 0 & 2 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix}$ (left camera) and $P' = \begin{bmatrix} 2 & 0 & 0 & 3 \\ 0 & 2 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix}$ (right camera). If the image coordinates of a 3-D point are (3, 3) and (0, 3) in left and right cameras, compute its depth (z-coordinate) in the 3D. [05]

d) Consider a camera with calibration matrix $K = \begin{bmatrix} 2 & 1 & 2 \\ 0 & 1 & 0 \\ 0 & 0 & 2 \end{bmatrix}$ and a right calibration matrix $K' = \begin{bmatrix} 0 & 1 & 3 \\ 1 & 2 & 2 \\ 0 & 0 & 1 \end{bmatrix}$. The right camera has $R = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix}$. Compute the fundamental matrix F. [05]

Q. 4 a) Explain the Viola-Jones algorithm for face detection. How does it work, and what are its strengths and limitations? [05]

b) Compare and contrast different approaches to object recognition, such as feature-based methods, deep learning-based methods, and hybrid approaches. [05]

c) Define category recognition and its significance in computer vision tasks. [05]

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NIT Code : EC108301EC

B. Tech. (8th Sem.) Mid-Term Examination, March 2024

Subject: Computer Vision

Branch: Electronics & Communication Engineering

Time: Two Hours

Max Marks: 30

Min Pass Marks: 12

NOTE:

- **All questions are compulsory.**
- **Associated marks are mentioned at the end of each question within [ ].**
- **Write all parts of one question in one place only.**
- **Answer must be to the point and justify the marks allotted.**

Q. 1 Compute the point of intersection of the lines $2x + 1 = 0$ and $x + 3y + 1 = 0$. **[02]**

Q. 2 Detect edge in the following image using magnitude and direction of the gradient (Ignore border) using Sobel operator? **[05]**

1	2	3	4	5
3	4	5	6	7
5	6	7	8	9
7	8	9	10	11
9	10	11	12	13

Q. 3 Explain how the SIFT operator achieves invariance to (i) illumination; (ii) scale; (iii) rotation. **[05]**

Q. 4 Show that average value of the Laplacian of Gaussian operator is zero. **[03]**

Q.5 *What do you understand by Camera Calibration?* **[05]**

Q.6 *What is a color space? Explain its classification.* **[05]**

Q.7 *Find the vanishing line for the homography matrix H given as* **[05]**

$$H = \begin{bmatrix} 1 & 1 & -2 \\ 2 & 0 & 1 \\ 0 & 2 & -1 \end{bmatrix}$$

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2/7

Roll No. .....

NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR
Department of Electronics and Communication Engineering
VIII Semester, B.Tech. End Semester Examination April-2024
Sub: Cryptography and Network Security, Code: EC108302EC

Time: 3 Hours **Max. Marks: 50**

Answer any ten questions

Q.1 (a) Convert the plain text "ATTACK" into cipher text using Ceaser Cipher with shift key of 3.

(b) Convert the plain text "ATTACK" into cipher text using Hill cipher with key matrix $\begin{bmatrix} 2 & 3 \\ 4 & 5 \end{bmatrix}$. [5]

Q.2. Briefly describe "SubBytes", "ShiftRows", "MixColumns", and "AddRoundKey" of AES encryption algorithm? [5]

Q.3. Explain about the RSA cryptosystem. Perform encryption and decryption using **RSA algorithm** for the following: $p\ (prime\ number) = 3, q\ (prime\ number) = 11, e\ (public\ key) = 7, M\ (plaintext) = 5$ [5]

Q.4. Briefly explain the Diffie-Hellman key exchange algorithm. Consider a Diffie-Hellman scheme with a common prime $q = 11$ and a primitive root $\alpha = 2$. [5]

i. Show that 2 is a primitive root of 11.
ii. If user A has public key $Y_A = 9$, what is A's private key X_A?
iii. If user B has public key $Y_B = 3$, what is the shared secret key K, shared with A?

Q.5. What are the differences between MD5 and MD4 message digest algorithm? Explain in detail the MD5 compression function. [5]

Q.6. Differentiate between SHA-1 and SHA-512 with respect to digest size, message size, block size, word size, and number of steps. Draw the general structure of SHA-1 hash algorithm. [5]

Q.7. What are the requirements for a hash function? Consider the following hash function. Messages are in the form of a sequence of decimal numbers, $M = (a_1, a_2, a_3, a_4, a_5, a_6)$. Calculate the hash value h by using the function $h = (\sum_{i=1}^{6} a_i)\ mod\ n$, for some predefined value of n. Use the message $M = (15, 17, 18, 20, 23, 29)$ and $n = 15$. Does this hash function satisfy any of the requirements for a hash function? Explain your answer.

Q.8. What are the five principal services provided by PGP? Explain each of them in detail. [5]

Q.9. Explain the following types of viruses (i) Parasitic virus, (ii) Memory-resident virus, (iii) Boot sector virus, (iv) Stealth virus, (v) Polymorphic virus, (vi) Metamorphic virus [5]

Q.10. List and briefly define three classes of intruders. What is the difference between statistical anomaly detection and rule-based intrusion detection? [5]

Q.11. Explain the following terminologies of Malicious programs (i) virus, (ii) Worm, (iii) Logic bomb, (iv) Trojan horse, (v) Trapdoor [5]

Q.12. Explain briefly Hardware Trojan Detection Methods. [5]

Roll No. 20116063

NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR
Department of Electronics and Communication Engineering
VIII Semester, B.Tech. MID Semester Examination Mar-2024
Sub: Cryptography and Network Security, Code: EC108302EC

Time: 2 Hours **Max. Marks: 30**

Answer any six questions

Q.1 Encrypt the plaintext "CRYPTOGRAPHY" using the Caesar cipher with the key 3 (Three) and also using the Hill cipher with the key $\begin{pmatrix} 9 & 4 \\ 5 & 7 \end{pmatrix}$. [5]

Q.2. Explain about the RSA cryptosystem. Perform encryption and decryption using **RSA algorithm** for the following: $p\ (prime\ number) = 3, q\ (prime\ number) = 11, e\ (public\ key) = 7, M\ (plaintext) = 5$ [5]

Q.3. What is the difference between a Block cipher and a Stream cipher? What is Brute-force attack? [5]

Q.4. Briefly explain the Diffie-Hellman key exchange algorithm. Consider a Diffie-Hellman scheme with a common prime $q = 11$ and a primitive root $\alpha = 2$. [5]

i. Show that 2 is a primitive root of 11.
ii. If user A has public key $Y_A = 9$, what is A's private key X_A?
iii. If user B has public key $Y_B = 3$, what is the shared secret key K, shared with A?

Q.5. What are the parameters and design features of a **Feistel Network**? In **Feistel Cipher**, prove that "output of the first round of the decryption process is the 32-bit swap of the input to the sixteenth round of the encryption process." [5]

Q.6. Using suitable blocks, explain Output Feedback Mode (OFB) of operation. Explain how Output Feedback Mode (OFB) of operation is better than Cipher Feedback (CFB) mode of operation. [5]

Q.7. Briefly explain DES algorithm. In DES algorithm, the input to S-box 1 is **100011**. What is its corresponding output? [5]

	0	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*	*11*	*12*	*13*	*14*	*15*
0	14	04	13	01	02	15	11	08	03	10	06	12	05	09	00	07
1	00	15	07	04	14	02	13	10	03	06	12	11	09	05	03	08
2	04	01	14	08	13	06	02	11	15	12	09	07	03	10	05	00
3	15	12	08	02	04	09	01	07	05	11	03	14	10	00	06	13

(S-box 1)

6/11
3/11
Leave

20116063

NIT RAIPUR, ECE DEPARTMENT

OPTICAL COMMUNICATION (MID SEMESTER EXAM – 2023)

7th Semester ECE Full Marks: 30 Time: 2 Hours

Answer all questions (The figures in the right-hand margin indicate marks)

1. [2 x 5 = 10]

   a. Mention the merits and demerits of fiber optic communication systems.

   b. List the non-linear effects observed in fiber optic system?

   c. Explain about the performance parameters of OTDR.

   d. Explain the characteristics of optical sources.

   e. Draw the DRZ signal for the data bits: 0 1 0 0 1 0 1 1 1 0 1.

2. If a step index fiber has a core of refractive index 1.5, cladding of refractive index 1.49, core diameter of 80 μm, assuming that the fiber is kept in air, calculate critical angle, NA of the fiber. [3]

3. Explain about various types of fiber, their applications, merits and demerits. [3]

4. With neat diagram explain the operation of MZ modulator. [3]

5. What is a DPSK modulator and demodulator, explain its merits and demerits. [3]

6. Explain in detail about OTDR with the complete description of the OTDR trace. [4]

7. A 1550 nm digital fiber optic link needs to operate at 685 Mb/s over 250 km, the fiber has a loss of 0.22 dB/km, and there are 5 splices with loss of 0.2 dB. The coupling loss at the receiver is 2.5 dB and the receiver uses InGaAs APD with sensitivity of – 42 dBm, Calculate the laser power need to launch, assuming system margin of 8 dB. [4]

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National Institute of Technology Raipur
Electronics & Communication Engineering

MID-SEMESTER EXAM

Semester: Autumn
Subject: Wireless Sensor Network
Duration: 2 Hours

Academic Year: 2023-24
Subject Code: EC107203EC
Maximum Marks: 30

Note: There are five questions of six marks each and all are compulsory questions. Answer all questions in the given order of questions.

S.No.	Question	Marks
1(A)	Explain the difference between following concepts as applicable to MAC layer of a wireless sensor network: (i) Transmission Range; (ii) Carrier Sensing Range; and (iii) Interference Range.	3
1(B)	Explain with proper diagram: (i) Hidden node problem: and (ii) Exposed node problem.	3
2(A)	Explain the difference between schedule based MAC protocol and random access MAC protocol. Clearly, enlist the advantages and disadvantages of both types of protocols.	3
2(B)	Explain the mechanism of CSMA/CD and CSMA/CA protocol. Further explain how the above protocol addresses hidden node and exposed node problem.	3
3(A)	Explain the difference between following in context to propagation of wireless signal: (i) Reflection; (ii) Refraction; and (iii) Scattering.	3
3(B)	Explain the difference between coherence time and coherence bandwidth.	3
4(A)	Explain the difference between large scale fading and small scale fading.	3
4(B)	Discuss the wireless communication scenario in which following statistical fading models are applicable: (i) Rayleigh fading; (ii) Rician fading; and (iii) Nakagami Fading.	3
5(A)	Under AWGN channel assumption. derive the probability of error expression for BPSK modulation.	3
5(B)	Explain the variation in BER and spectral efficiency under following modulation schemes: (i) BPSK; (ii) QPSK; (iii) 8PSK	3

20116063 (ECE)

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR
Department of Electronics and Communication
B. Tech. Mid Semester Examination – Sep, 2023
Sub: Real Time Embedded Systems, Code: EC107302EC

Sem.: VII

Max. Marks: 30

Answer any Three questions from each unit.

UNIT I

1. What are Mean Time Between Failure (MTBF) and Mean Time To Repair (MTTR)? What are the differences between MTBF and MTTR? If the availability of an embedded product is 90 % and the MTBF of the product is 30 days, then calculate the MTTR in days/hours for the product. [5]

2. Explain quality attribute in the embedded system development context? What are the different Quality attributes to be considered in an embedded system design? [5]

3. What is hardware software co-design? Explain the fundamental issues in hardware software co-design. [5]

4. Explain the Product-Life-cycle curve of an embedded product development. [5]

UNIT II

5. Explain different types of non-preemptive scheduling algorithms. State the merits and de-merits of each. [5]

6. List the functions of a kernel. What can be the functions outside the kernel? [5]

7. Three processes with process IDs P1, P2, P3 with estimated completion time 10, 5, 7 milliseconds respectively enters the ready queue together in the order P1, P2, P3 (Assume only P1 is present in the 'Ready' queue when the scheduler picks it up and P2, P3 entered 'Ready' queue after that). Now a new process P4 with estimated completion time 6 ms enters the 'Ready' queue after 5 ms of scheduling P1. Calculate the waiting time and Turn Around Time (TAT) for each process and the Average waiting time and Turn Around Time (Assuming there is no I/O waiting for the processes) in the Non-preemptive Last-Come-First-Served (LCFS) Scheduling. Assume all the processes contain only CPU operation and no I/O operations are involved. [5]

8. Memory allocation and management are the most important functions of the kernel. Why? How does memory allocation differ in RTOS and OS? What is memory locking? [5]

20116063

Total Number of Pages: 02	Course: B.Tech
	Sub Code: EC107101EC

7th Semester Examination: December 2023

SUBJECT: OPTICAL COMMUNICATION

BRANCH: ELECTRONICS AND COMMUNICATION ENGINEERING (ECE)

Time: 3 Hour

Max Marks: 50

The figures in the right-hand margin indicate marks.

Part-I

Q1		**Answer any 2 from the following questions:**	
	a)	Explain about the non-linear effects in fiber optic communication, how it can be minimized.	2.5
	b)	What is dispersion in fiber optic system, its types, explain in detail.	2.5
	c)	Explain about the principle and operation of OTDR.	2.5

Part - II

Q2		**Answer any 2 from the following questions:**	
	a)	Explain about optical RZ pulse modulator.	2.5
	b)	Write the merits and demerits of Optical DPSK based system.	2.5
	c)	Explain about optical phase modulators, its types.	2.5

Part-III

Q3		**Answer any 4 from the following questions:**	
	a)	What is optical MSK modulation, explain with neat block diagram, merits and demerits.	5
	b)	A 1310 nm digital fiber optic link needs to operate at 800 Mb/s over 220 km, the fiber has a loss of 0.25 dB/km, and there are 5 splices with loss of 0.3 dB each splice. The coupling loss at the receiver is 4 dB and the receiver uses InGaAs APD with sensitivity of – 40 dBm, Calculate the laser power need to launch assuming system margin of 6 dB.	5
	c)	Define sensitivity, selectivity and fidelity of optical communication receiver. Explain about these in detail.	5
	d)	What is Optical coherent modulation, its types. Mention its merits, demits in terms of SNR.	5

	e)	Explain various types and sources of noise in an optical communication system. How to minimize these noise power?	5
		Part-IV	
Q4		**Answer any 4 from the following questions:**	
	a)	Distinguish between heterodyne and homodyne optical detection techniques in detail.	5
	b)	What is Coherent OFDM technique in optical communication system. Explain about it.	5
	c)	What is optical multi-level modulation, explain with example.	5
	d)	Explain about WDM, DWDM, CWDM, SONET in optical Communication system.	5
	e)	What is eye diagram, Q-factor, bit error rate, timing jitter, explain with neat diagram and also find the relation between BER and Q-factor.	5

*** THE END ***

20116063

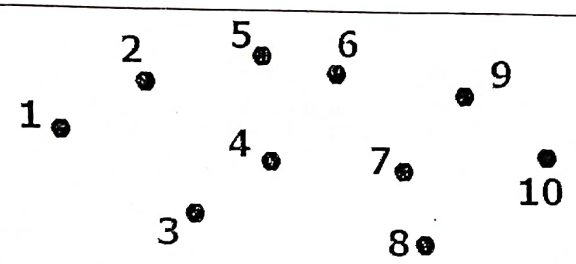
National Institute of Technology Raipur
Electronics & Communication Engineering

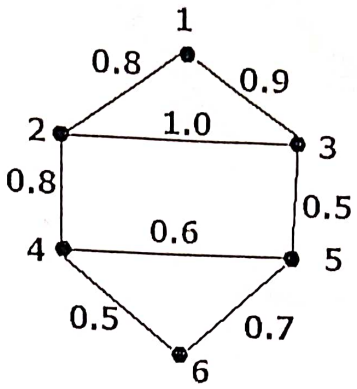
END-SEMESTER EXAM 7th Sem

Semester: Autumn
Subject: Wireless Sensor Network
Duration: 3 Hours

Academic Year: 2023-24
Subject Code: EC107203EC
Maximum Marks: 50

Note: There are ten questions of five marks each and all are compulsory questions. Answer all questions in the given order of questions.

S.No.	Question	Marks
1	 Consider the above sensor node deployment with sensor 2 being the source and sensor 10 being the destination node. (Note this scenario is referred in Question 1, 2, 3, 6 and 7). For the above scenario, explain the routing of packets in following flat-based data centric routing protocols: (a) Flooding; (b) Diffusion. Also discuss the mechanisms by which heavy traffic is avoided in the above protocols.	5
2	Explain how a routing protocol can be characterized as an active or reactive routing protocol. Furthermore, in context to wireless sensor network shown in Question 1, explain the route discovery mechanism in AODV and DSR protocol.	5
3	Conceptualize a graph for the wireless sensor network shown in Question 1. Next formulate a shortest path optimization problem with sensor 2 being the source and sensor 10 being the destination node. Also explain how generic shortest path algorithm can be used to solve the formulated optimization problem.	5
4	Consider the graph shown below for a particular wireless sensor network with	5

	node 1 being the source and node 6 being the destination. Compute the shortest path using (a) Dijkstra method: (b) Bellman-Ford equation.  	
5	Explain with aid of scenarios, how topology control can improve (a) energy efficiency; (b) network capacity. Also briefly mention at least 5 guidelines for designing a topology control solution.	5
6	For the wireless sensor network scenario shown in Question 1, formulate a range assignment problem. Next, in context to the considered wireless sensor network, discuss the following conditions: (a) connectivity; (b) strong connectivity; (c) broadcast; (d) symmetry.	5
7	For the wireless sensor network scenario shown in Question 1, draw the coverage graph assuming sensing range is disc shape centred on the node location and senses at least two nearest nodes. Explain the difference between full coverage, barrier coverage and sweep coverage.	5
8	Draw the structure of physical layer data unit of IEE 802.15.4 protocol. Briefly discuss each of the components in the above data unit.	5
9	Explain with proper diagram: (i) Hidden node problem; and (ii) Exposed node problem. Further explain how these problems are addressed in CSMA protocol.	5
10	Briefly discuss at least five sources energy wastage at MAC layer in a typical wireless sensor network.	5

National Institute of Technology, Raipur, CG- 492010

B.Tech. (Electronics & Communication Engg.) – 7th Semester

EC107201EC (Low Power Circuit Design)

Mid Sem. Exam (Sep. 2023)

Time: 2 hrs **Maximum Marks:** 30

Note: 1) Attempts of all the questions are compulsory.

2) Assume suitable data wherever necessary.

3) Use a neat and clean HB pencil/black pen to draw the figures.

Answer the following questions.

Q.1	Explain read and write operation of 6T SRAM Cell.	**4 Marks**
Q2.	Explain General Memory Architecture using suitable block diagram. How one can fetch information in 16 X 16 DRAM array, Explain in detail.	**4 Marks**
Q.3	Define Programming and Erasing in flash Memory.	**2 Marks**
Q.4	What is the need of low power in CMOS circuit design?	**2 Marks**
Q.5	Explain the different parameters in MOS to reduce the threshold voltage for high switching speed applications?	**2 Marks**
Q.6	Explain the glitch power dissipation in CMOS circuit.	**2 Marks**
Q.7	Explain the VTCMOS and MTCMOS to suppress low power CMOS.	**2 Marks**
Q.8	Derive the expression for short circuit power and switching power dissipation for CMOS Inverter.	**2 Marks**
Q.9	Describe the effects of oxide thickness, silicon thickness, gate length and work function in MOS Device.	**4 Marks**
Q.10	Explain the following technical terms (a) Clock gating (b) Transistor stacking (c) Sense Amplifier (d) Sleep transistor (e) Butterfly curve (f) Cell Ratio	**6 Marks**

NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
EC107201EC - Low Power Circuit Design (Program Elective)
End Semester Exam

20116063

Time: 02:00 PM to 05:00 PM November- 2023

Max. Marks: 50

INSTRUCTIONS TO THE CANDIDATES
1) Use only Pen for diagrams.
2) Assume suitable data whenever necessary.

Q 1. Design CMOS Half-Adder adder using following steps:
(a) Using Basic logic gate [3]
(b) Impliment using CMOS logic Q1. (a). [7]

Q 2. Explain components of Power consumption dynamic and static in CMOS logic? [10]

Q 3. Attempt any two of the following using pass gate logic: -
(a) (i) NOT (ii) AND (iii) OR (iv) NAND
(v) NOR (vi) X-OR (vii) X-NOR
(b) Provide overview of Low-Voltage Low-Power Multipliers?
(c) Explain in Dynamic CMOS Precharge-Evaluate Logic? [5+5]

Q 4. (a) Explain Domino CMOS Logic Charge Sharing?
(b) Explain Domino CMOS Logic An Example of Multiple-Output Domino Circuits? [5+5]

Q 5. Attempt any two of the following: -
(a) Describe the following terms in context of digital IC: -:
(i) Speed of Operation (ii) Power dissipation (iii) Figure of Merit
(iv) Fan In (v) Fan Out (v) Noise Immunity
(vi) Operating Temperature
(b)Design full adder using Complementary Pass Transistor Logic (CPL)?
(c) Design the following logic gates using transmission gate technology
(i) NOT (ii) NAND (iii) NOR
[5+5]

Roll No. 20116063

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR

Department of Electronics and Communication

B. Tech. End Semester Examination – December, 2023

Sub: Real Time Embedded Systems

Sem: VII
Time: 3 Hrs.

Code: EC107302EC
Max. Marks: 50

(Attempt Any Ten Questions)

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1. What are Mean Time Between Failure (MTBF) and Mean Time To Repair (MTTR)? What are the differences between MTBF and MTTR? If the availability of an embedded product is 90% and the MTBF of the product is 30 days, then calculate the MTTR in days/hours for the product. [5]

2. Three processes with process IDs P1, P2, P3 with estimated completion time 6, 4, 2 milliseconds respectively, enters the ready queue together in the order P1, P2, P3. Calculate the waiting time and Turn Around Time (TAT) for each process and the Average waiting time and Turn Around Time (Assuming there is no I/O waiting for the processes) in Round Robin (RR) algorithm with Time slice = 2 ms. [5]

3. What is the difference between Data Flow Graph (DFG) and Control Data Flow Graph (CDFG) model? Explain their significance in embedded system design. Draw a CDFG to incorporate decision nodes at the loop start and loop end to limit the summation terms up to n = 10 for Equation as follows: $y_n = \sum a_i x(n-i) + \sum b_i y(n-1)$ used in an IIR filter. [5]

4. Memory allocation and management are the most important functions of the kernel. Why? How does memory allocation differ in RTOS and OS? What is memory locking? [5]

5. Design an automatic tea/coffee vending machine based on FSM model for the following requirement.
   - The tea/coffee vending is initiated by user inserting a 5 rupee coin.
   - After inserting the coin, the user can either select 'coffee' or 'Tea' or press 'Cancel' to cancel the order and take back the coin. [5]

6. Explain the different types of UML diagrams and their significance in each stage of the system development life cycle. [5]

7. What is 'Process Life Cycle'? Represent the process states and state transition in the Process Life Cycle. [5]

8. Define Shared Memory, Message Passing IPC (Inter Process/Task Communication) mechanism. [5]

P.T.O.

9. What is the difference between Finite State Machine Model (FSM) and Hierarchical/Concurrent Finite State Machine Model (HCFSM)? Design an Automatic Teller Machine (ATM) unit based on FSM model for the following requirements: [5]

- The transaction is started by user inserting a valid ATM card.
- Upon detecting the card, the system prompts for a Personal Identification Number (PIN).
- The card is validated against the PIN and on successful validation; the system displays the following options: 'Balance Enquiry', 'Cash Withdrawal', 'Cancel'.
- If the user selects 'Cash Withdrawal', the system prompts for entering the amount to withdraw and upon entering the amount it asks whether a printed receipt is required for the transaction. Upon receiving an input for this, the system verifies the available balance, deduct the amount to withdraw, dispense the cash, prints the transaction receipt (if the user answer to the system query 'whether a printed receipt is required for the transaction' is 'YES') and returns back to the original state to accept a new transaction request.
- If the user selects the option 'Balance Enquiry', the system prompts the message whether a printed request is required for the transaction. If user response is 'YES', the balance is printed and the system returns to the original state to accept new transaction request. If the user input is 'NO' to the query 'whether a printed receipt is required for the transaction', the balance amount is displayed on the screen for 30 seconds and the system returns back to the original state to accept a new transaction request.
- If the user selects the option 'Cancel', the system returns back to the original state to accept a new transaction request.
- If there is no response from the user for a period of 30 seconds and if the time interval between the two consecutive digits entering for the PIN exceeds 30 seconds, the system displays the message 'User Failed to Respond within the specified Time' for 10 seconds and returns back to the original state to accept a new transaction request.

10. Model the task in case study of Inter-Robot Communication in a Robot Orchestra. [5]

11. Model the task in case study of an embedded system for an Adaptive Cruise Control System in a Car. [5]

12. Model the task in case study of an embedded system for an Automatic Chocolate Vending Machine. [5]