Practical Memory Safety with *REST*

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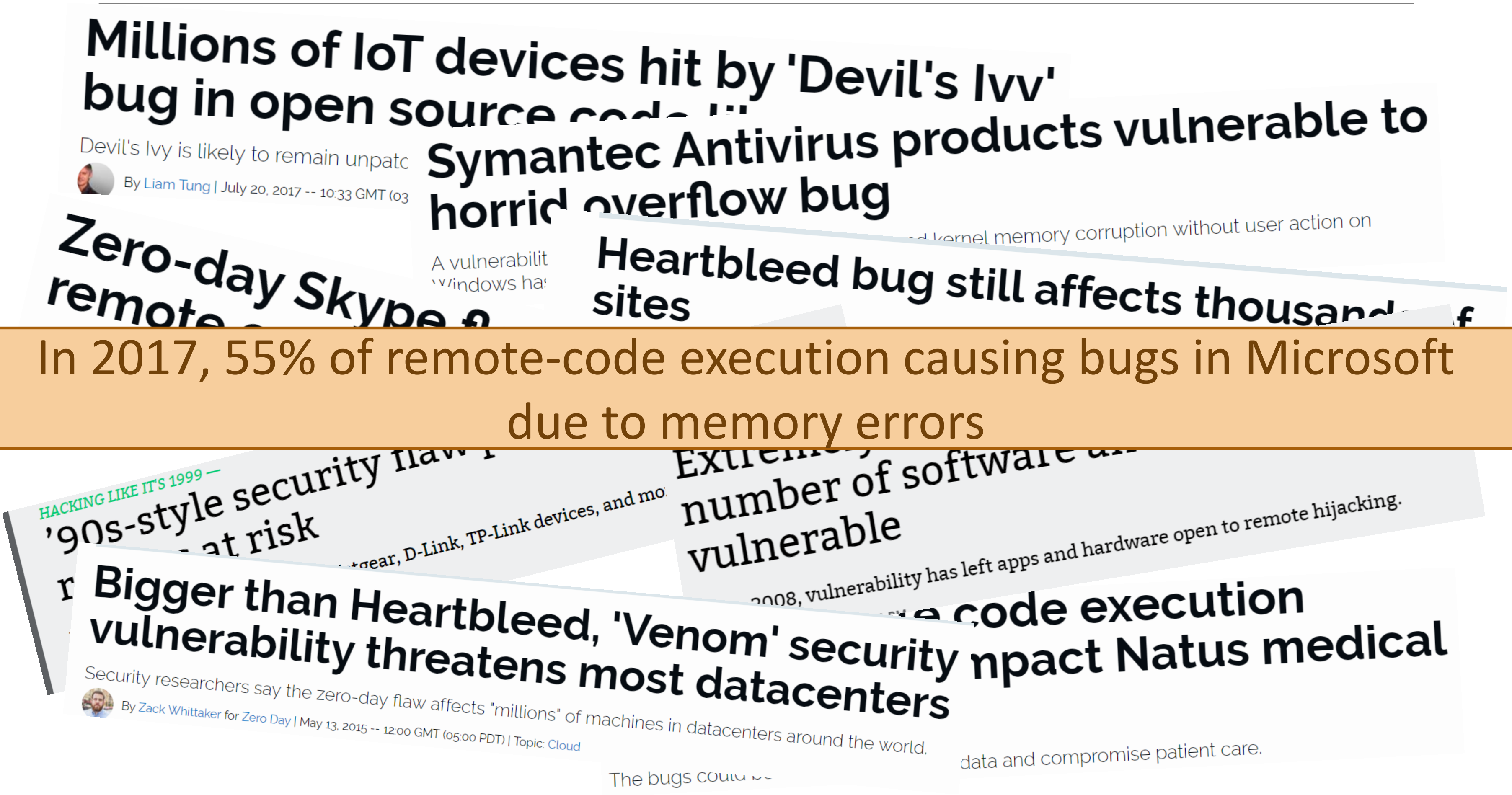
COLUMBIA UNIVERSITY

Is memory safety relevant?



Millions of IoT devices hit by 'Devil's Ivy' bug in open source code li

Devil's Ivy is likely to remain unpatc

By Liam Tung | July 20, 2017 -- 10:33 GMT (03

Symantec Antivirus products vulnerable to horrid overflow bug

A vulnerabilit Windows has

kernel memory corruption without user action on

Zero-day Skype f remote c

Heartbleed bug still affects thousands of sites

In 2017, 55% of remote-code execution causing bugs in Microsoft due to memory errors

HACKING LIKE IT'S 1999 —

'90s-style security flaw p at risk

tgear, D-Link, TP-Link devices, and mo

Extremely number of software an vulnerable

2008, vulnerability has left apps and hardware open to remote hijacking.

Bigger than Heartbleed, 'Venom' security vulnerability threatens most datacenters

Security researchers say the zero-day flaw affects "millions" of machines in datacenters around the world.

By Zack Whittaker for Zero Day | May 13, 2015 -- 12:00 GMT (05:00 PDT) | Topic: Cloud

code execution npact Natus medical

data and compromise patient care.

The bugs could be

Is memory safety relevant?

Yes!

Practical memory safety

Presenting…

Random Embedded Security Tokens or *REST*

Core H/W primitive: Insert known 64B random value (*token*) in program and detect accesses to them.

Practical memory safety

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char *buf = malloc(BUF_LEN);
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for (i=0; i<out_of_bounds; i++)
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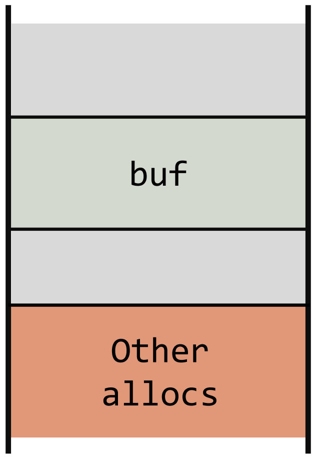

Heap

Practical memory safety

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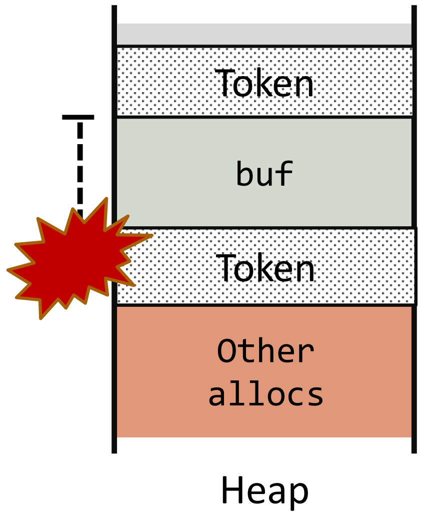


Practical memory safety

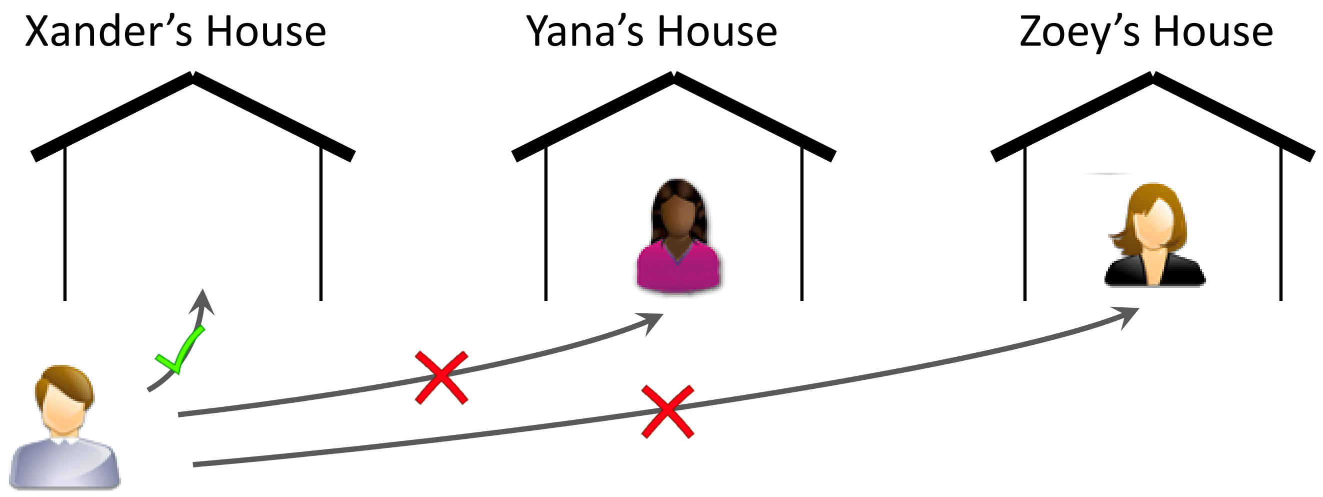
Presenting…

Random Embedded Security Tokens or *REST*

Core H/W primitive: Insert known 64B random value (*token*) in program and detect accesses to them.

- Trivial hardware implementation
- Software framework based on *AddressSanitizer*
- Provides heap safety for legacy binaries

Background: Spatial Memory Safety



Background: Spatial Memory Safety

```
char *ptr_buf = malloc(BUF_LEN);
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ptr_buf[in_bounds] = X;
…
ptr_buf[out_of_bounds] = Y;
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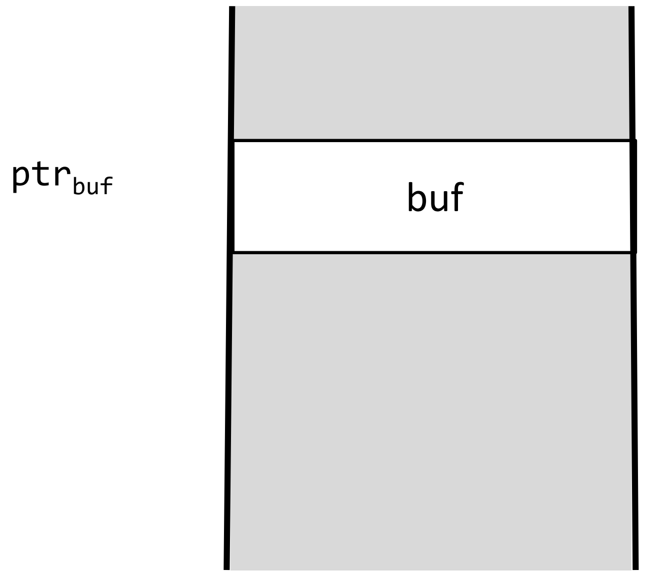

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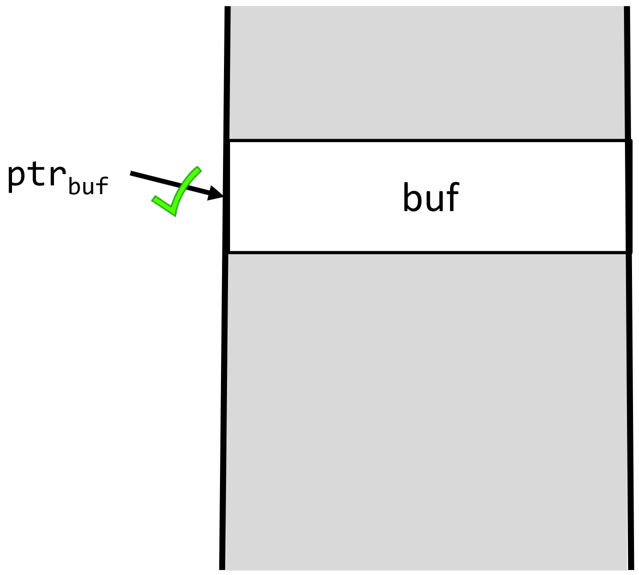

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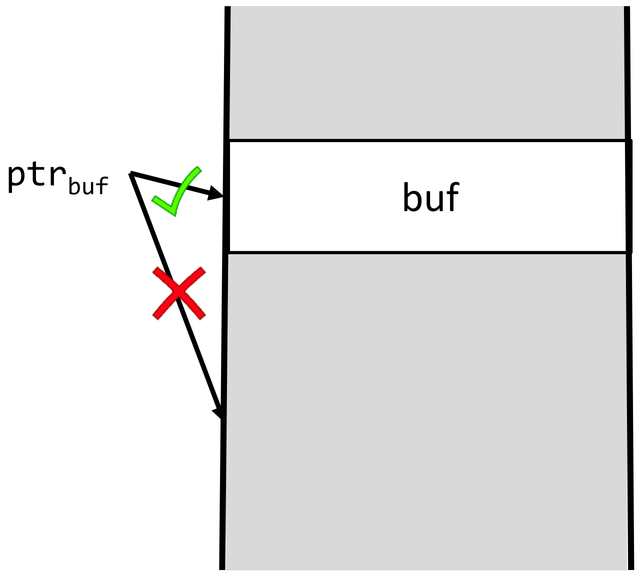
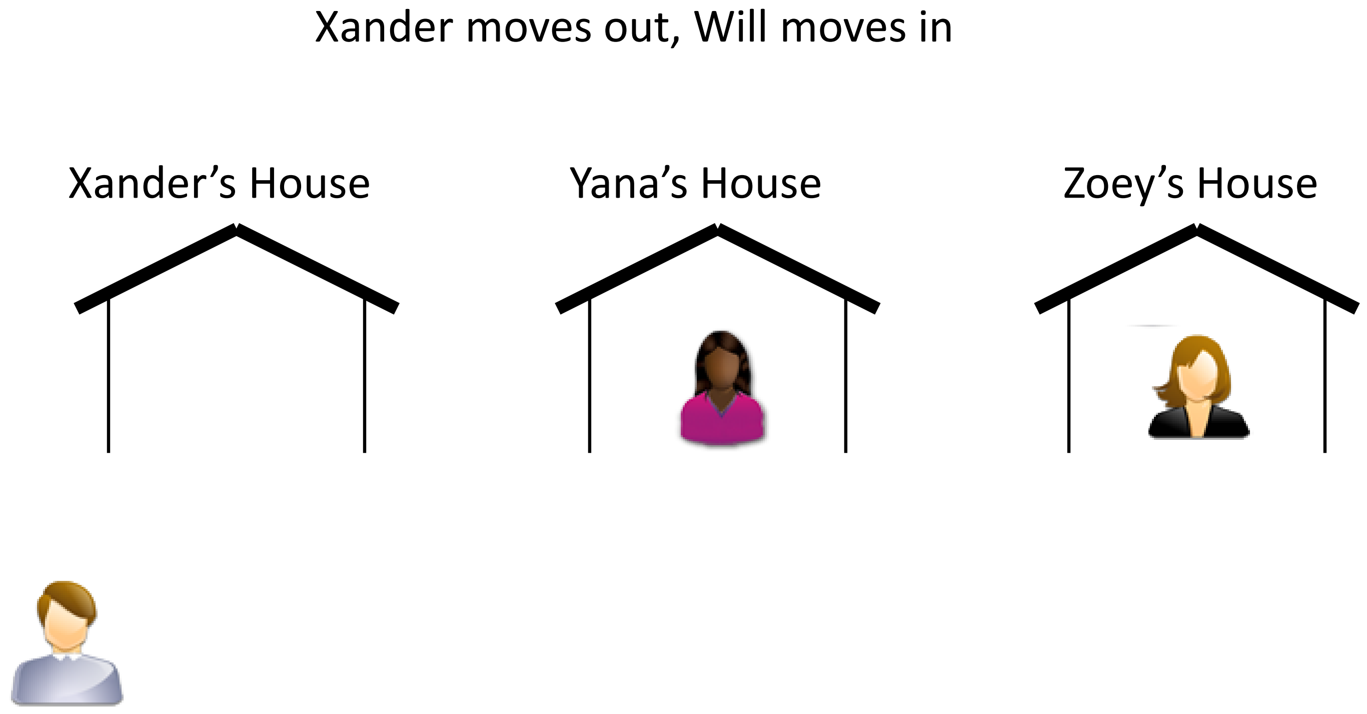


Background: Temporal Memory Safety



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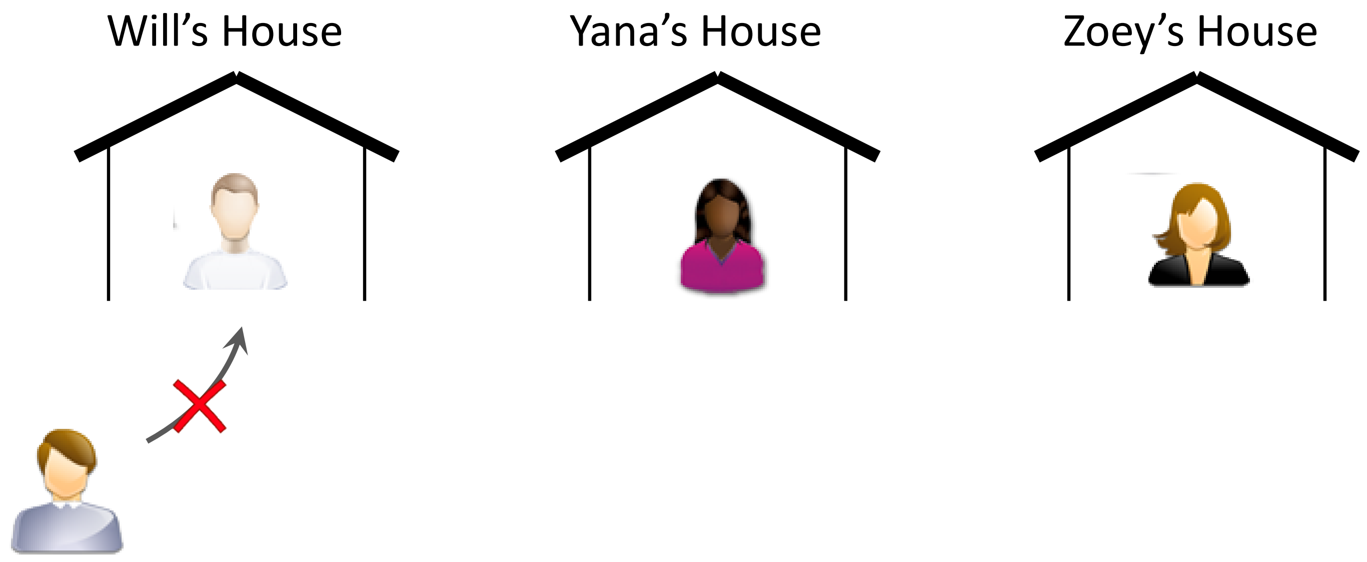
Xander moves out, Will moves in



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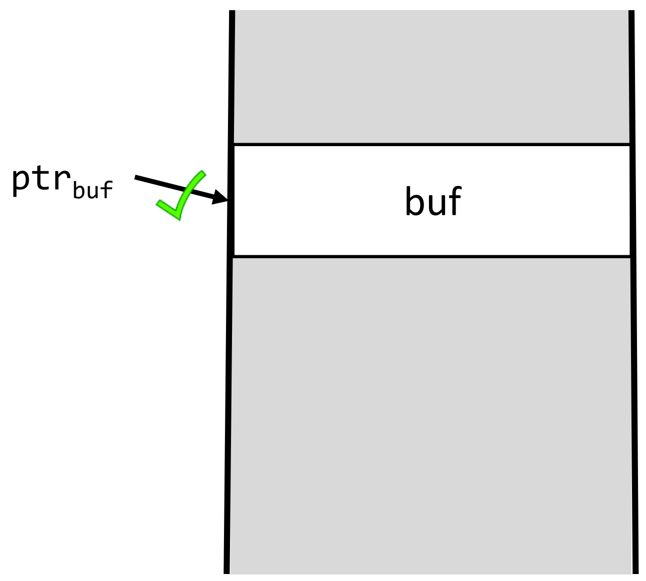

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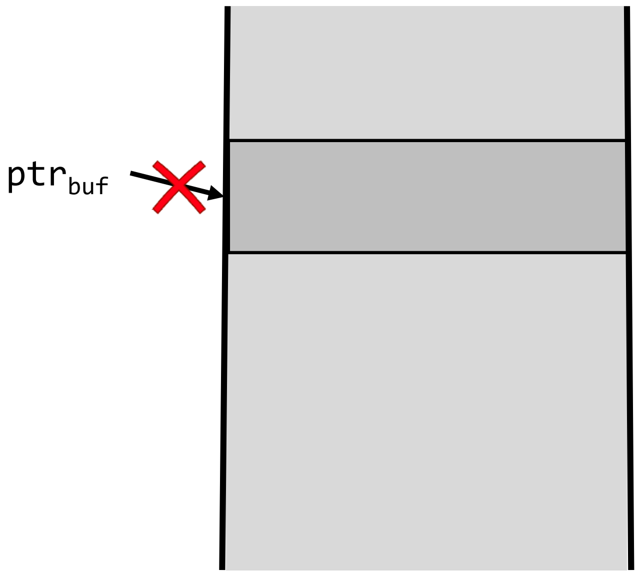

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Mainly categorizable into 2 types.

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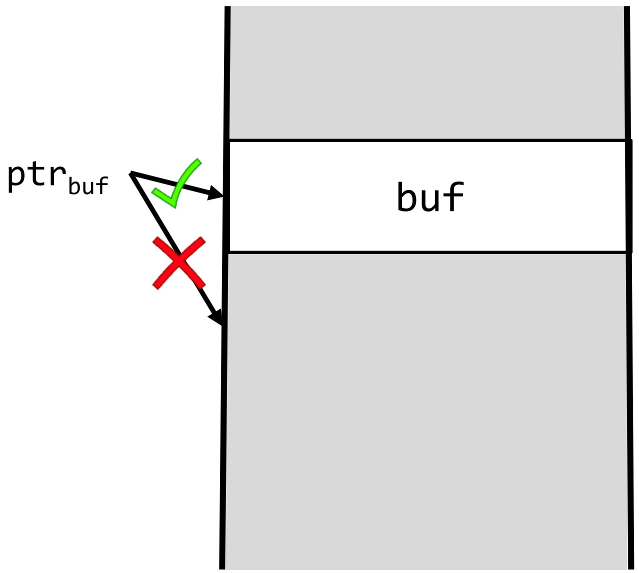
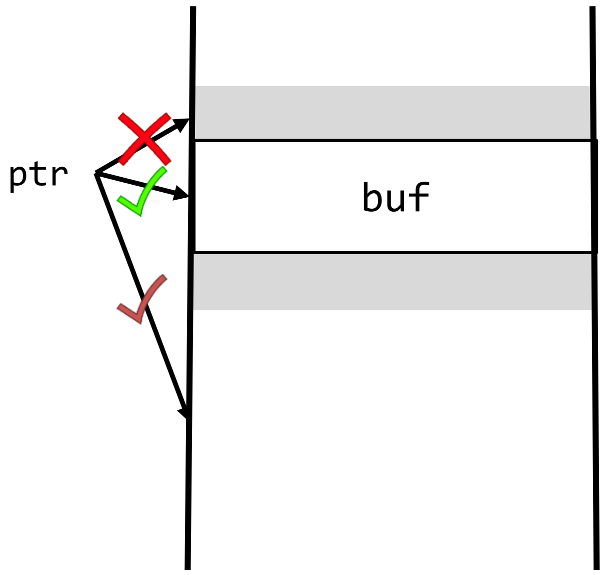
- **Whitelisting:** Pointer based
  + Good coverage
  + Temporal safety (for some)
  - Performance overhead
  - Implementation overhead
  - Imprecise



Previous H/W Solutions

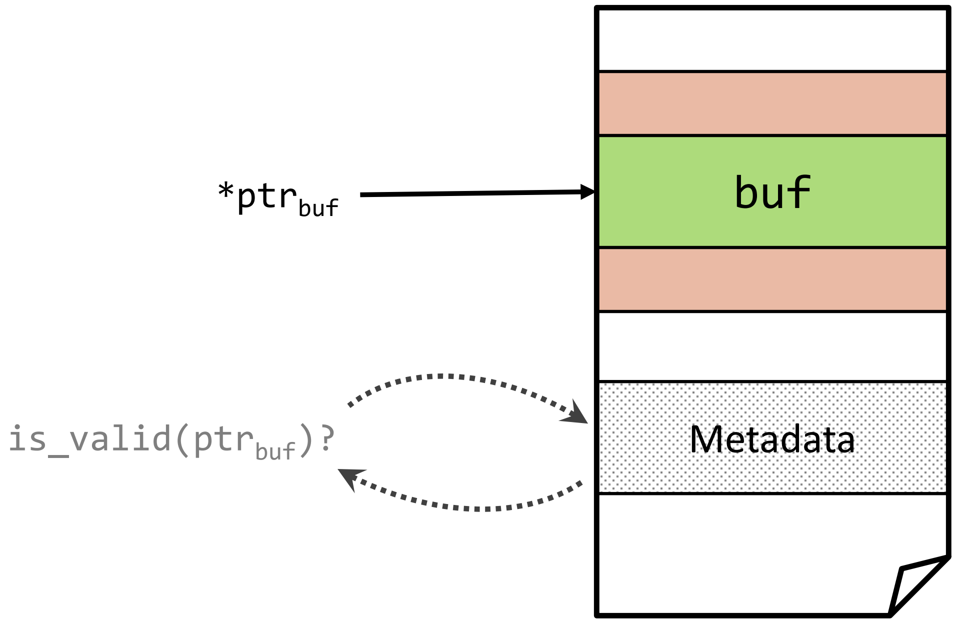
Mainly categorizable into 2 types.

- **Whitelisting:** Pointer based
  - + Good coverage
  - + Temporal safety (for some)
  - - Performance overhead
  - - Implementation overhead
  - - Imprecise
- **Blacklisting:** Location based
  - + Fast
  - - Weaker coverage (has false negatives)
  - - Implementation overhead
  - - No temporal protection



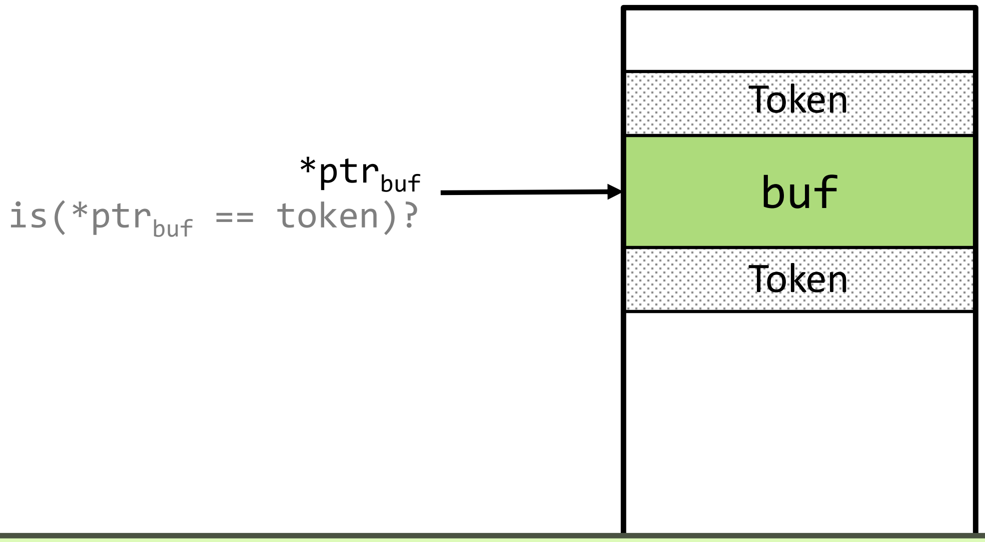
Previous H/W Solutions

Tag-based



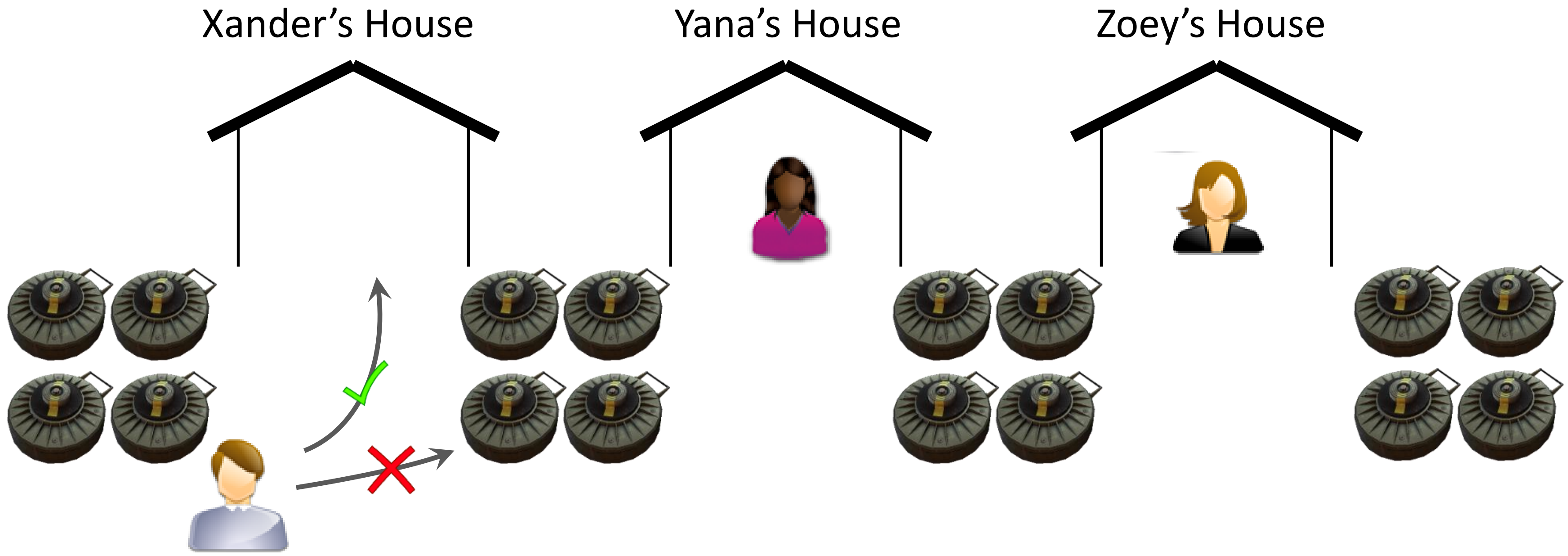
REST: Primitive Overview

Content-based blacklisting

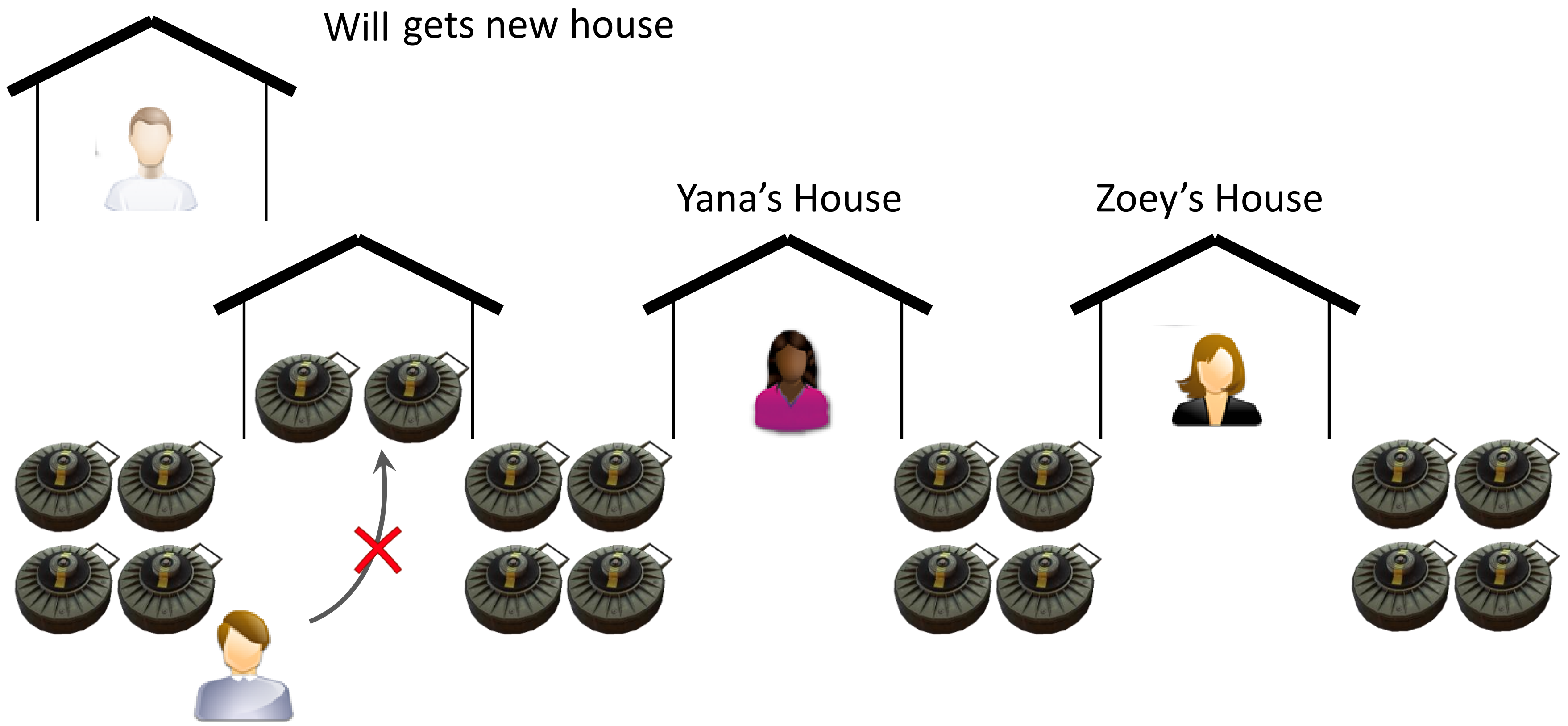


REST primitive has trivial complexity, overhead

REST: Spatial Memory Safety



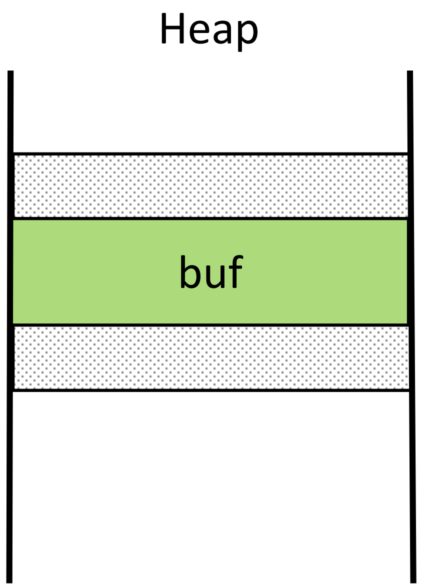
REST: Temporal Memory Safety



REST Software

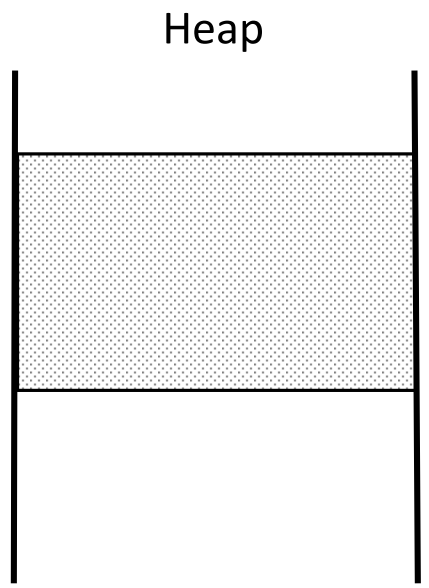
Heap Safety

- Allocate and bookend region, `malloc` to program



Heap Safety

- Allocate and bookend region, `malloc` to program
- REST'ize at `free`
- Do not reallocate region until heap sufficiently consumed



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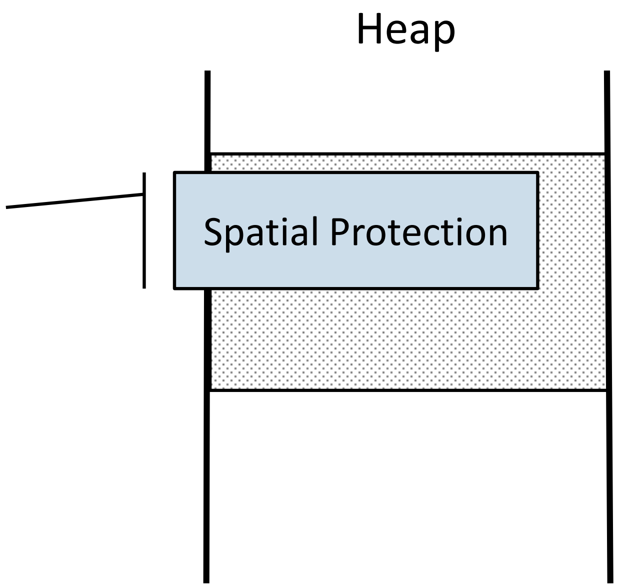

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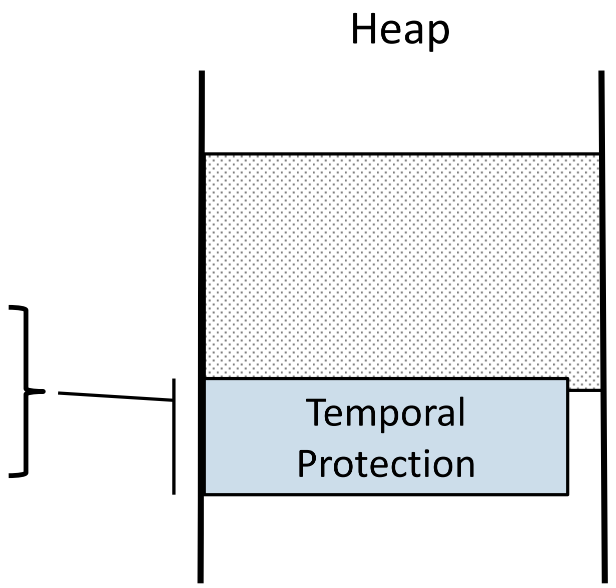

Can be enabled for legacy binaries

Stack Safety

```
void foo() {
    char buf[64];
    …
    return;
}
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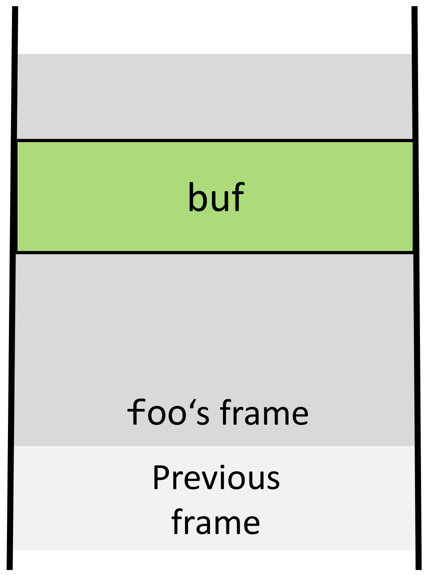

Stack Safety

```
void foo() {
    char rz1[64];
    char buf[64];
    char rz2[64];
    arm(rz1);
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    disarm(rz1);
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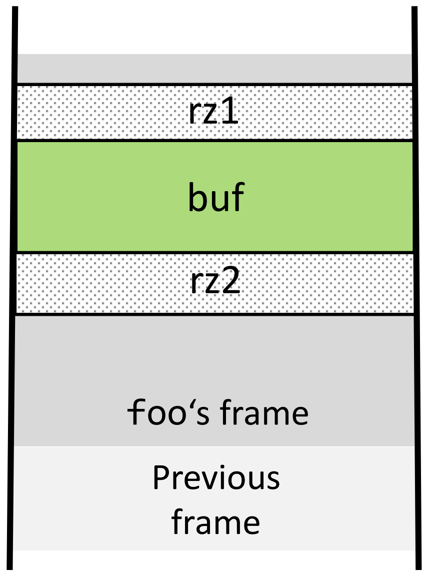

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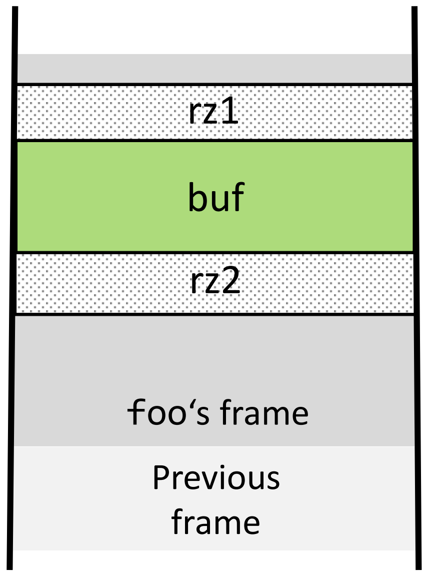

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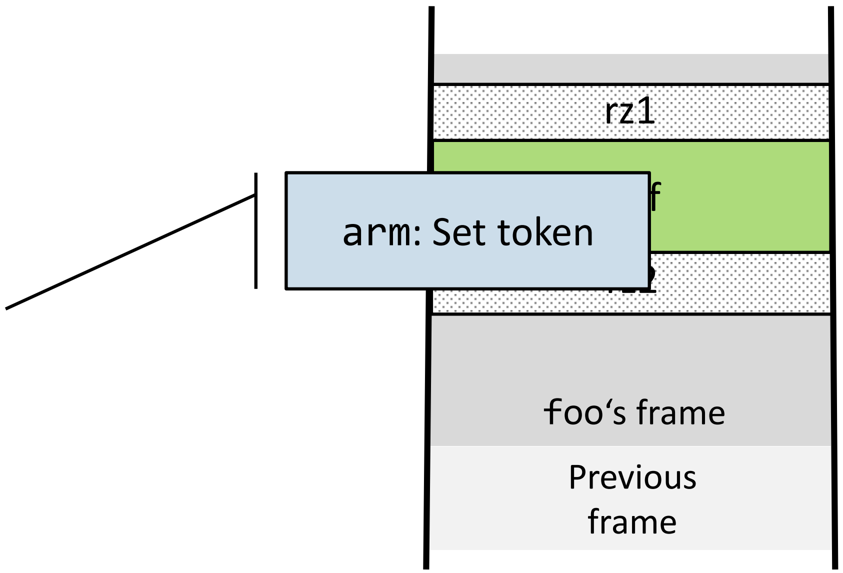

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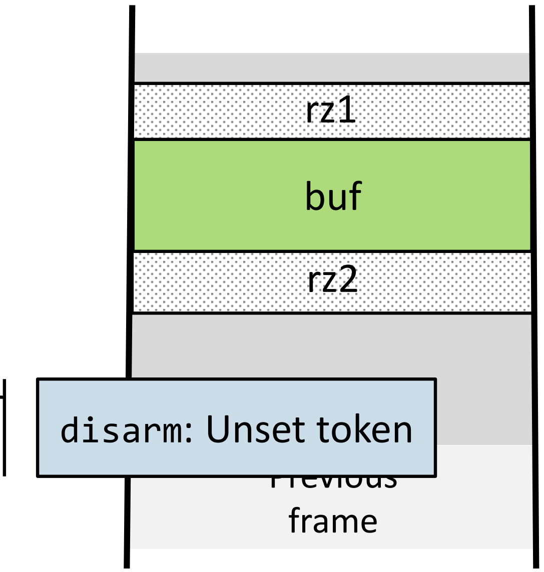

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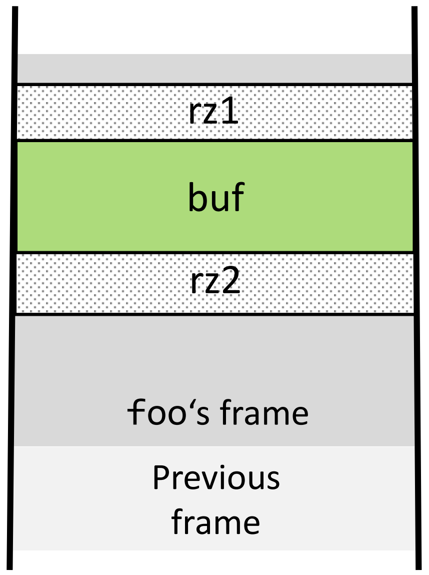
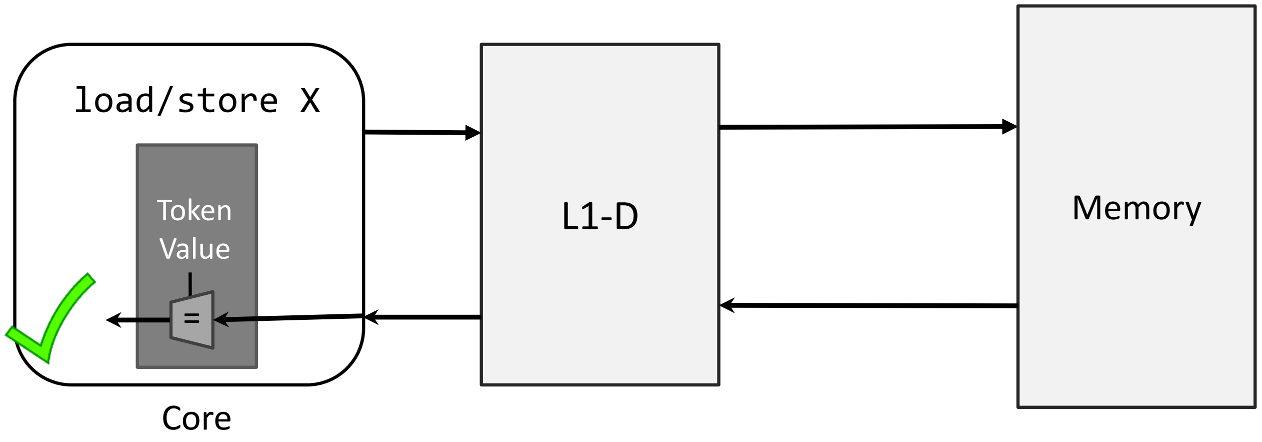


Requires recompilation with *REST* plugin

REST Hardware

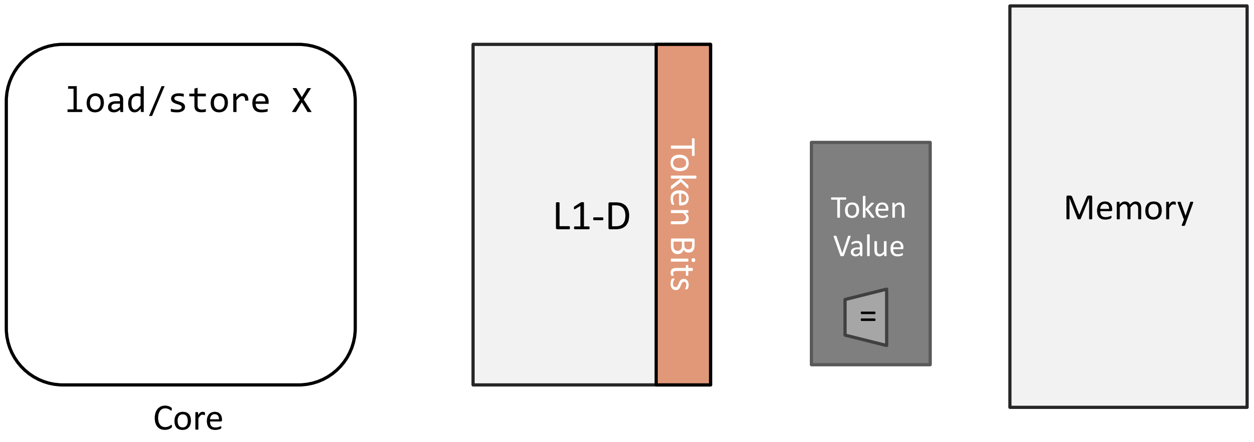
Naïve Design

Every store involves an extra load → Complicated and expensive

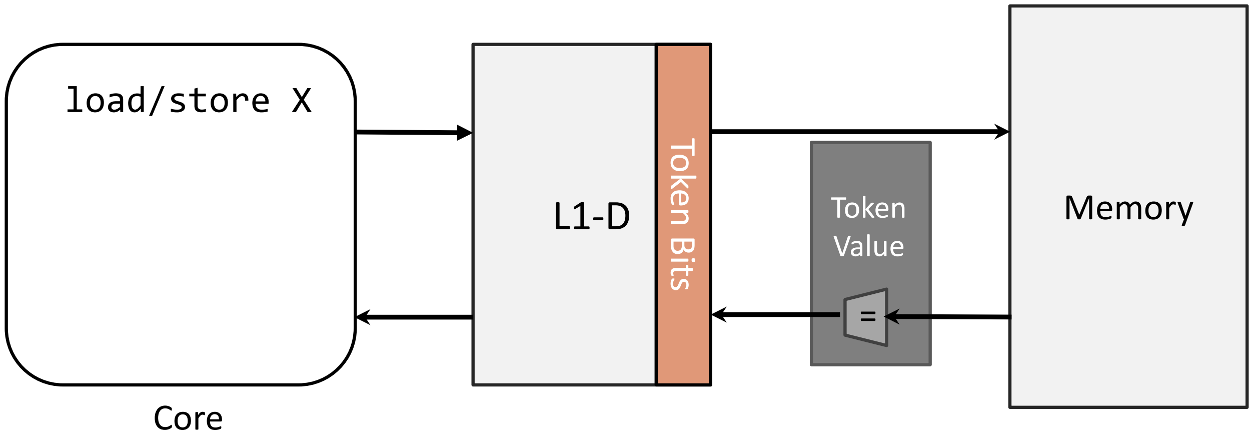


Cache Modifications

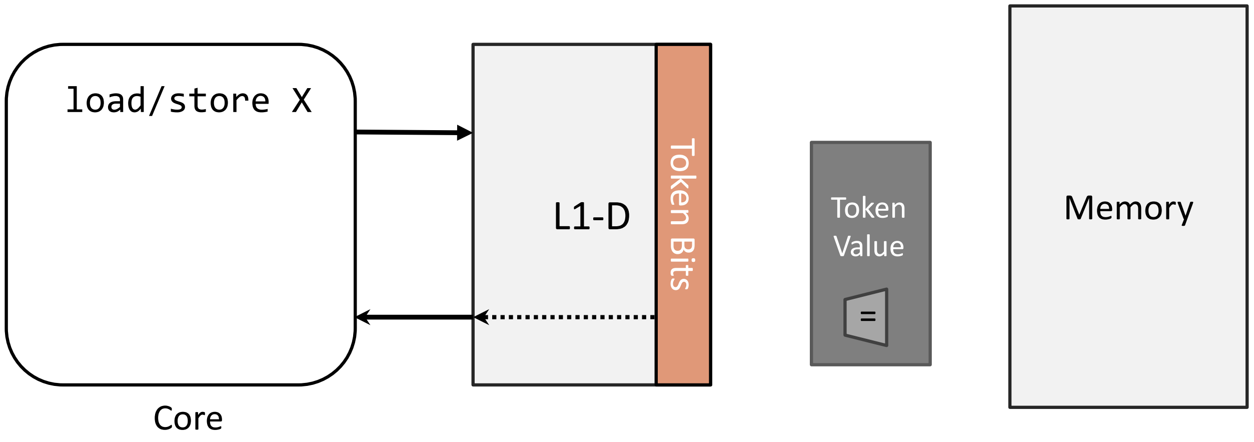
Comparator at L1-D mem interface + 1b per L1-D line



Cache Miss

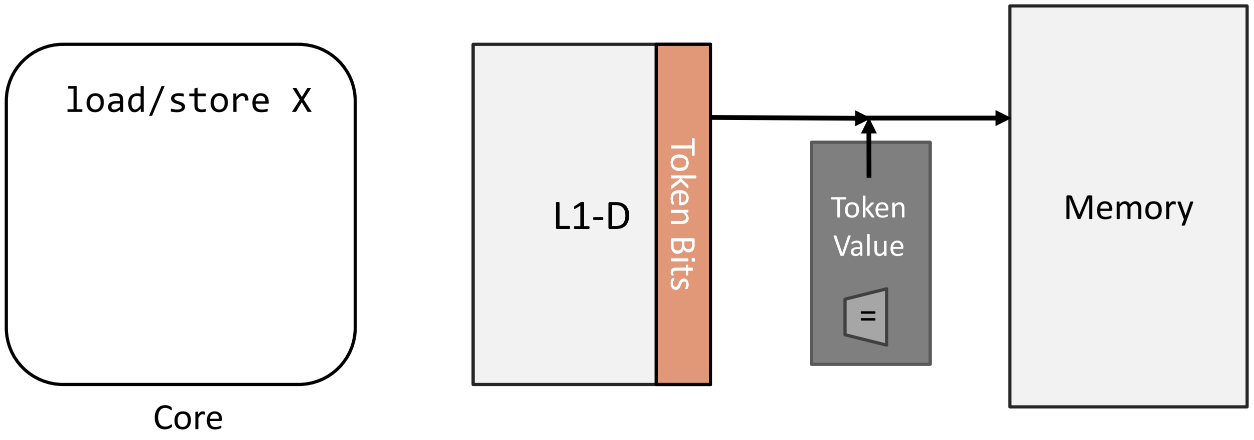


Cache Hit



Cache Eviction

Armed outgoing line filled with token value



What about the core?

TODO: Have to support arms and disarms

- 512b writes
- Special semantics: can only touch token with `disarm`

LSQ design concerns:

- Forwarding would break semantics
- 512b data entries
- How to match unaligned token access?

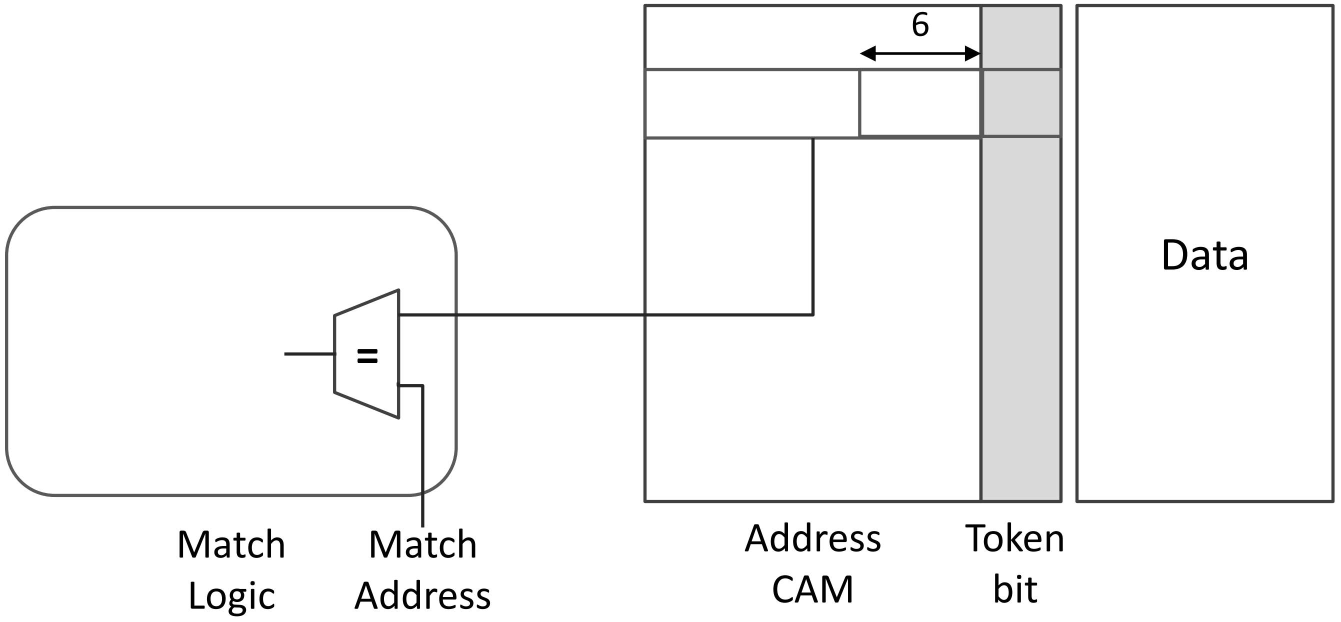
Load-Store Queue

- Forwarding breaks semantics
- 512b data entries
- Detecting unaligned token access

Add 1b tag

Only update token bit

Split regular match logic



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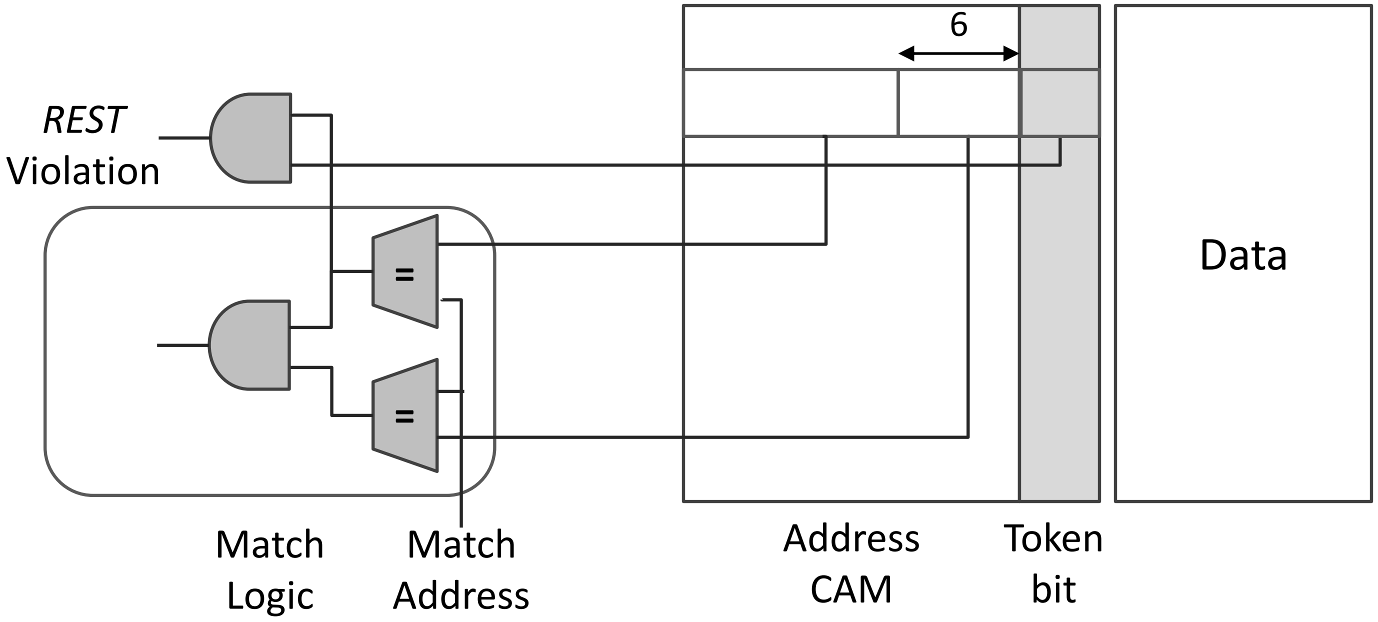
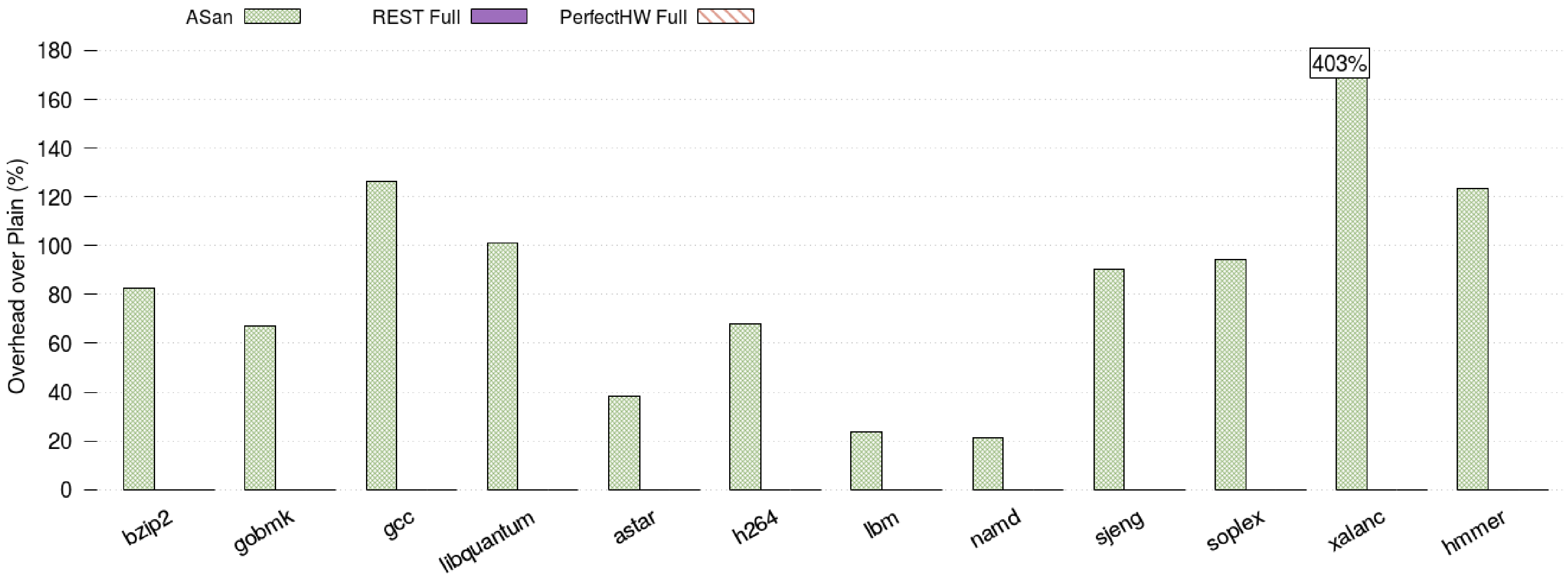


REST Overhead

REST Performance



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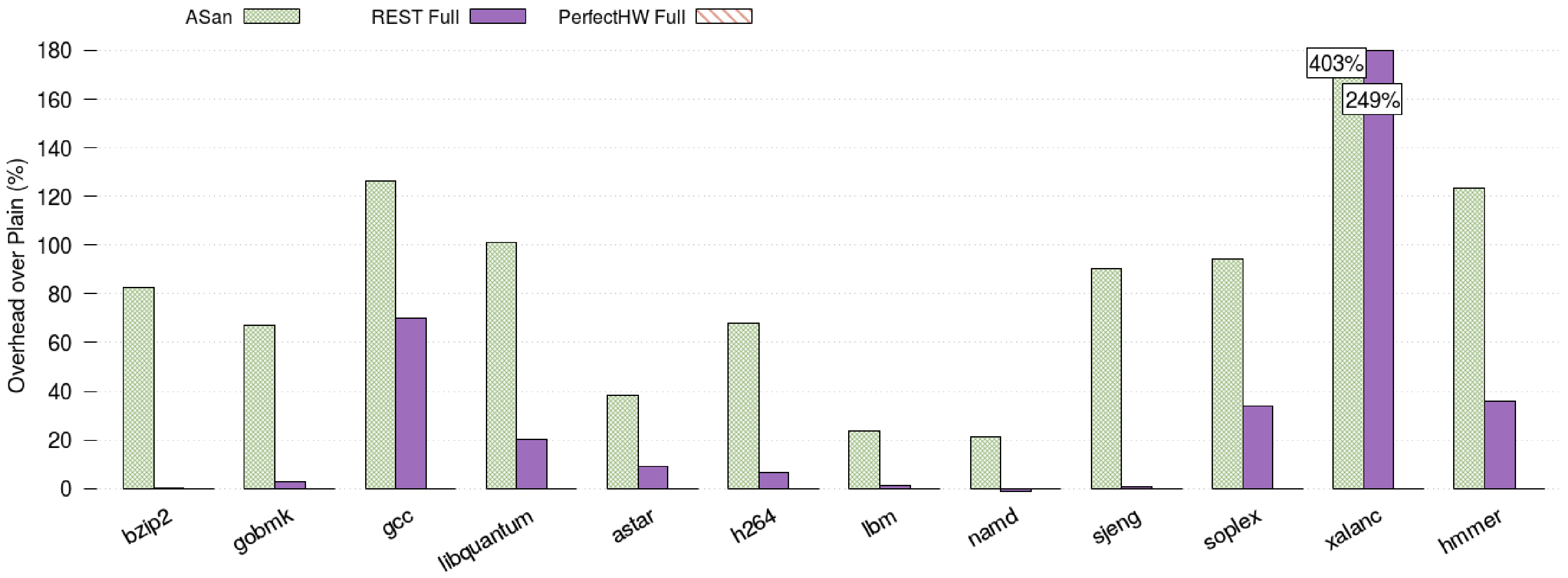

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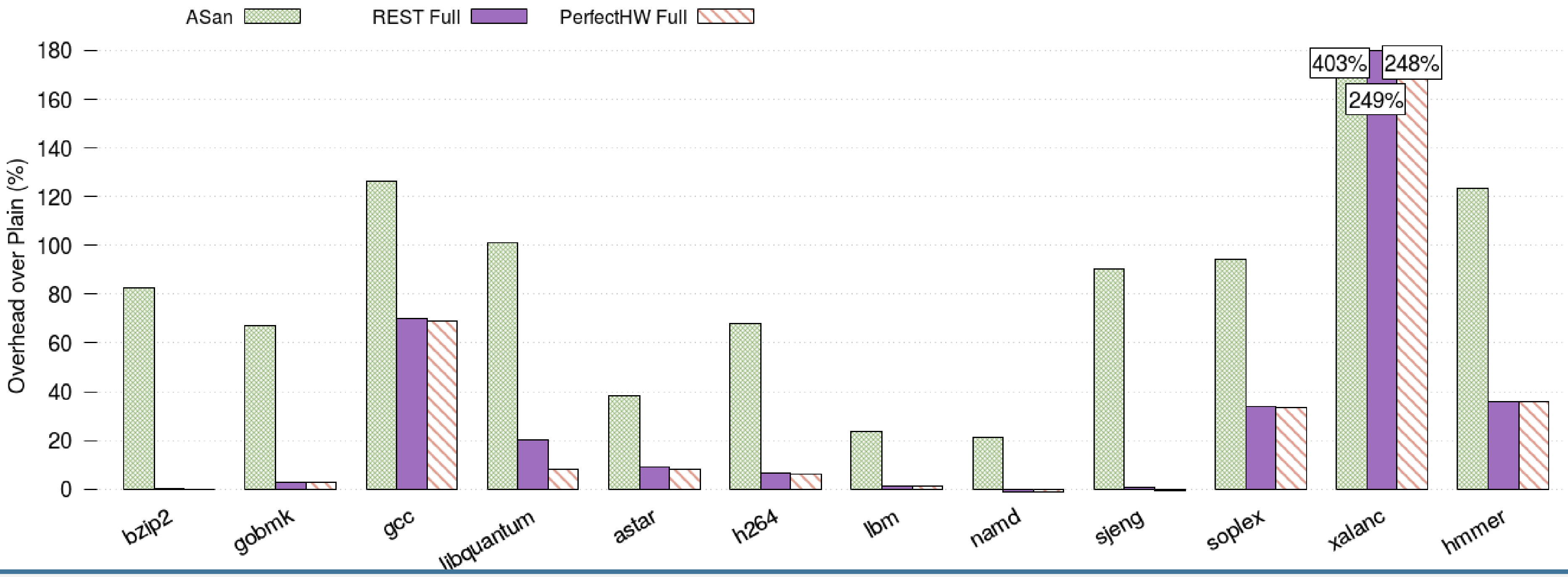

REST primitive overhead near-zero.

Software overhead mostly from allocator.

To conclude…

REST: Hardware/software mechanism to detect common memory safety errors

- Low overhead, low complexity hardware implementation
- Heap safety for legacy binaries

22-90% faster than comparable software solution on SPEC CPU

Questions?