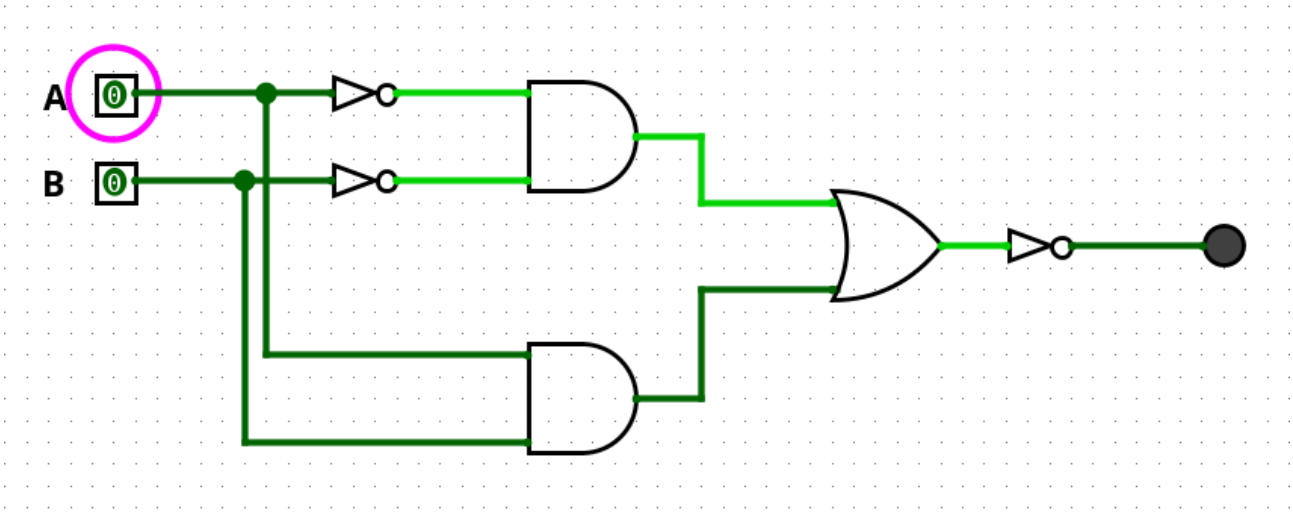
Name: Md. Abdullah Al Mamun
Roll: 2003028

Question 1:



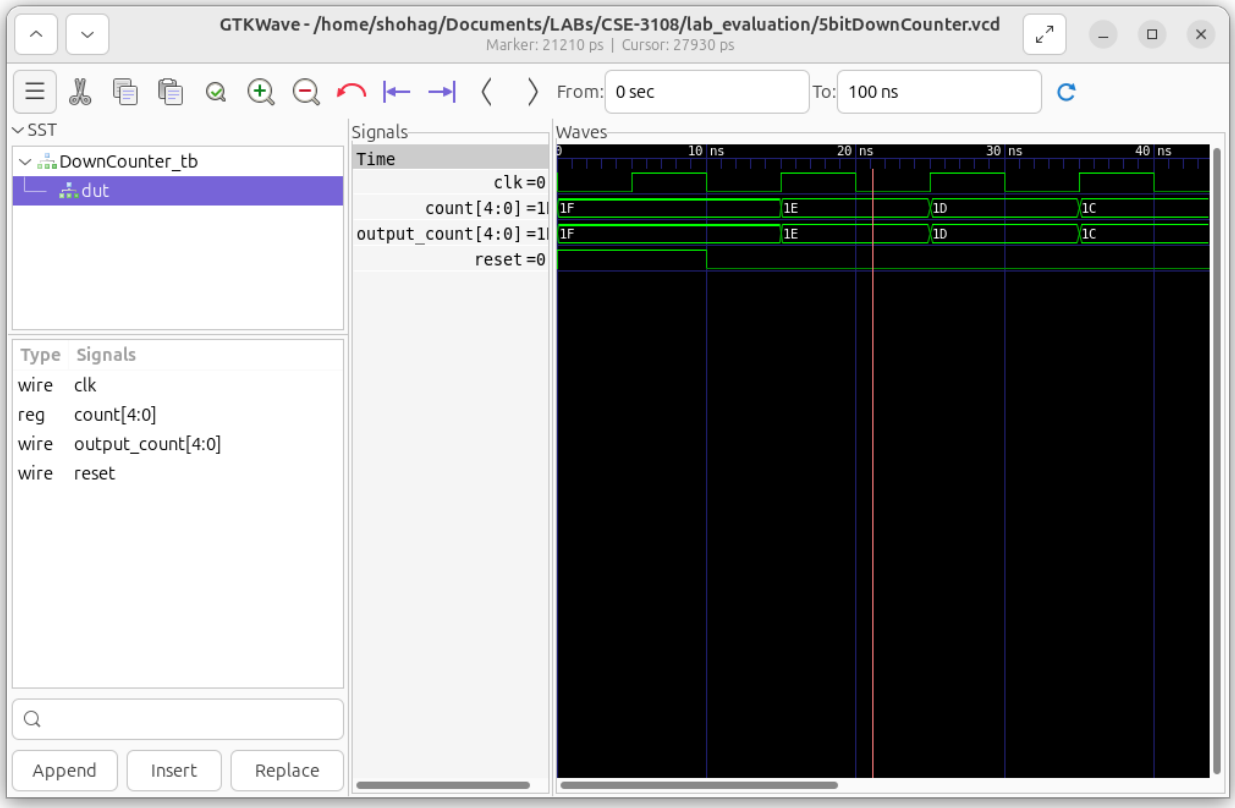
Question 2:

Module:

```
module DownCounter ( input wire clk, input wire reset, output wire
[4:0] output_count); reg [4:0] count;

always @(posedge clk or posedge reset) begin if (reset) count <=
5'b11111; else count <= count - 1; end

assign output_count = count;

endmodule
```

Test Bench:

```
`timescale 1ns/1ps

module DownCounter_tb; reg clk; reg reset; wire [4:0] count;

DownCounter dut(clk, reset, count);

initial begin $dumpfile("5bitDownCounter.vcd"); $dumpvars(0, DownCounter_tb);

clk = 0; reset = 1; #10 reset = 0; end

initial begin $monitor("count = %b", count); end

always #5 clk = ~clk;

initial begin #100 $finish; end

endmodule
```



Question 3:

```
mov R1, #0 ;mov R2, #10 ;
while CMP R1, R2 ;
 BEQ done ;
 ADD R1, R1, #5 ;
 B while ;
done STOP ;end
```