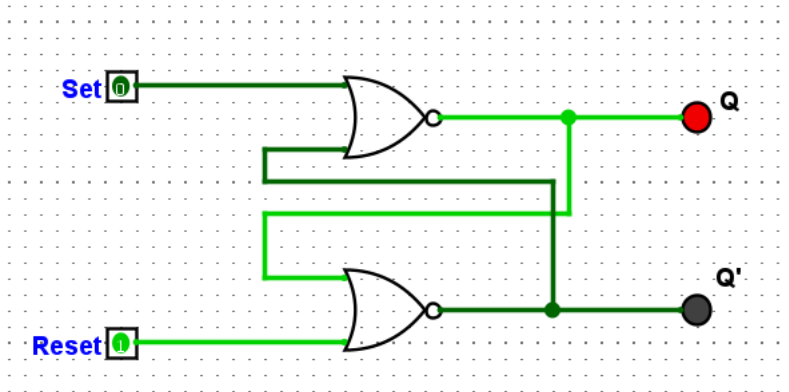


1. RS Flip-flop

Set the pins in the following order and record the states for Q and Q'

Set	Reset	Q	Q'
1	0	0	1
1	1	0	0
0	1	1	0
1	1	0	0



Describe in a sentence, the behaviour of the circuit when one of the inputs is 1 (but not both) and why this is useful for digital circuit design.

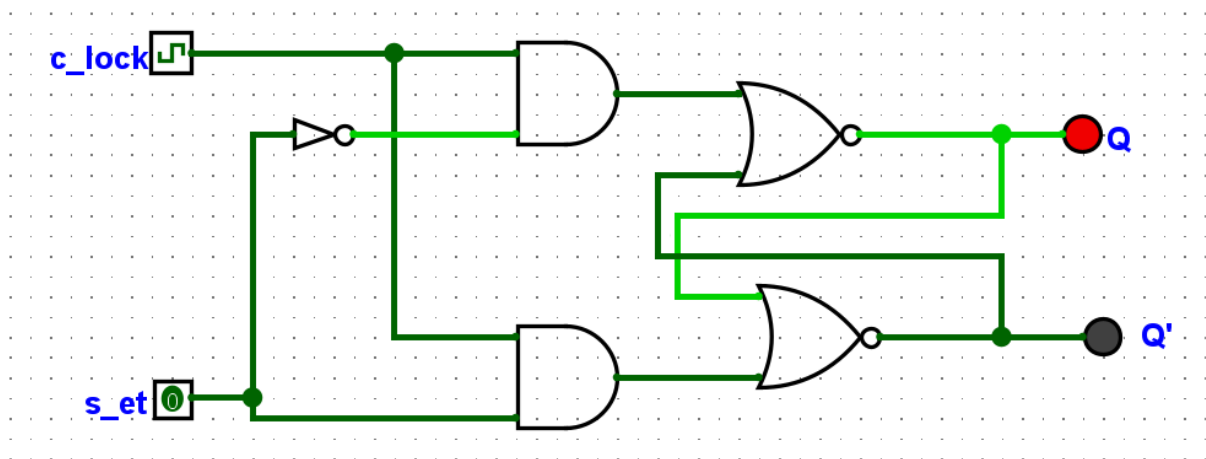
- When one of the inputs is 1, the opposite output will also be one and the following output will be 0. The opposite output will always be in the same stage as the inputs (for example when S is 1 and Reset is 0, the output will be the opposite as Q will be 0 and Q' will be. Vice versa).
- Unless the circuit is invalid or "reset", the circuit will also store 1 bit.

What do you notice about the two times you set both inputs to 0. Briefly explain what is happening here and why this is an issue for digital circuit design?

- When two inputs are set to 0 simultaneously it enters an undefined state where both outputs are 0 and 1 at the same time. This is problematic for the circuit and refer to as a "invalid" state.

2. D Flip flop

Clock	Pin	Q	Q'
0	0	0	1
0	1	0	1
1	0	1	0
1	1	1	0
0	1	1	0
0	0	1	0



Briefly explain the behaviour of a D Flip Flop and how it is useful for digital circuit design.

- When the clock pulse equal 1, the Q and Q' could be set using the set input (if the set input is 1, Q will be 1 and Q' will be 0 and vice versa). On the other hand, when the clock pulse equal 0, the states of Q and Q' is locked and can't be changed.
- This behaviour is useful for digital circuit design as it allowed synchronize controls, enabling precise timing control and avoiding "invalid" state.

What is the role of the clock? How does it impact the changing of state of Q and Q'?

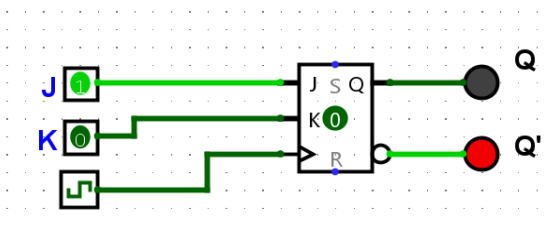
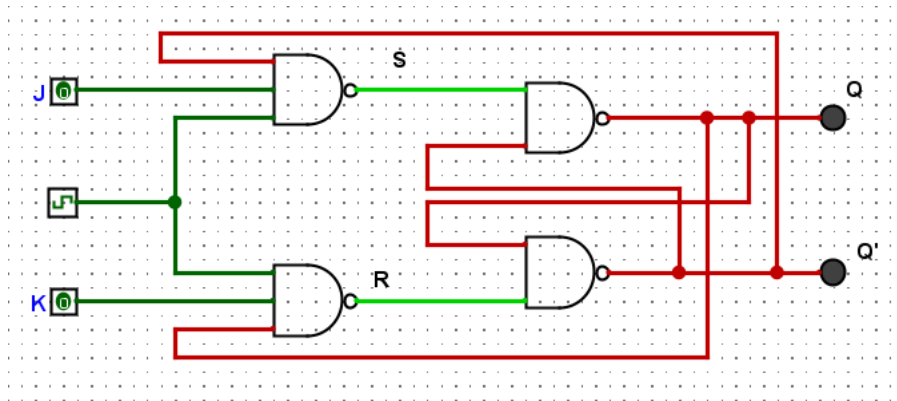
- The clock control when the input data is transferred and using to set the states of the outputs in Q and Q'.

Why is it generally preferred over the R-S Flip Flop?

- The D flip flop has a predictable output with precise timing and no "invalid state".

3. The J K flip flop.

J	K	Q (when clocked)	Q' (when clocked)
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	0



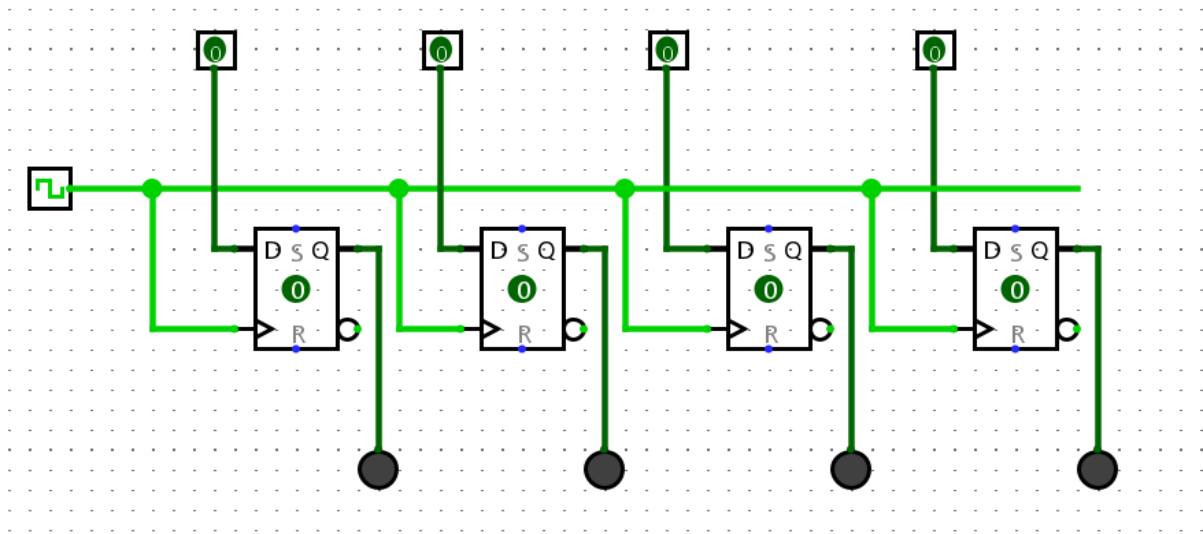
How can a J-K Flip Flop be made to behave like a D Flip Flop?

- Turn the J input to 1 and K input to 0, by times the clock pulse equal 1, the Q state is 1 and Q' is 0. The output will be stored that way.
 - On the other hand, turn the K input to 1 and J input to 0, by times the clock pulse equal 1, the Q state is 0 and Q' is 1. The output will be stored that way.
- ⇒ This behaviour is the same as the D flip flop.

How can a J-K Flop be made to behave like a toggle (T Flip Flop)?

- Turn both input J and K to 1, each times the clock pulse equal 1 enter the circuit, the output of Q and Q' will switch.
- ⇒ This behaviour is the same as the T flip flop.

4. Register



Use your register to fill out the following test schedule:

Ox	Input Bin	Output Binary
0	0000	0000
1	0001	0001
2	0010	0010
3	0011	0011
4	0100	0100
5	0101	0101
A	1010	1010
B	1011	1011
C	1100	1100
D	1101	1101
E	1110	1110
F	1111	1111