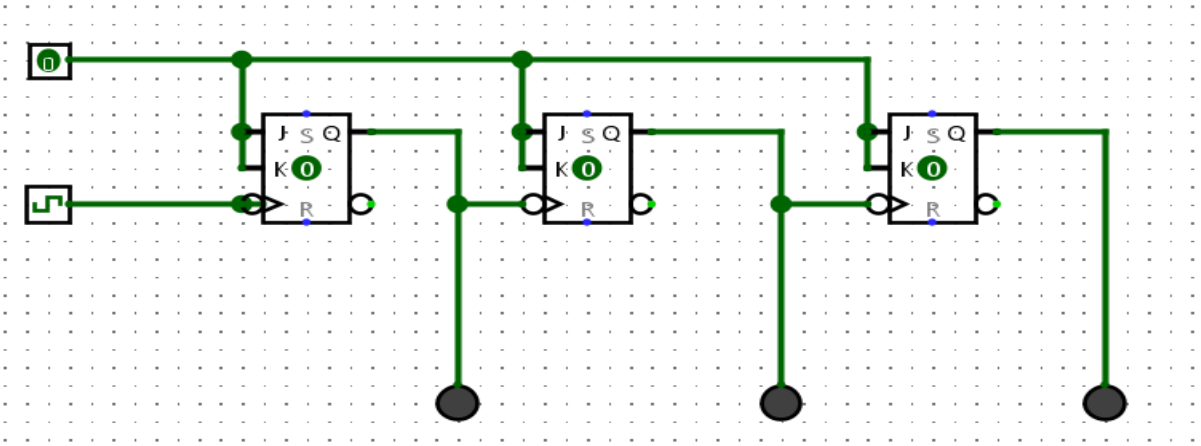
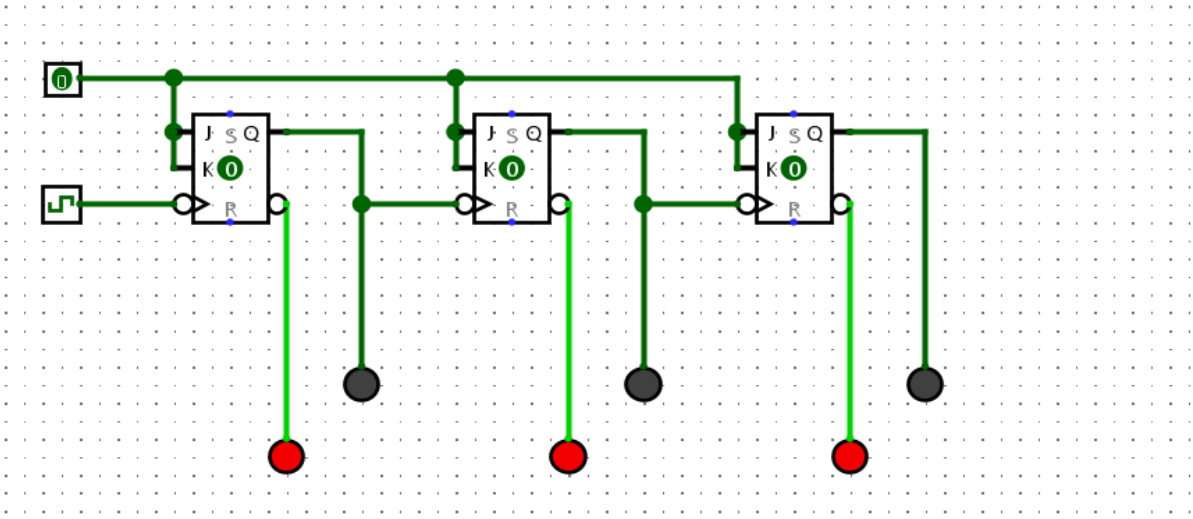
2. Use LEDs to show the output "Q" from each Flip Flop. For this to work, you will also need to set your JK Flip Flops to Trigger with the clock's Falling Edge instead of its Rising Edge (click on each FF and set this in the Attributes Pane).

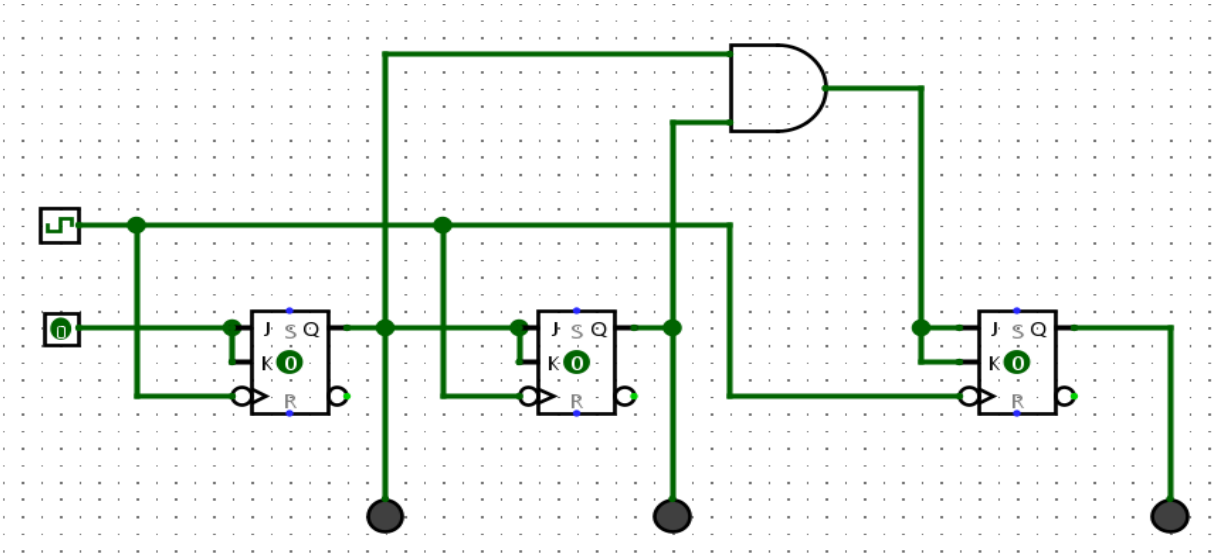


5. Now build a big-endian 3-bit "count down" counter, that counts from 111 to 000. Review the week 3 lecture slides to get some hints on this and discuss your plan with your lab demonstrator if you need to.

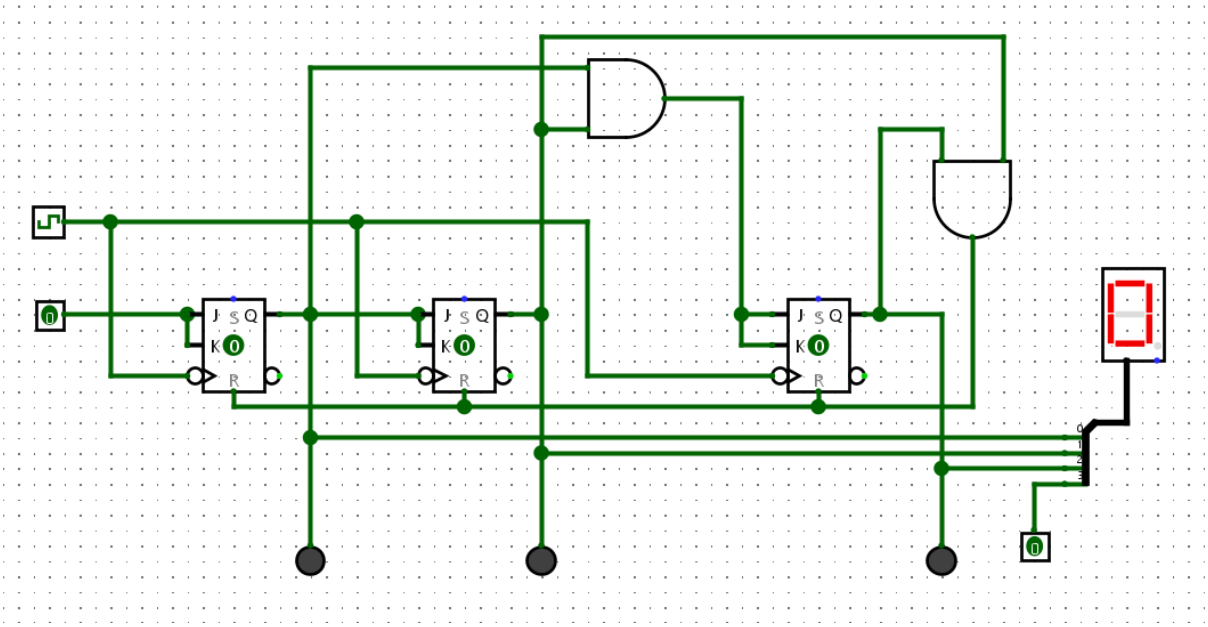
- There are many ways to make to make this count down including keeping the count of 2 the same and utilize the Q' of each flip flop or changing every flip flop states from Falling Edge to Rising Edge.



7. Take your original counter from Step 2 and modify it so it now counts from 0 to 111 using a common clock. That is, each flip flop receives a clock pulse at the same time. Review the lectures if you need to.

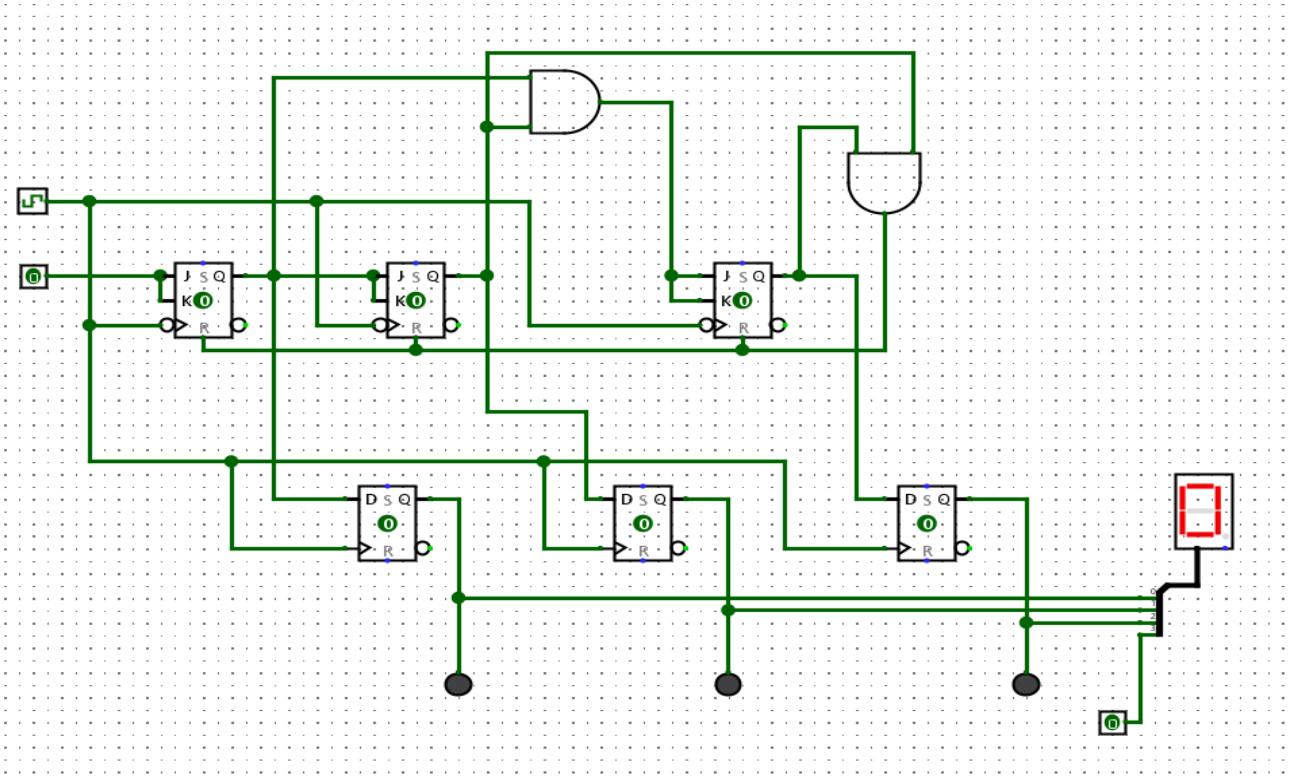


9. Now modify your clock from Step 7 so it counts from 0 to 5 (i.e, MOD 6), and then wraps around back to 0. Think about how you are going to detect the upper limit, and how you are then going to set things back to 0 when you reach 6 (110).



10. The circuit in Step 9 goes into a momentary illegal state (i.e, it displays the binary string 110 due to the delay between detection of the limit, and the eventual reset back to 0. In the lecture we discussed using D Flip Flops as a buffer, to hold the output state one extra clock pulse before showing (allowing time for any resetting to occur first).

10.1 Modify your counter so that it resets after 5 (101) back to 0 (000) without the momentary illegal state.



10.2. Why is handling such things important?

- Because such illegal states can affect the Data Integrity, glitches, and Circuit Reliability, long-term stability