מטרת המעבדה:

במעבדה זו, השתמשנו בתוכנות QUARTRUS ן MODELSIM על מנת לבצע סינתזה למודלים שיצרנו במעבדות קודמות. את המעבדה הרצנו על הבקר FPGA CYCLONE של כרטיס DE10.

במעבדה זו מימשנו שני מעבדים חשובים בתחום החומרה:

מעבד SINGLE CYCLE- מעבד אותו מימשנו תחילה כדי להוסיף את הפקודות הנדרשות.

מעבד PIPELINE- מעבד אותו מימשנו לאחר מימוש הsingle CYCLE, כדי לעבוד עם מעבד יעיל יותר.

כלומר במעבדה לבסוף מימשנו מעבר PIPELINE של MIPS היודע לבצע ISA בסיסית של פקודות אסמבלי.

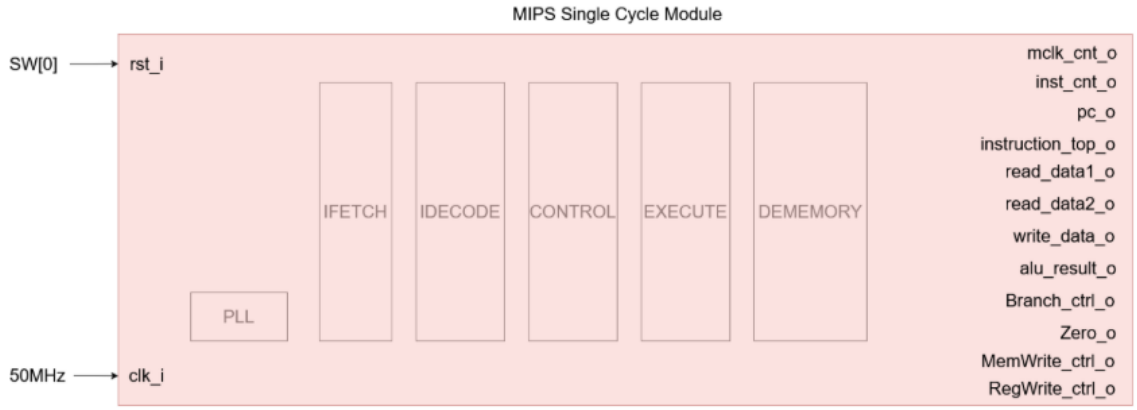


Figure 7: Single-cycle MIPS architecture top entity

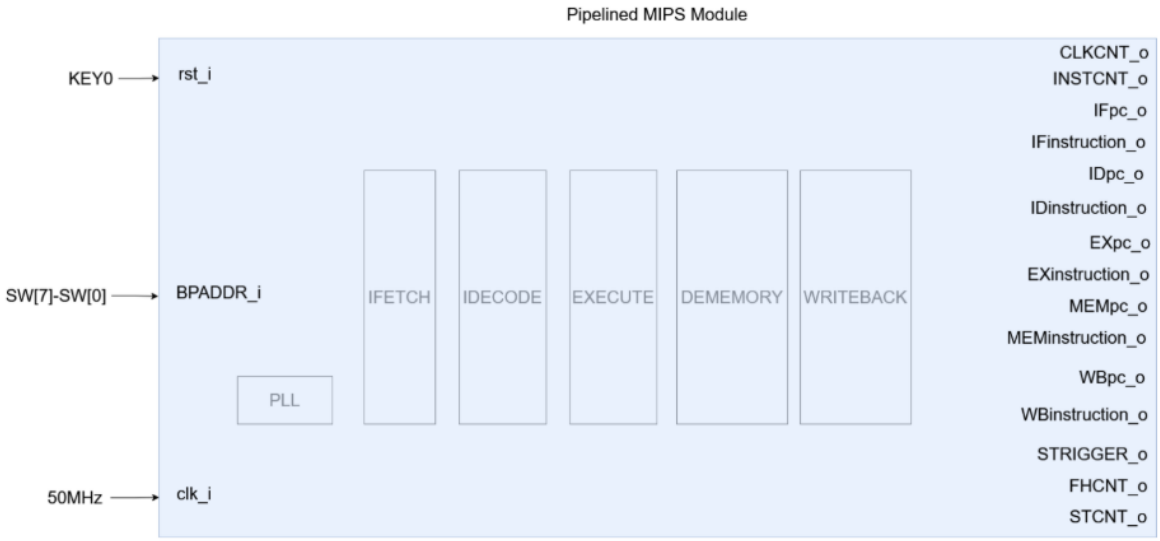
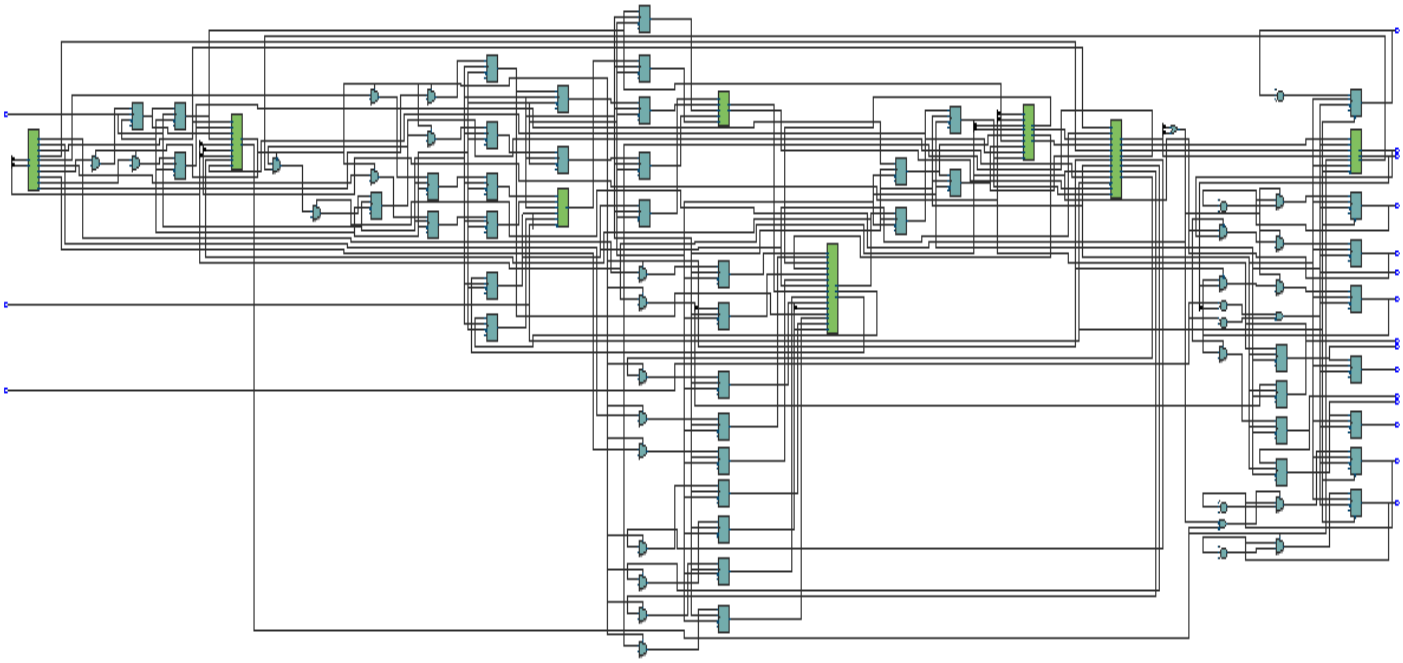


Figure 8: Pipelined MIPS architecture top entity

המעבד :

כעת, נסביר על המערכת שמימשנו ועל המודולים השונים בה.

הRTL של המערכת שלנו :



- INPUT : BPADDER[0:7], RST,CLK

BPADDER- נכנס אליו כתובת הBREAK POINT בהתאם לאינפוט שבמתגים 0-7.

- OUTPUT : CLKCNT, INSTCNT, IFPC, IFINSTRUCTION, IDPC, IDINSTRUCTION, EXPC, EXINSTRUCTION, MEMPC, MEMINSTRUCTION, WBPC, WBINSTRUCTION, STRIGGER, FHCNT, STCNT.

FHCNT- מונה הסופר כמה פעמים בוצעה פקודת FLUSH.

CLKCNT- מונה הסופר כמה מחזורי שעון עברו.

STCNT- מונה הסופר כמה פעמים בוצעה פקודת STALL.

הסיבה בגינה יש לכל שלב במעבד הPIPELINE 5 שלבים גם את מוצא ה PC וגם את מוצא ה INSTRUCTION הינה כדי שנוכל לראות באופן יפה את מעבר הפקודות בPIPELINE בין הרגיסטרים החוצצים את המעבד.

מימוש ראשוני אותו התבקשנו לבצע במעבדה :

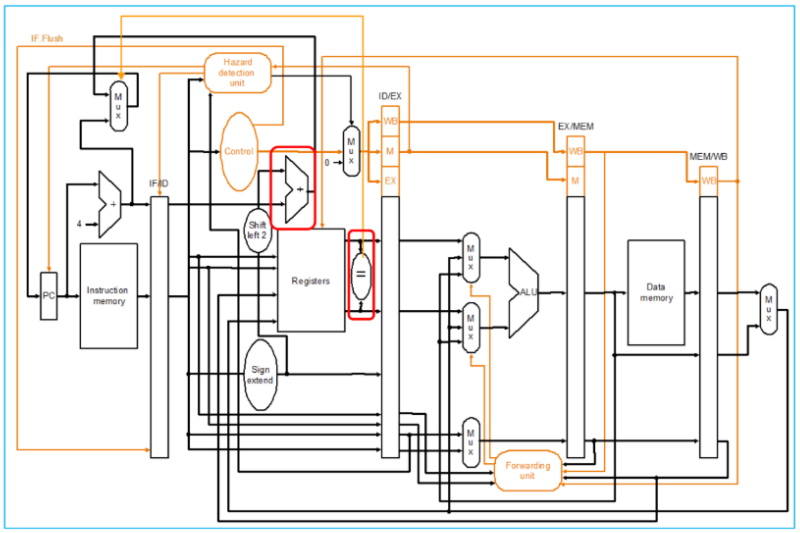


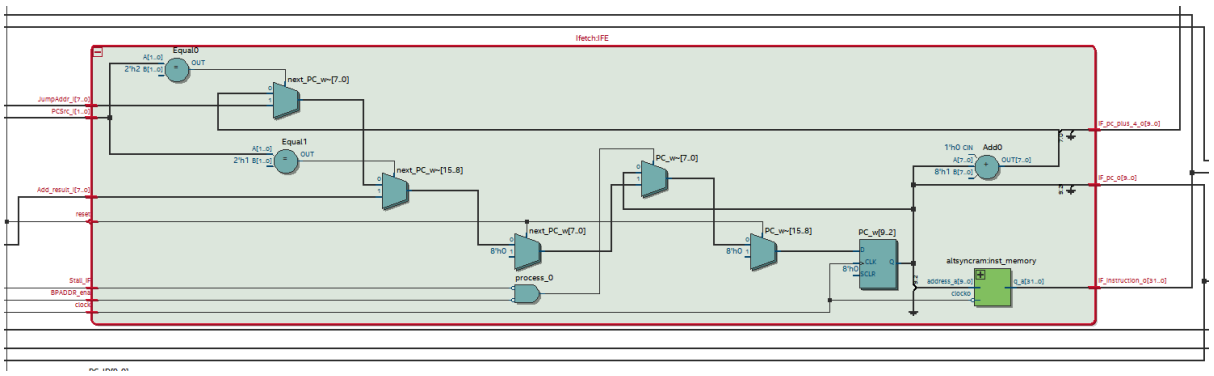
Figure 6: Five-stage pipelined MIPS architecture with forwarding and single delay slot support

השלבים במעבד :

שלב ה FETCH :

בשלב זה נרצה להביא פקודה בכתובת ה PC מהזיכרון ITCM. הPC מתעדכן ל 3 מצבים הנבחרים על ידי אות בקרה PCSEL, והמצבים הם : 4+PC, PC מפקודת BRANCH ו PC מפקודת JUMP.

שרטוט הRTL :



מודול DECODE :

בשלב זה נרצה לפענח את הפקודה המגיעה מה FETCH. את הפקודה אנחנו נפרק לפי 3 תבניות הנלמדו בחומר התיאורטי של הקורס והן : I TYPE, J TYPE,R TYPE .

תבניות הפקודות :

Type	-31-			format (bits)		-0-
R	opcode (6)	rs (5)	rt (5)	rd (5)	shamt (5)	funct (6)
I	opcode (6)	rs (5)	rt (5)	immediate (16)		
J	opcode (6)	address (26)				

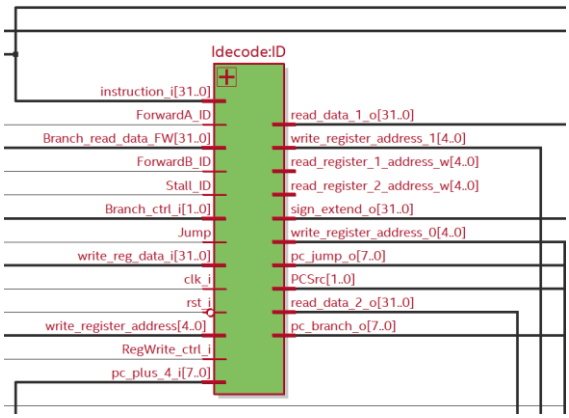
כך נשלוף את הכתובת רגיסטרים איתם נרצה לעבוד בשלבים המתקדמים במעבד. בנוסף בשלב זה נרצה לפענח את סוג הפקודה הרצויה להתבצע, וכך אותות הבקרה במודול הבא יעלו בהתאם.

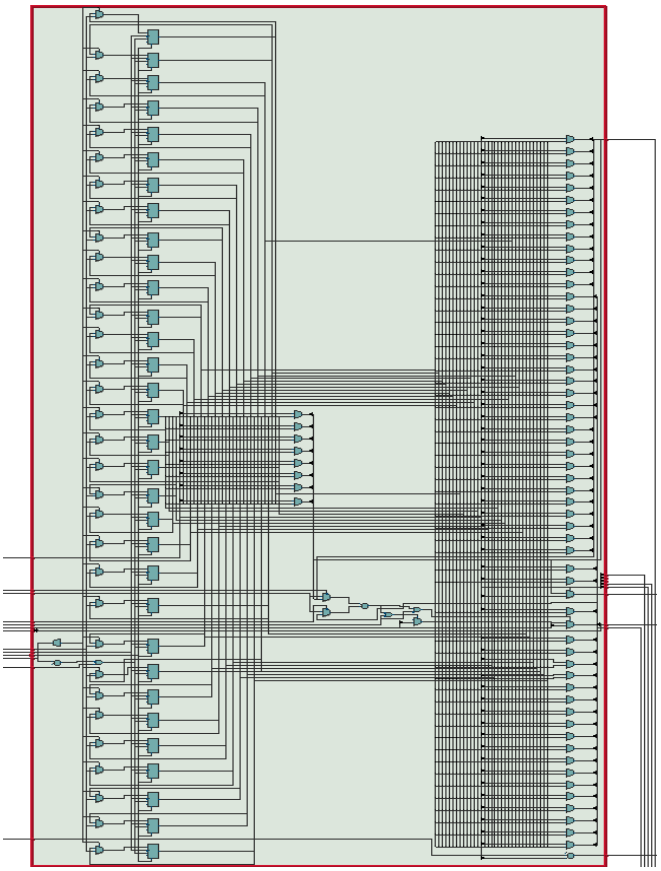
כדי לייעל את פעילות המעבד כבר בשלב זה נבצע את פעולות ההסתעפות : BRUNCH ו JUMP, אם אחד מהם מתקיים. במידת הצורך נקבל נתונים ממודל ה FORWORDING.

בנוסף בשלב זה יושבת יחידת הCONTROL האחראית להעלות את כל קווי הבקרה הדרושים לפעילות התקינה של המעבד וביצוע הפקודות.

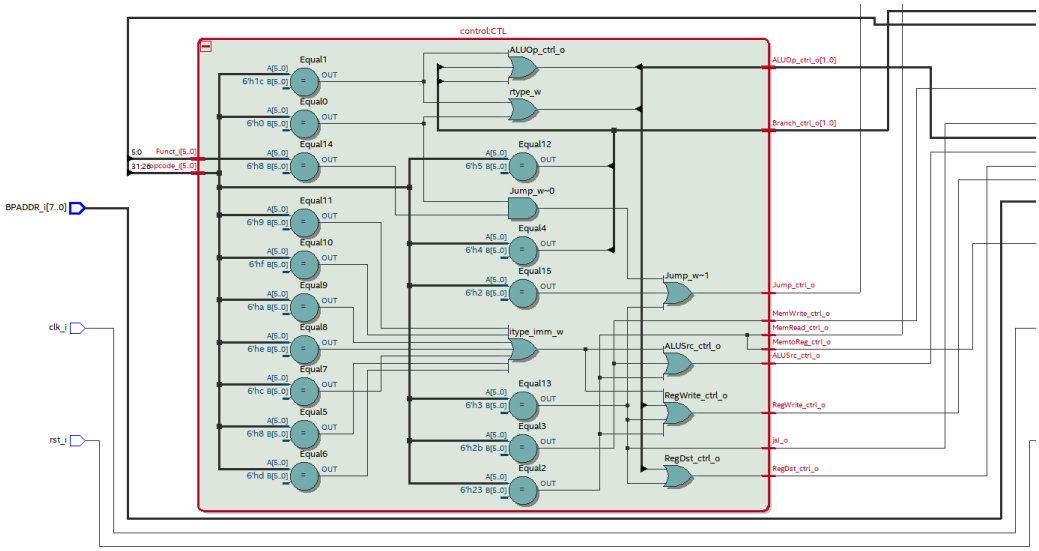
יחידה זאת מקבלת 2 שדות חשובים לפיענוח הפקודה והם שדה ה OPCODE ושדה ה FUNCT.

ה RTL של DECODE :





ה RTL של יחידת ה CONRTOL :



מודול ה EXECUTE :

בשלב זה במעבד הפקודות יוצאות לפועל, כלומר בשלב זה נמצאים רכיבים חשובים במעבד כמו רכיב ה ALU ורכיב ה SHIFTER.

בשלב זה מבצעים פקודות כמו חישוב כתובות או ביצוע פעולות אריתמטיות.

כשעבדנו עם מעבד SINGLE CYCLE בוצעו בשלב זה גם חישוב ה PC הבא ופקודות ההסתעפות.

כעת כשעברנו למעבד PIPELINE עלינו להוסיף עוד 2 מודולים הכרחיים שהם HAZARD UNIT ו FORWORDING UNIT.

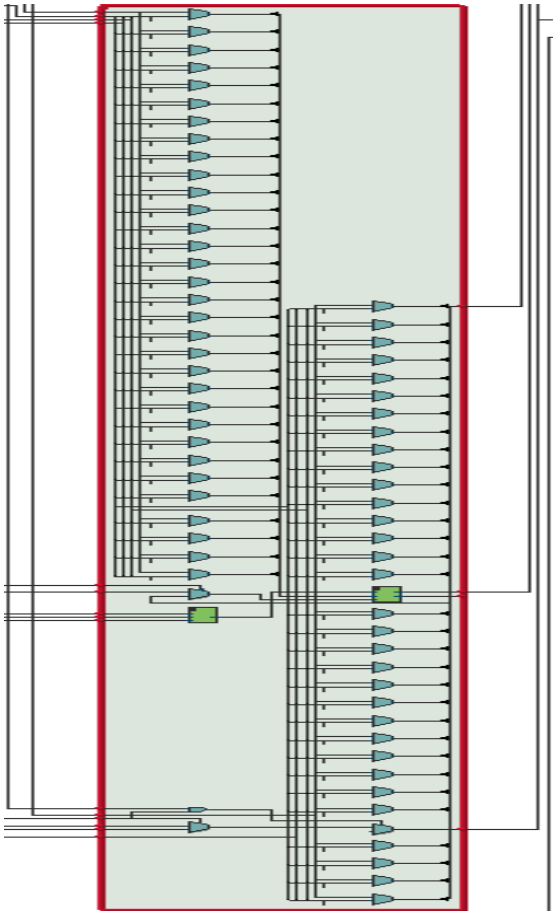
זאת מכיוון שיתכן שחישבנו כתובות או נתונים במעבד לפקודה אחת אך לפקודה אחריה נצטרך להשתמש בנתונים אלה שיתכן שעוד לא הספיקו להישמר בכתובות או ברגיסטרים המתאימים. לשם כך, יש 2 אותות חשובים שהם STALL ו FLUSH.

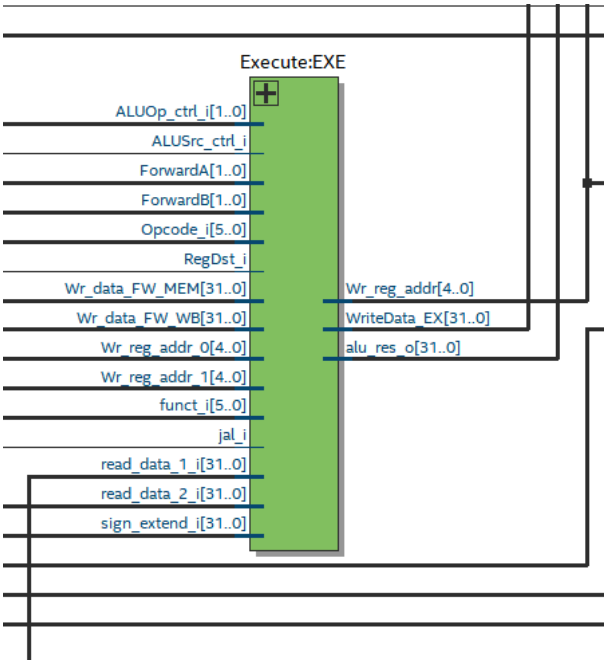
לדוגמה בפקודת BRUNCH הנמצאת בשלב הDECODE ועתידה להתבצע יש בשלב ה FETCH פקודה חדשה. ברגע שההחלטה לבצע BRUNCH התבצעה יש לבצע FLUSH לשלב ה FETCH ולזרוק את הפקודה וה PC יתעדכן לערך הרצוי.

פקודת STALL היא פקודה המבצעת NOP, כלומר היא פקודה הממתינה סייקל כדי שהמידע יוכל לעבור בPIPELINE באופן תקין.

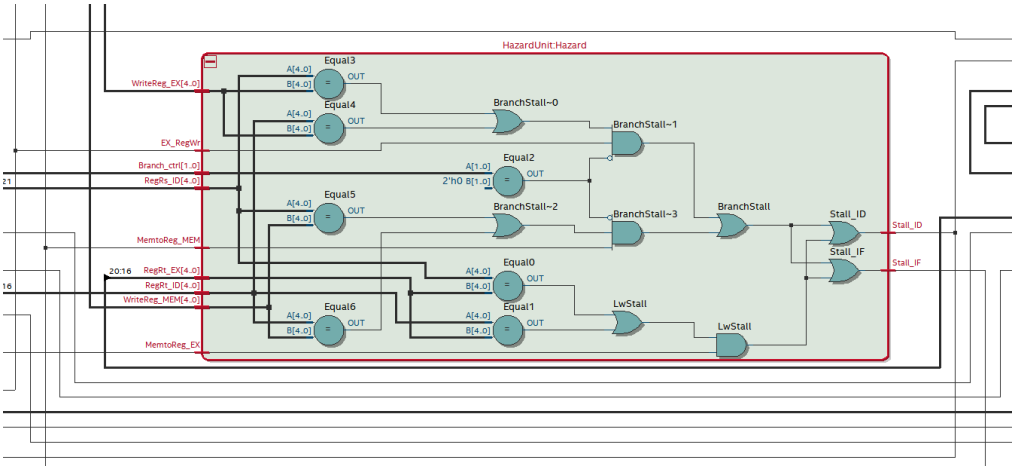
יחידת ה FORWARDING חשובה במעבד זה על מנת לפתור בעיות של DATA DEPENDENCIES.

RTL של יחידת ה EXECUTE :

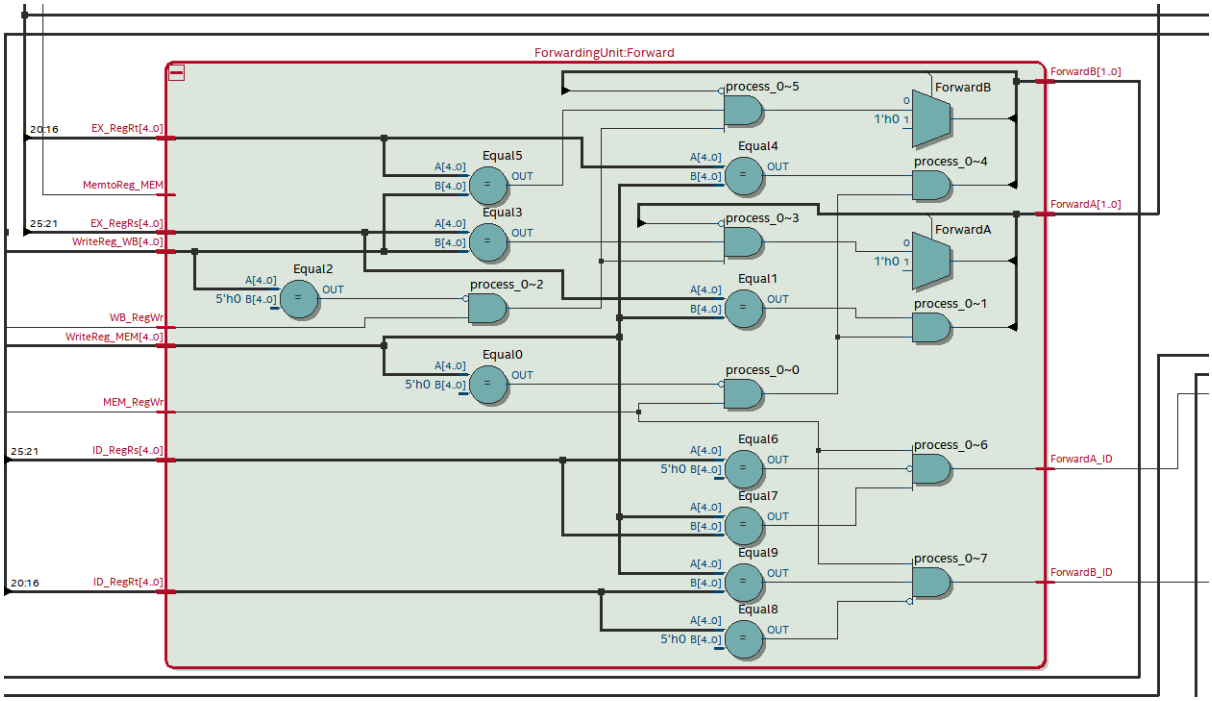




RTL של יחידת הHAZARD :



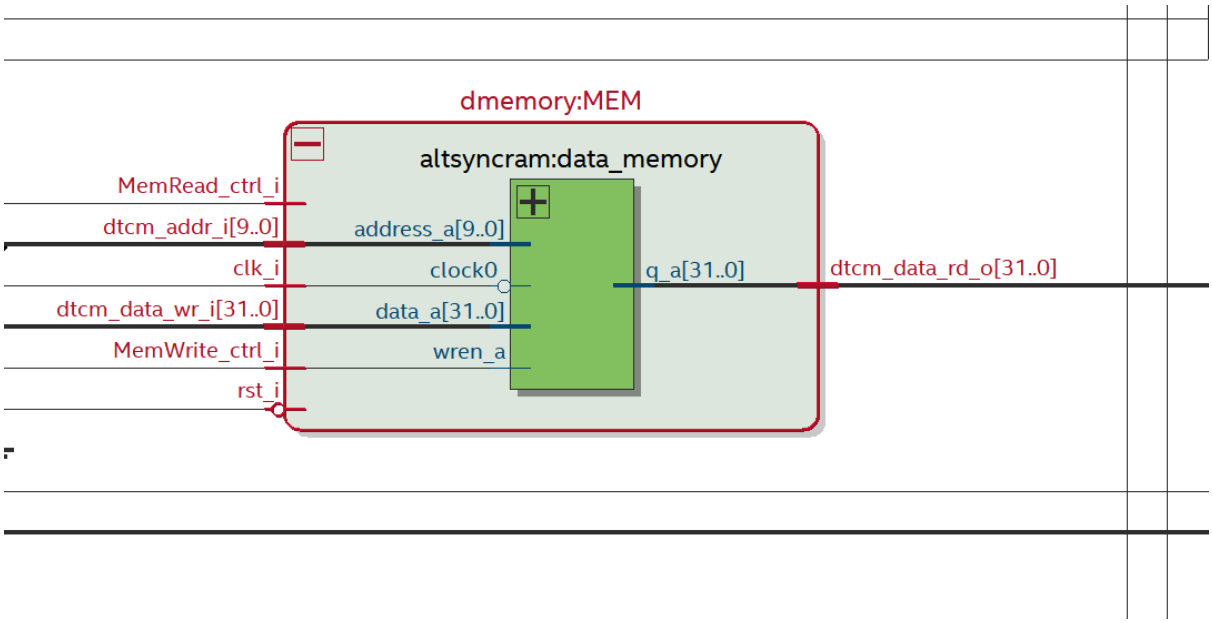
ה RTL של יחידת ה FORWORDING :



מודול ה DATA MEMORY :

מודל זה אחראי על ביצוע הכתיבה והקריאה מתוכן ה DATA MEMORY שזהו בעצם זיכרון ה RAM של המערכת שלנו.

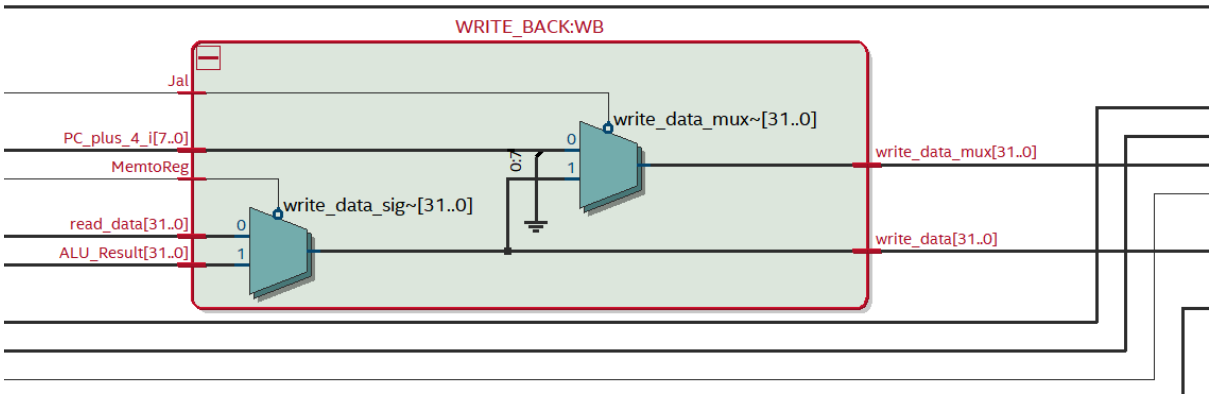
ה RTL של יחידת הDATA MEMORY :



מודול ה WRITE BACK :

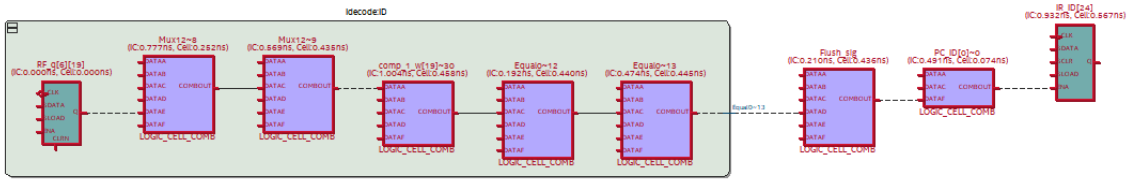
מודול זה אחראי על ניהול החזרת המידע וכתיבת המידע לזיכרון בסוף שלבי ה PIPELINE. מודול זה מוציא את הכתובת ואת המידע כתוצאה מהפעולה שהמעבד ביצע ושולחת את התוצאה לרכיבים הרלוונטיים במעבד לצורך שמירת המידע.

ה RTL של יחידת ה WRITE BACK :



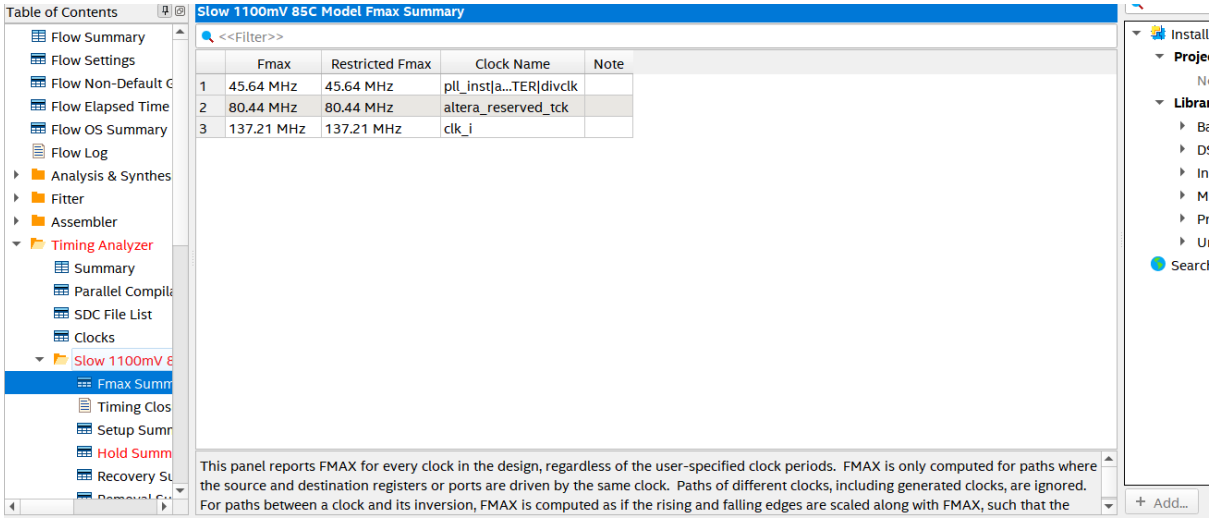
המסלול הקריטי :

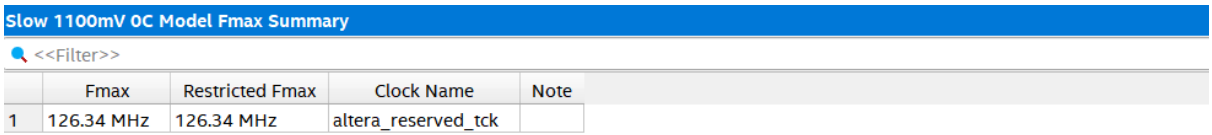
מתוך תוכנת ה QUARTRUS נמצא את המסלול הקריטי במעבד שלנו. הנתיב הקריטי אותו קיבלנו הינו ה DATA MEMORY.



מציאת תדר מקסימלי :

מתוך תוכנת ה QUARTRUS נמצא את התדר המקסימלי של המעבד שלנו :





SIGNLE TAP

בשלב זה ביצענו את הבדיקות על הקוד שכתבנו בעזרת תוכנת ה QUARTUS. לכל טסט הוצאנו קבצי ITCM ו DTCM מתאימים לביצוע התוכנית. קבצים אלה קבצים מותאמים לבקר שלנו אותם הוצאנו מתוך תוכנת ה MARS בקוד MIPS.

את הבקר קינפגנו כך ש RST מחובר לכפתור KEY0 והמתגים מחוברים לפי ביט לתוצאת ה BPADDER.

לאחר ביצוע קומפילציה וצריבת התוכנית הרצנו את הקוד וחיכינו לעצירתו כאשר נגיע לTRIGGER המתאים שהזנו.

להלן 6 טסטים שביצענו ופירוט על מה ניתן לראות בכל טסט.

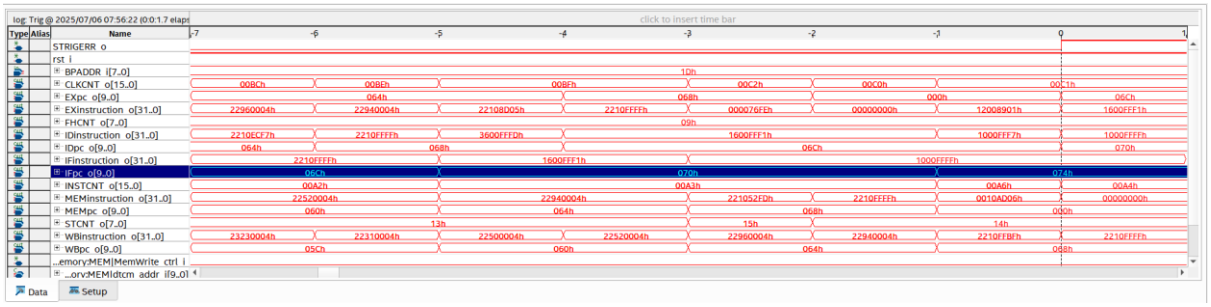
קבצי ה STP המצורפים ממוספרים לפי מספרי הטסטים המוצגים בקטע זה.

הסבר טסט 1 : נבחין כי בטסט זה הגדרנו את ה BPADDER להיות תוצאת ה pc בסיום הרצת התוכנית כמבוקש. אכן, ניתן לראות כי הטסט עצר בהגעה לערך הPC המתאים כלומר התוכנית עצרה בזמן המתאים.

עוד ניתן לראות את מעבר הפקודות בPIPELINE במוצא ה PC בכל מעבר רגיסטר.

ניתן לראות בסיום הרצת התוכנית את תוצאת הזיכרון שכוללות את המערכים המקוריים ולאחר מכן את תוצאות הפעולות שנעשו במעבד שהן פעולות חיבור, כפל וחיסור ואת האיחסון שלהם במקומות היעודים בזיכרון.

טסט 1



Instance 0: DTCM

000000	00	00	00	0A	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	01	00	00	00	00	00	00	00	00	00	00	00	02	00	00	00	00
00000a	00	00	00	00	00	00	00	00	00	00	00	03	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	04	00	00	00	00	00	00	00	00	00	00	00	00
000014	00	00	00	05	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	06	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	07	00	00	00	00
00001e	00	00	00	00	00	00	00	00	00	00	00	08	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	09	00	00	00	00	00	00	00	00	00	00	00	00
000028	00	00	00	0A	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	64	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	63	00	00	00	00
000032	00	00	00	00	00	00	00	00	00	00	00	62	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	61	00	00	00	00	00	00	00	00	00	00	00	00
00003c	00	00	00	60	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	5F	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	5E	00	00	00	00
000046	00	00	00	00	00	00	00	00	00	00	00	5D	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	5C	00	00	00	00	00	00	00	00	00	00	00	00
000050	00	00	00	5B	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	65	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	65	00	00	00	00
00005a	00	00	00	00	00	00	00	00	00	00	00	65	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	65	00	00	00	00	00	00	00	00	00	00	00	00
000064	00	00	00	65	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	65	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	65	00	00	00	00
00006e	00	00	00	00	00	00	00	00	00	00	00	65	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	65	00	00	00	00	00	00	00	00	00	00	00	00
000078	00	00	00	65	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	64	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	C6	00	00	00	00
000082	00	00	00	00	00	00	00	00	00	00	01	26	00	00	00	00	00	00	00	00	00	00	00	00	00	00	01	84	00	00	00	00	00	00	00	00	00	00	00	00
00008c	00	00	01	E0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	02	3A	00	00	00	00	00	00	00	00	00	00	00	00	00	00	02	92	00	00	00	00
000096	00	00	00	00	00	00	00	00	00	00	02	E8	00	00	00	00	00	00	00	00	00	00	00	00	00	00	03	3C	00	00	00	00	00	00	00	00	00	00	00	00
0000a0	00	00	03	8E	00	00	00	00	00	00	00	00	00	00	00	00	FF	FF	FF	9D	00	00	00	00	00	00	00	00	00	00	00	00	FF	FF	FF	9F	00	00	00	00
0000aa	00	00	00	00	00	00	00	00	FF	FF	FF	A1	00	00	00	00	00	00	00	00	00	00	00	00	FF	FF	FF	A3	00	00	00	00	00	00	00	00	00	00	00	00
0000b4	FF	FF	FF	A5	00	00	00	00	00	00	00	00	00	00	00	00	FF	FF	FF	A7	00	00	00	00	00	00	00	00	00	00	00	00	FF	FF	FF	A9	00	00	00	00
0000be	00	00	00	00	00	00	00	00	FF	FF	FF	AB	00	00	00	00	00	00	00	00	00	00	00	00	FF	FF	FF	AD	00	00	00	00	00	00	00	00	00	00	00	00
0000c8	FF	FF	FF	AF	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0000d2	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
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0000e6	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
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הסבר טסט 2 ו3 : נבחין כי בטסטים הבאים הגדרנו את ה BPADDER להיות תוצאת ה pc בסיום הרצת התוכנית כמבוקש. אכן, ניתן לראות כי הטסט עצר בהגעה לערך הPC המתאים כלומר התוכנית עצרה בזמן המתאים.

עוד ניתן לראות את מעבר הפקודות בPIPELINE במוצא ה PC בכל מעבר רגיסטר.

ניתן לראות בסיום הרצת התוכנית את תוצאת הזיכרון שכוללות את המערכים המקוריים ולאחר מכן את תוצאות הפעולות שנעשו במעבד שהן פעולות חיבור, כפל וחיסור הקורות במעבר על הקוד דרך לולאות וביצוע קפיצות (פעולות JUMP) ואת האיחסון שלהם במקומות היעודים בזיכרון.

נבחין כי קיבלנו תוצאות זהות לטסטים 1-3

ההבל בין טסטים 2,3 הוא באופן בו אנו ניגשים לפעולות מבחינת הקוד, ולכן נצפה לתוצאה זהה גם כאן.

טסט 2

Instance 0: DTCM

000000	00	00	00	01	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	02	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
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000078	FF	FF	FF	A9	00	00	00	00	00	00	00	00	00	00	00	00	FF	FF	FF	AB	00	00	00	00	00	00	00	00	00	00	00	64	00	00	00	00
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000096	00	00	00	00	00	00	00	00	00	00	02	92	00	00	00	00	00	00	00	00	00	00	00	00	00	00	02	E8	00	00	00	00	00	00	00	00
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0000be	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
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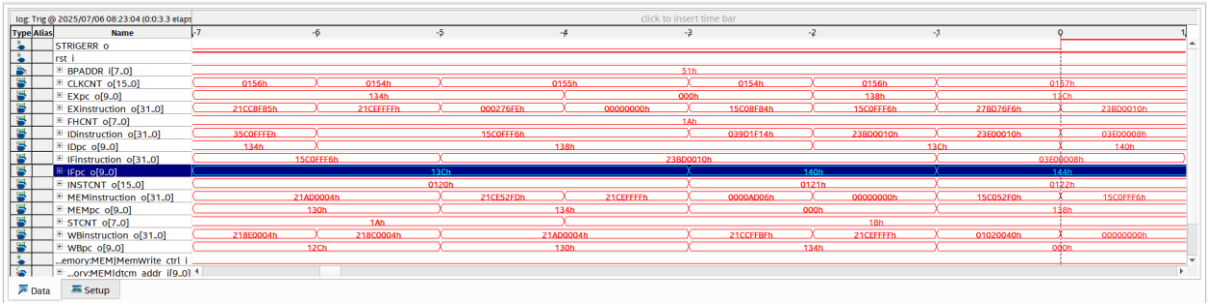
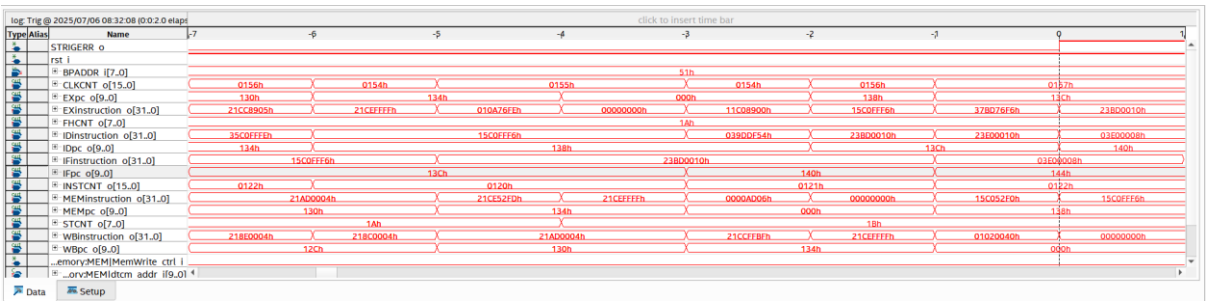


טסט 3



Instance 0: DTCM

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הסבר טסט 4 : כעת התבקשנו לכתוב טסט מקובץ C הניתן לנו בדו״ח מכין. אזי מה שביצענו הוא לכתוב את הקוד כקוד MIPS ולאחר הרצתו בMARS הוצאנו ITCM ו DTCM מתאימים להרצת התוכנית החדשה.

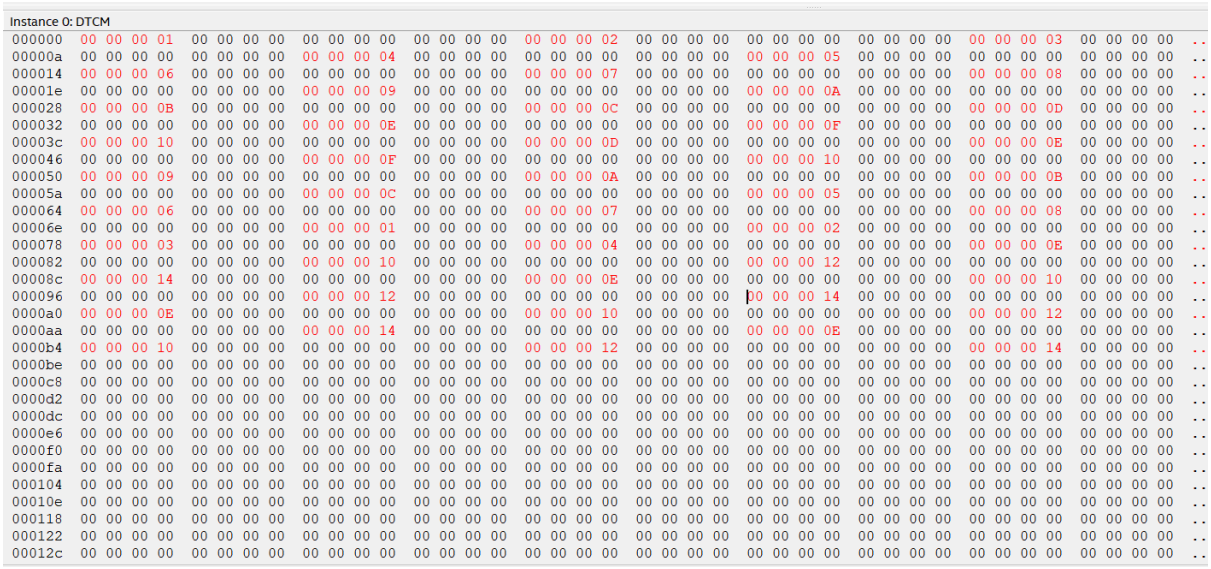
הקוד מבצע את הפעולות הבאות :

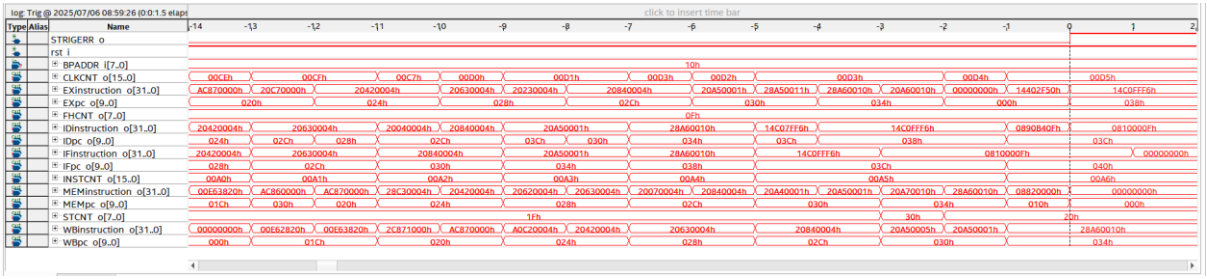
```
#define M 4

void addMats(int Mat1[M][M], int Mat2[M][M], int resMat[M][M]){
      define it yourself …
}

void main(){ //int=32bit
      int Mat1[M][M]={{1,2,3,4},{5,6,7,8},{9,10,11,12},{13,14,15,16}};
      int Mat2[M][M]={{13,14,15,16},{9,10,11,12},{5,6,7,8},{1,2,3,4}};
      int resMat[M][M];

      addMats(Mat1,Mat2,resMat); // resMat = Mat1 + Mat2
}
```

בזיכרון ניתן לראות את טעינת המערכים המקוריים ואת חישובי הפעולות שבוצעו במעבד ואוחסנו במקום היעודי.

גם כאן הגדרנו את ה BPADDER להיות הכתובת האחרונה של ה PC ובעליית הטריגר נעצרה התוכנית בכתובת הרצויה.

טסט 4





IPC = (166-15)/213=0.708

הסבר טסט 5 : בבדיקה זו, הגדרנו את רכיב ה־ BPADDER כך שישקף את ערך ה־ PCבסיום ביצוע התוכנית, בהתאם לדרישות. אכן, ניתן לראות כי ה־ PCהגיע לערך המצופה, מה שמעיד שהתוכנית נעצרה בזמן הנכון.

כמו כן, במהלך הריצה ניתן לעקוב אחר מעבר ההוראות לאורך שלבי ה PIPELINE דרך ערכי ה PC המופיעים במעבר בין רגיסטרים.

בסיום הריצה נצפו בזיכרון הנתונים המקוריים כלומר המערכים, ולאחריהם התוצאות של הפעולות הלוגיות שבוצעו במעבד, שהן AND, OR, XOR אשר אוחסנו במיקומים הייעודיים בזיכרון, בהתאם לתוכנית.

טסט 5

Instance 0: DTCM

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שמרנו את התוצאות במקומות היעודיים. גם כאן בדומה לשאר הטסטים הגדרנו את ה BPADDER להיות סוף הרצת התוכנית מה שמעלה לנו את הטריגר במקום הנכון לפי הpc של שלב ה FETCH.

טסט 6

Instance 0: DTCM

000000	00	00	00	01	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	64	00	00	00	00	00	00	00	00	00	00	00	03	00	00	00	00
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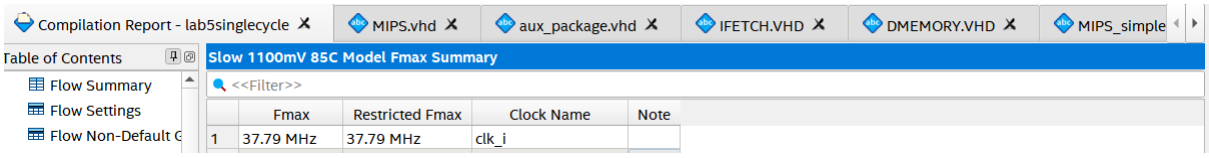
IPC = (166-15)/213=0.708

נצפה לקבל IPC זהה לשל טסט 4 מכיוון שמבנה הטסט זהה- הפקודות הלוגיות שונות.

Single Cycle:

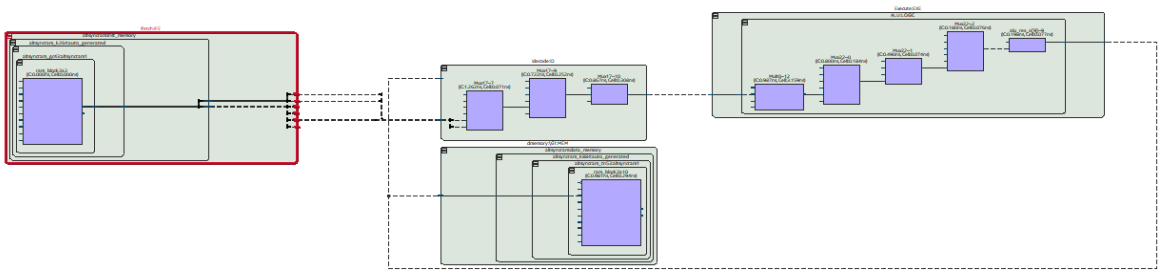
מציאת תדר מקסימלי:

מתוך תוכנת ה QUARTRUS נמצא את התדר המקסימלי של המעבד שלנו:



המסלול הקריטי:

מתוך תוכנת ה QUARTRUS נמצא את המסלול הקריטי במעבד שלנו. הנתיב הקריטי אותו קיבלנו הינו ה DATA MEMORY.



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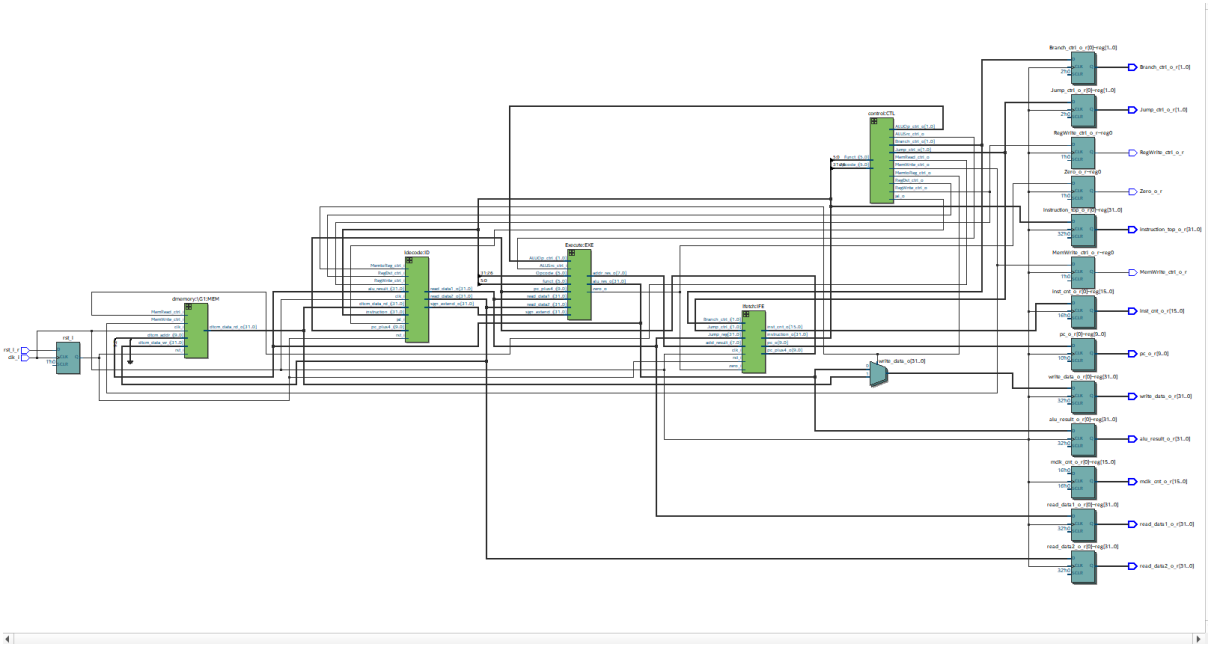

תיקון לאחר מעבר לפורמט הנכון:

טסט 2

8STP

Instance Manager: Ready to acquire

Index	Instance ID	Status	Width	Depth	Type	Mode
0	DTCM	Not running	32	256	RAM/ROM	Read/Write

Instance 0: DTCM

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00001e	FF	FF	FF	A9	FF	FF	FF	AB	00	00	00	64	00	00	00	C6	00	00	01	26	00	00	01	84	00	00	01	E0	00	00	02	3A	00	00	02	92	00	00	02	E8
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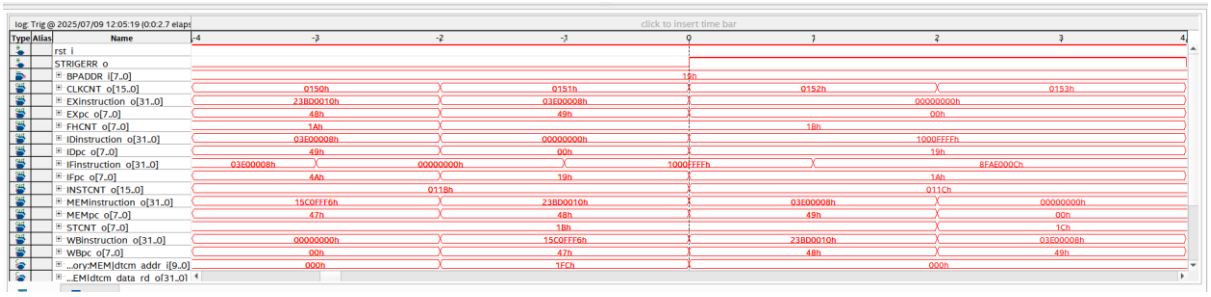

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9STP

Instance 0: DTCM

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000014	00 00 00 5B	00 00 00 65	00 00 00 65	00 00 00 65	00 00 00 65	00 00 00 65	00 00 00 65	00 00 00 65	00 00 00 65	00 00 00 65
00001e	00 00 00 65	00 00 00 64	00 00 00 C6	00 00 01 26	00 00 01 84	00 00 01 E0	00 00 02 3A	00 00 02 92	00 00 02 E8	00 00 03 3C
000028	00 00 03 8E	FF FF FF 9D	FF FF FF 9F	FF FF FF A1	FF FF FF A3	FF FF FF A5	FF FF FF A7	FF FF FF A9	FF FF FF AB	FF FF FF AD
000032	FF FF FF AF	00 00 00 00	00 00 00 00	00 00 00 00	00 00 00 00	00 00 00 00	00 00 00 00	00 00 00 00	00 00 00 00	00 00 00 00
00003c	00 00 00 00	00 00 00 00	00 00 00 00	00 00 00 00	00 00 00 00	00 00 00 00	00 00 00 00	00 00 00 00	00 00 00 00	00 00 00 00
000046	00 00 00 00	00 00 00 00	00 00 00 00	00 00 00 00	00 00 00 00	00 00 00 00	00 00 00 00	00 00 00 00	00 00 00 00	00 00 00 00
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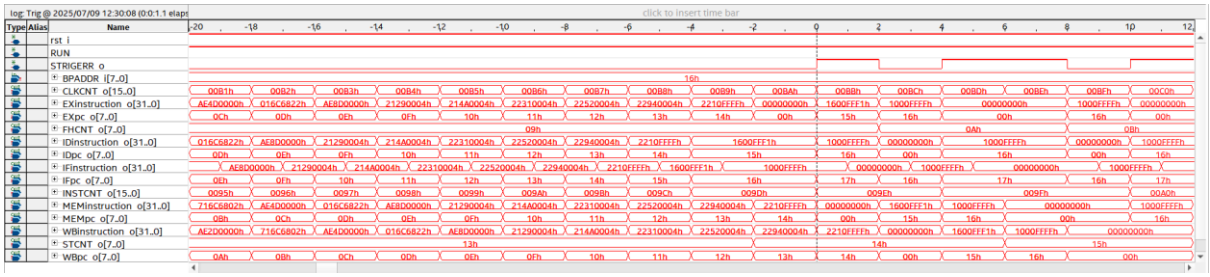

טסט 3

STP10

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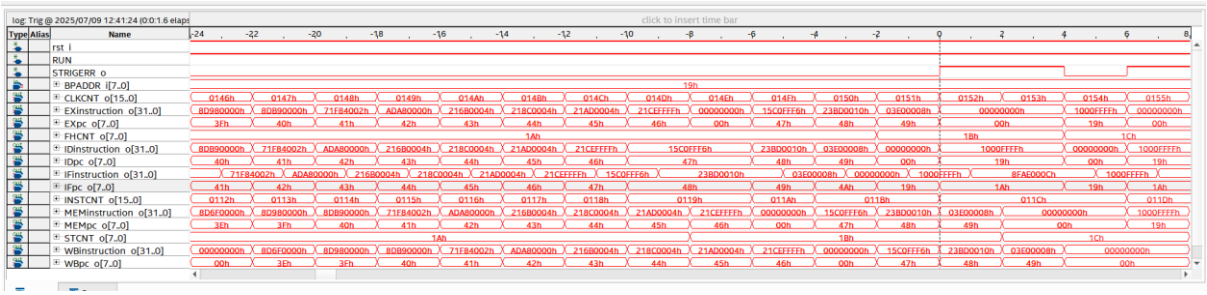
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