THE AMERICAN UNIVERSITY IN CAIRO
الجامعة الأمريكية بالقاهرة

Computer Architecture Project 1

MS4

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To

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Due date: April, 20th, 2019

- At first, we started by debugging the single memory and fixed the following issues:
    - Removed the counter signal to be part of the memory input. Instead we added two MUXs in the RISC-V module.
    - Added a MUX that chooses between func3 and 3'b010, namely "lw" func3 value depending on the counter value, whether it wants to get a data value or an instruction.
    - Added another MUX to determine the value of the MemRead and MemWrite signals. If the value getting fetched is a data, it selects the value of the MemRead and MemWrite. Otherwise, it passes a 1 for the MemRead and 0 for MemWrite, to read the instruction from the memory without writing any data back.
    - For the initial test program, we modified the offset of the "lw" and "sw" instructions to access the data section directly. Also, we divided the instruction into four memory elements because of byte addressability.