**CND 121: Introduction to Silicon Process & VLSI**

**Final Project**

**Section #: 16**

**Group #: 1**

**Project #: 5**

**Submitted by:**

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| --- | --- |
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**Submitted to Prof: Magdy Elmorsy**

**TA: Mariam Taher**

**Date: 14/12/2023**

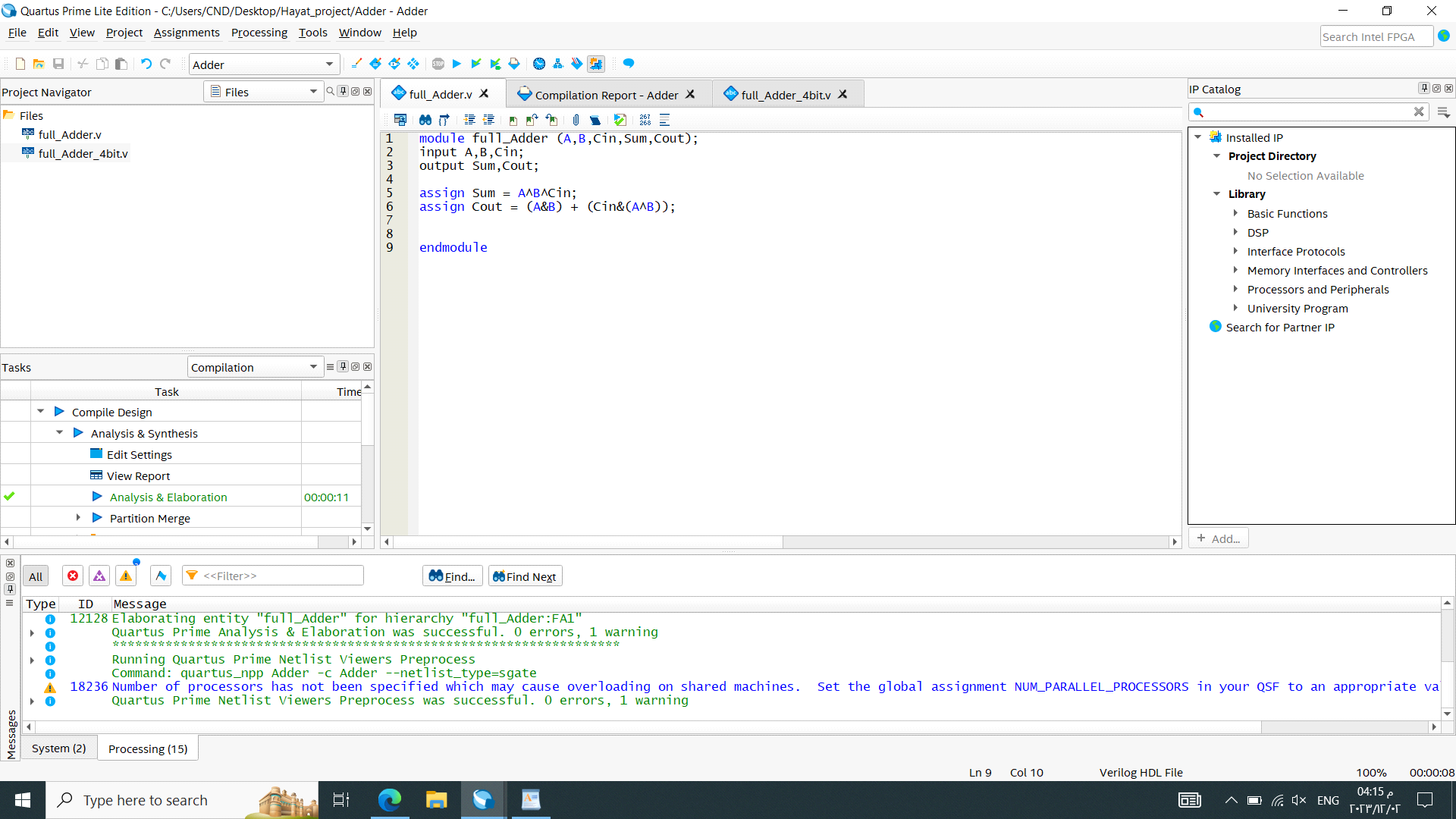
**Design of 4-bit Full Adder**

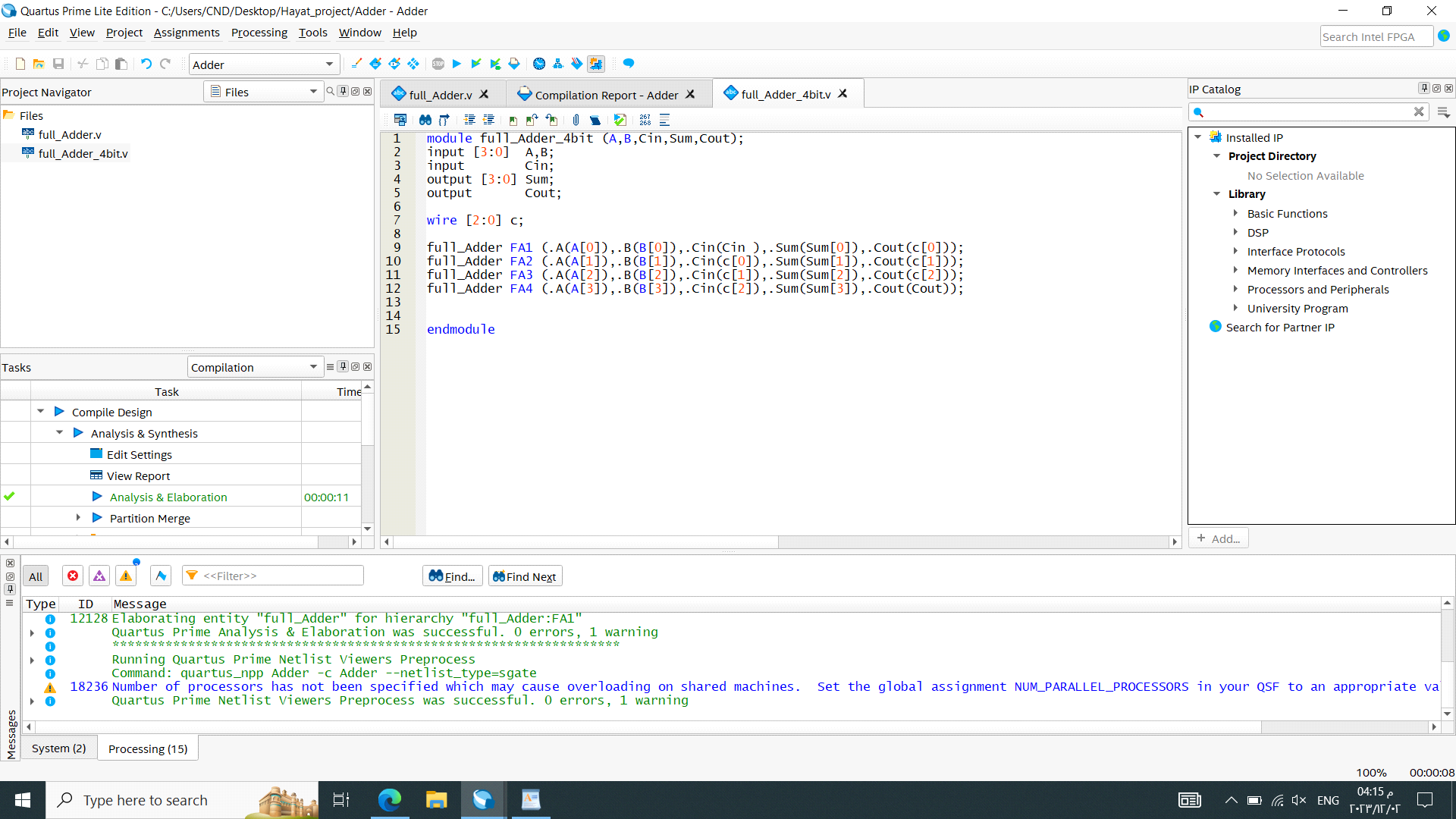
1. **Project Description**: :

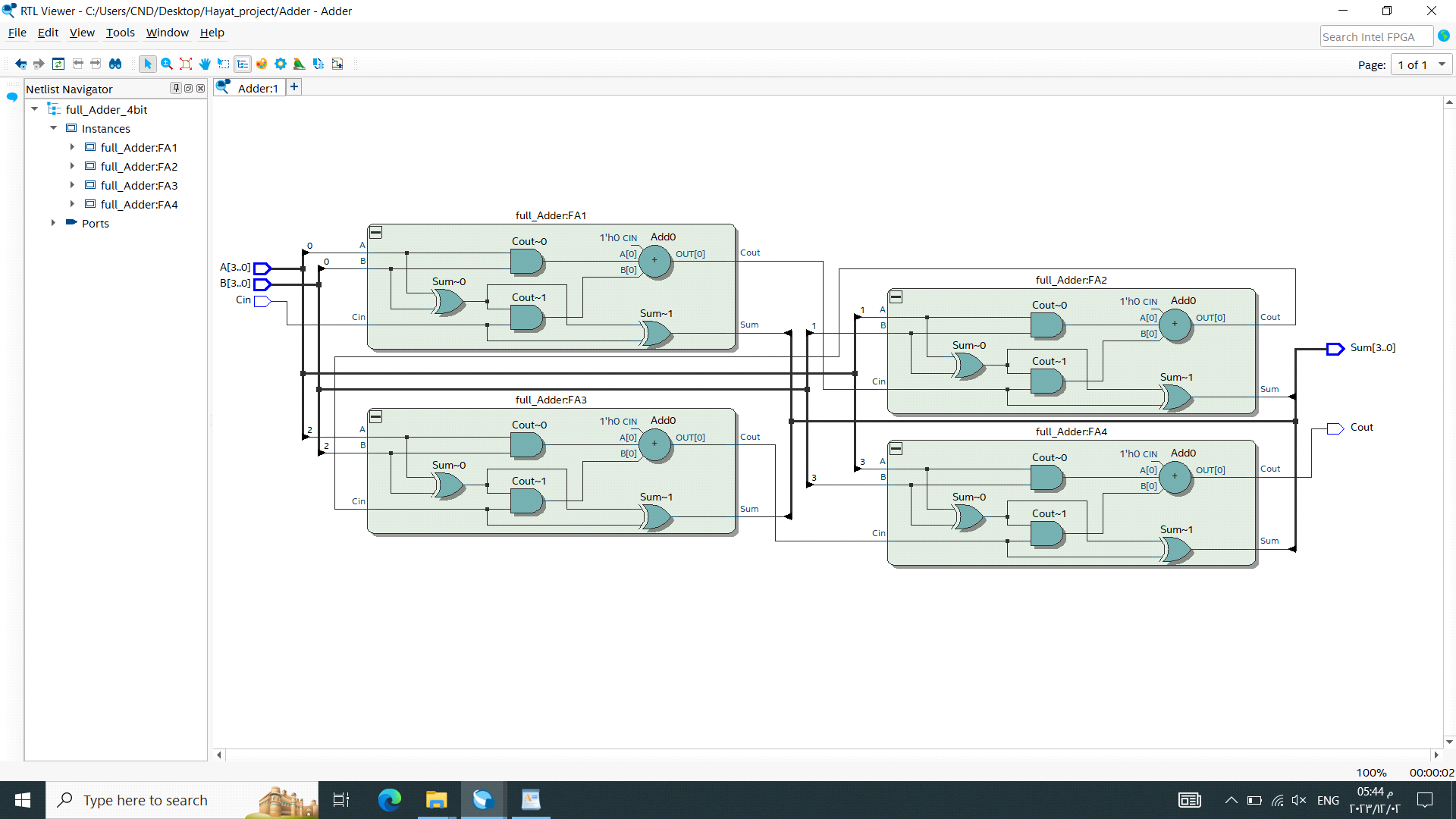
The aim of this project is to design 4-bit Full Adder using different techniques (Ripple Carry, Carry LookAhead)

1. **Our Approach :**

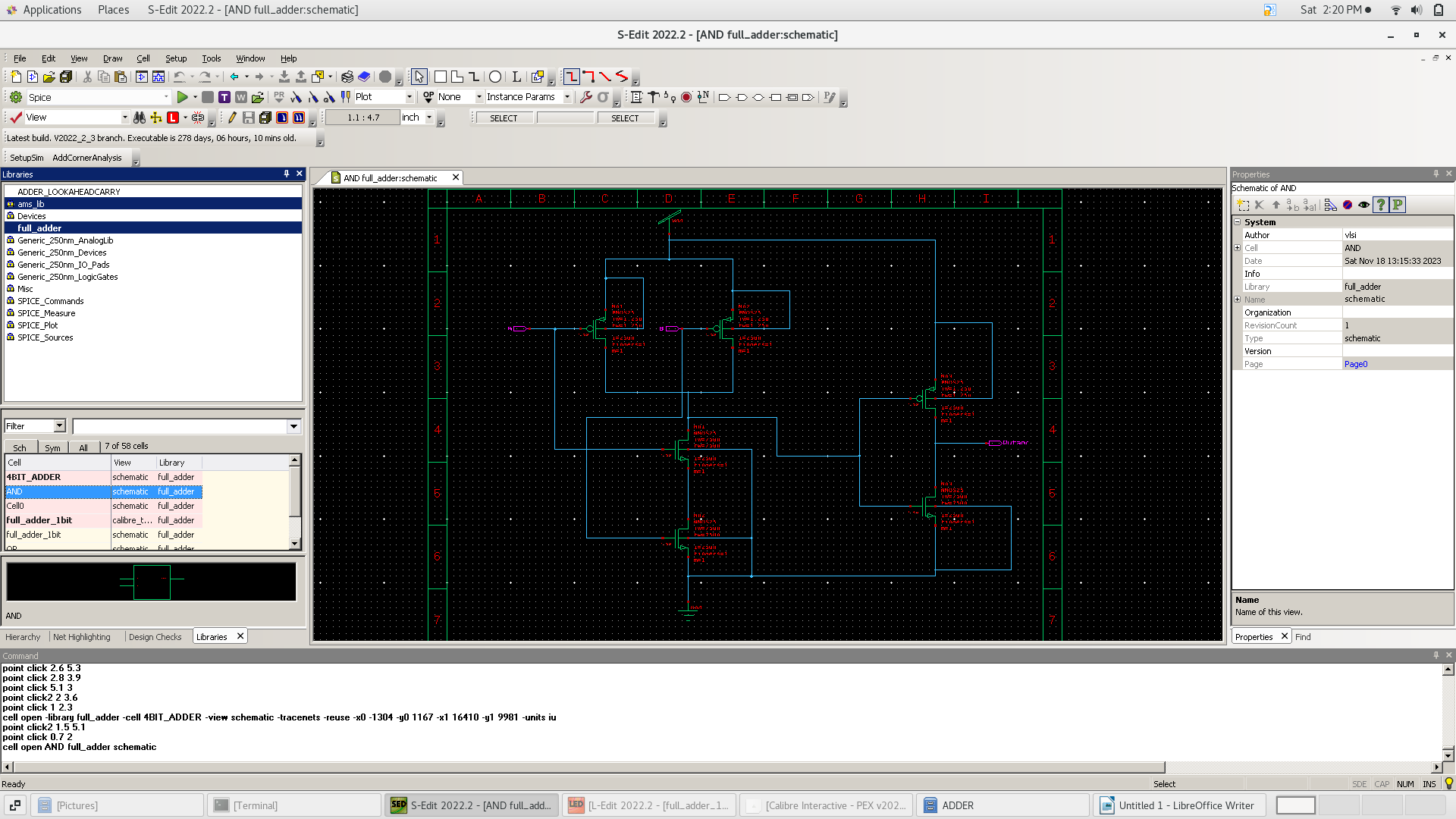
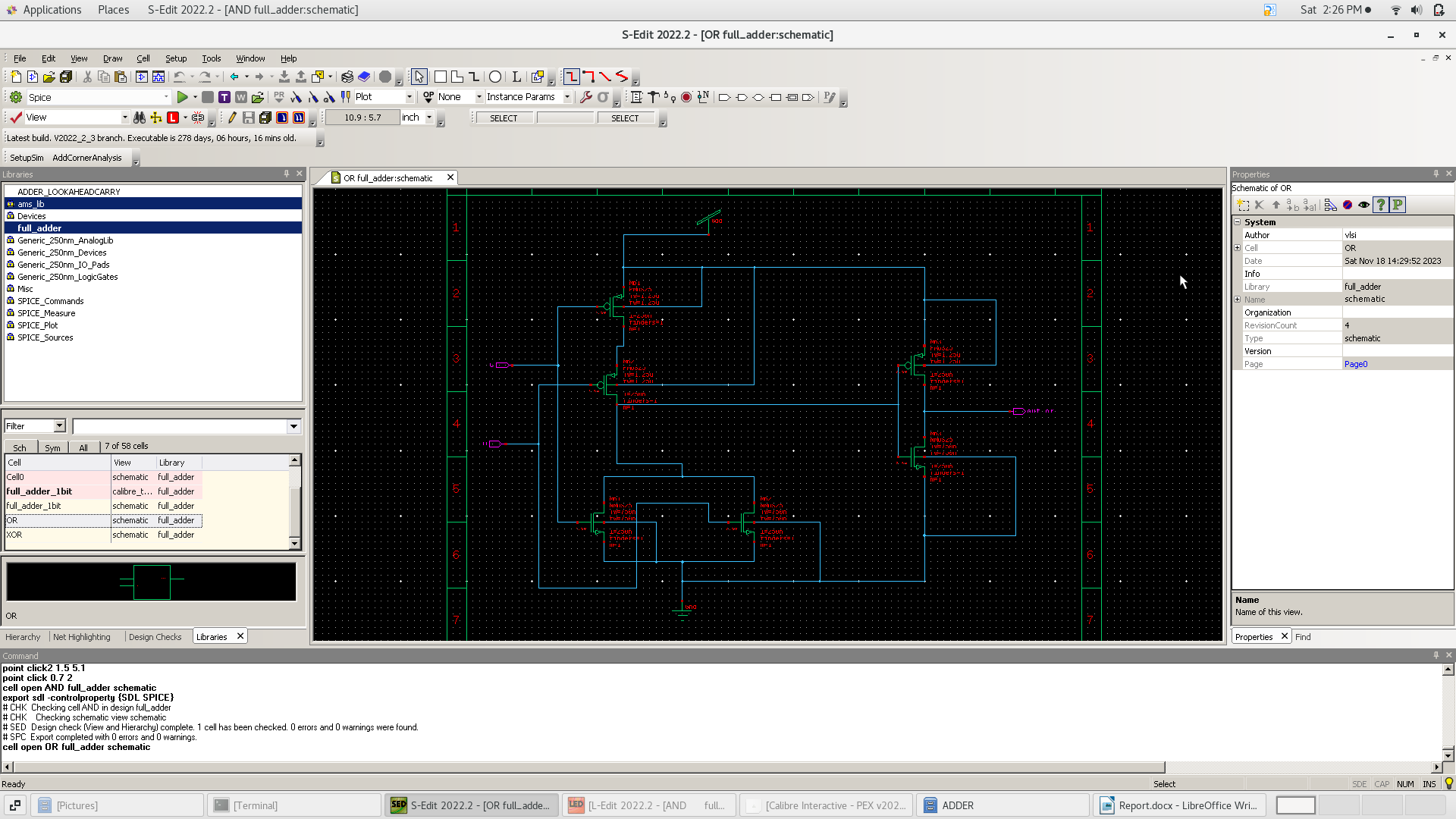
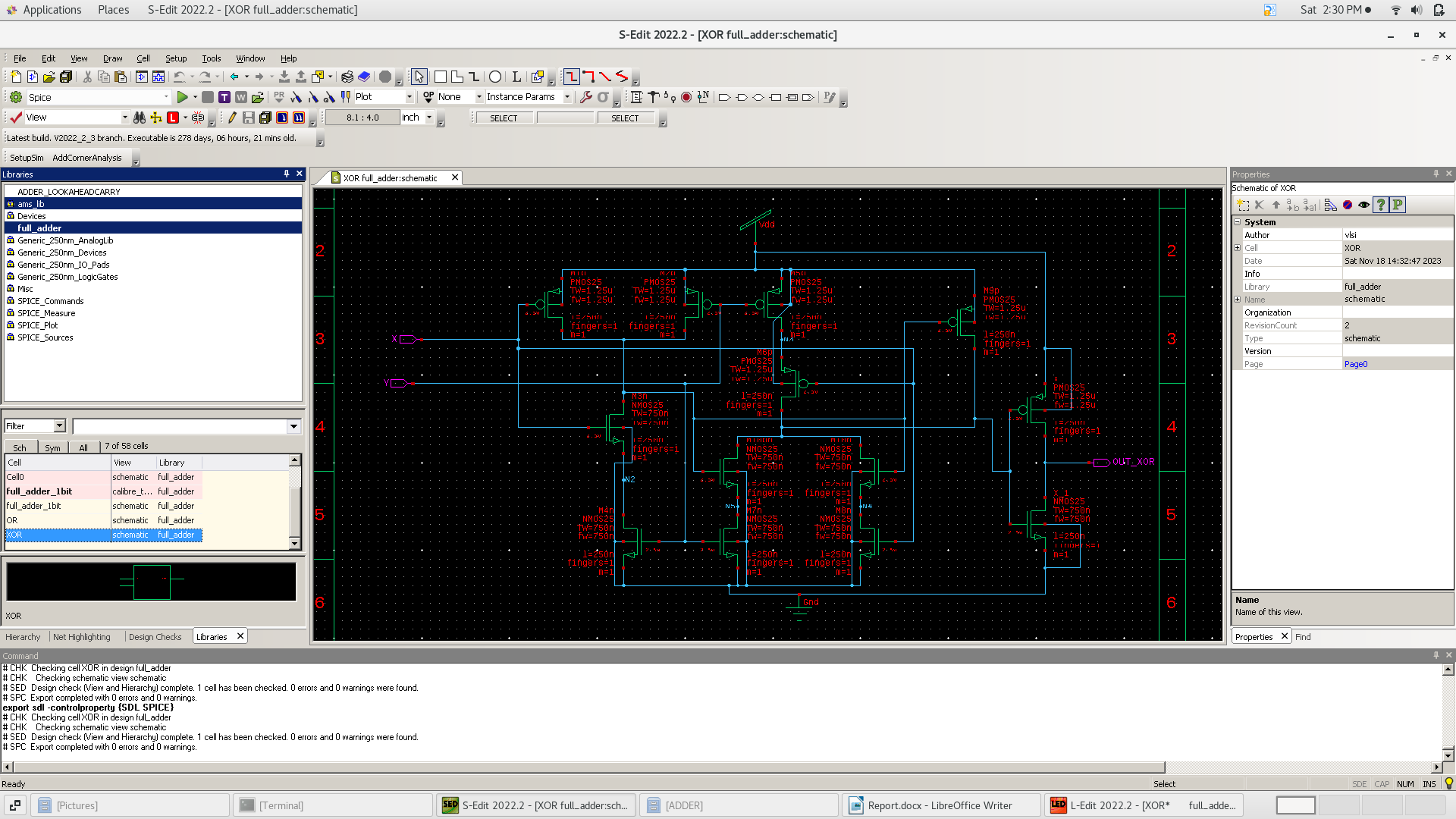
For each design we wrote the RTL (behavioral description) of,then we made a schematic that matches the output netlist in parallel with the layout as a hierarchy for each block.

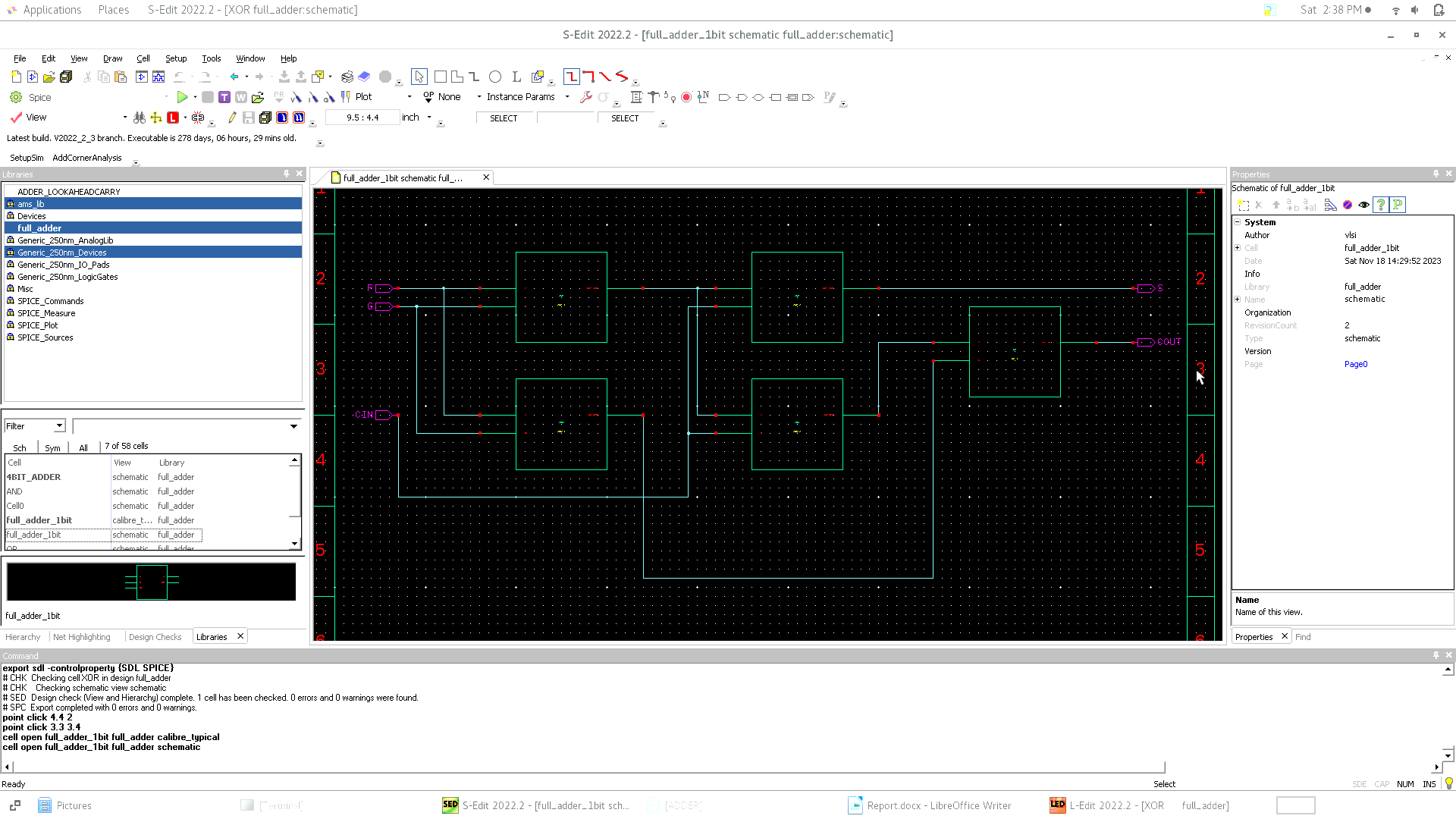
1. **Ripple Carry:**
2. **RTL**



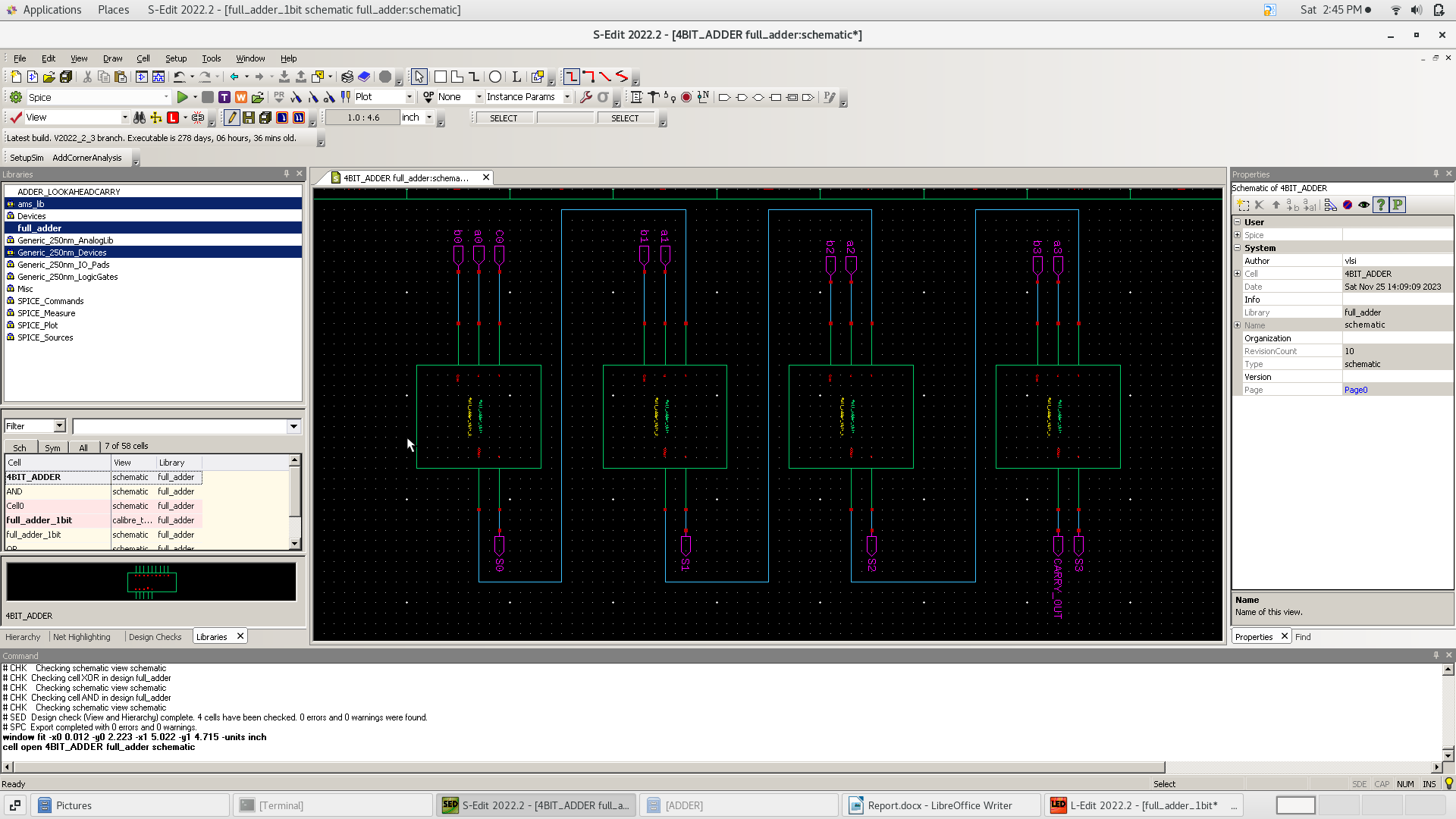
1. **Output Netlist**

For the schematic and layout, we started from basic blocks

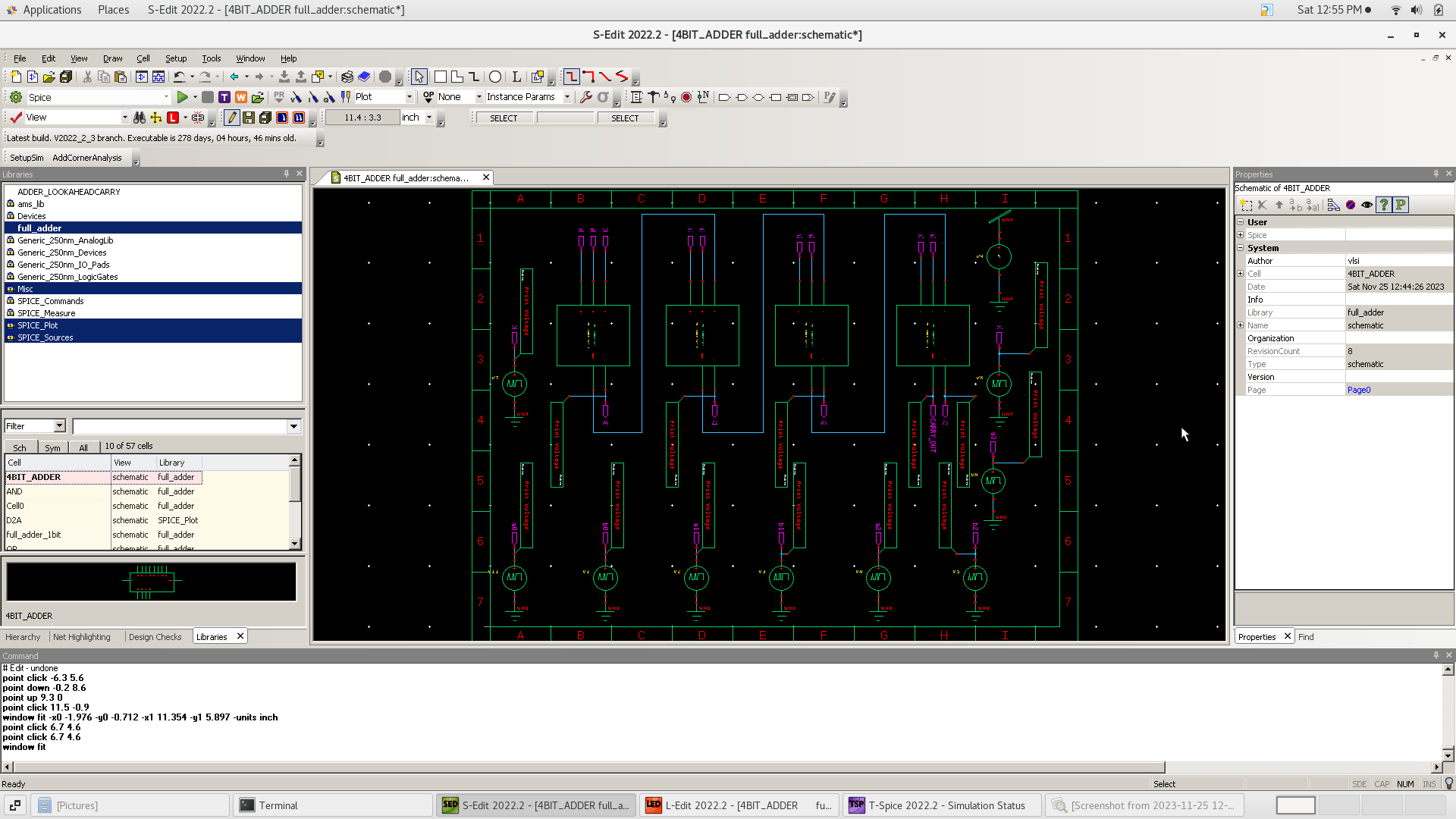
1. **AND Gate Schematic**
2. **OR Gate Schematic**
3. **XOR Gate Schematic**
4. **1-bit Full Adder Schematic**

After preparing basic components and the symbol of each we will build the 1-bit adder identical to the output netlist

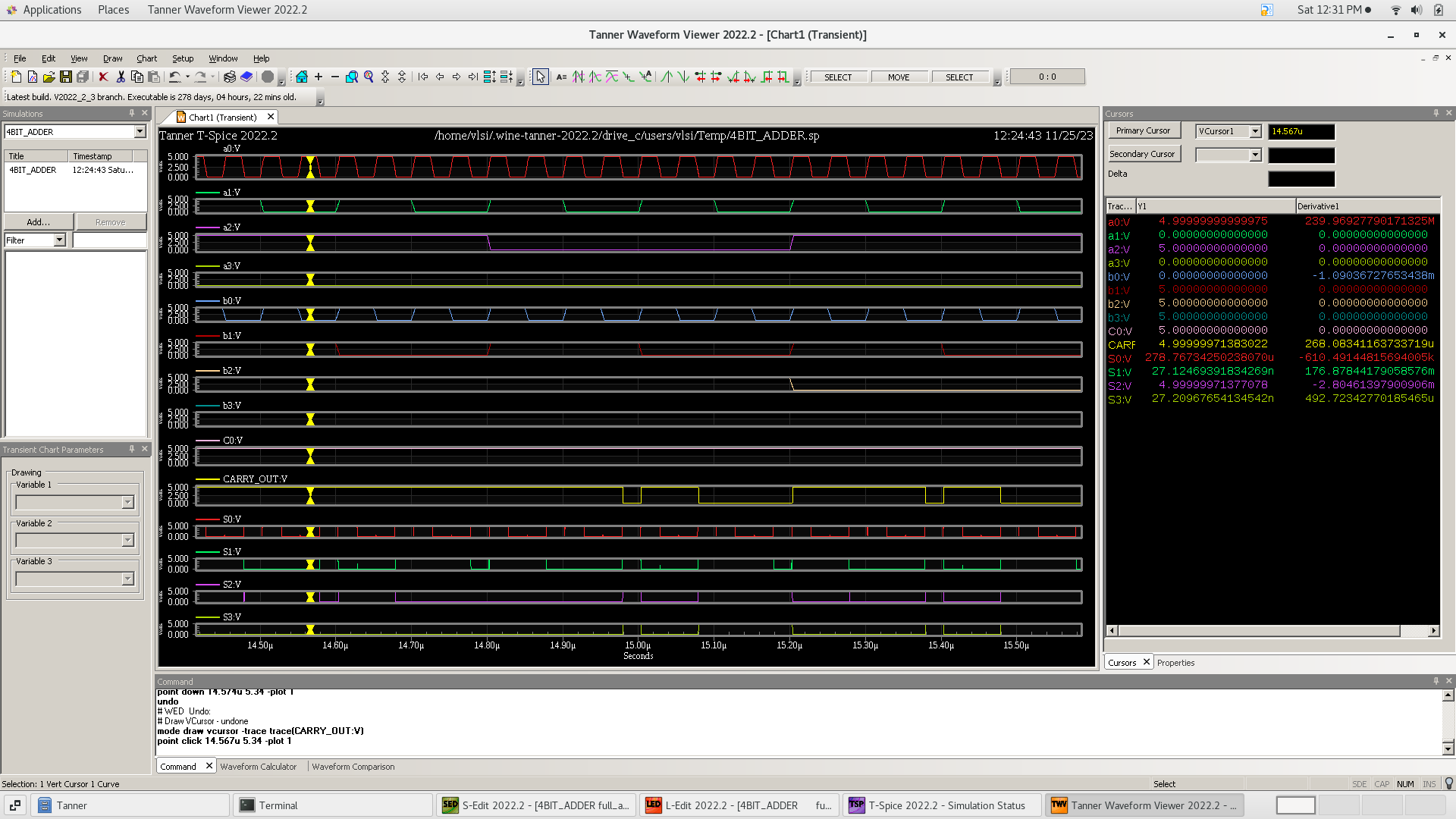
1. **4-bit Full Adder Schematic**

using the symbol of 1-bit Full Adder we will build 4-bit Adder

1. **Test Bench of Ripple Carry Adder**

we start to test the circuit to verify its functionality

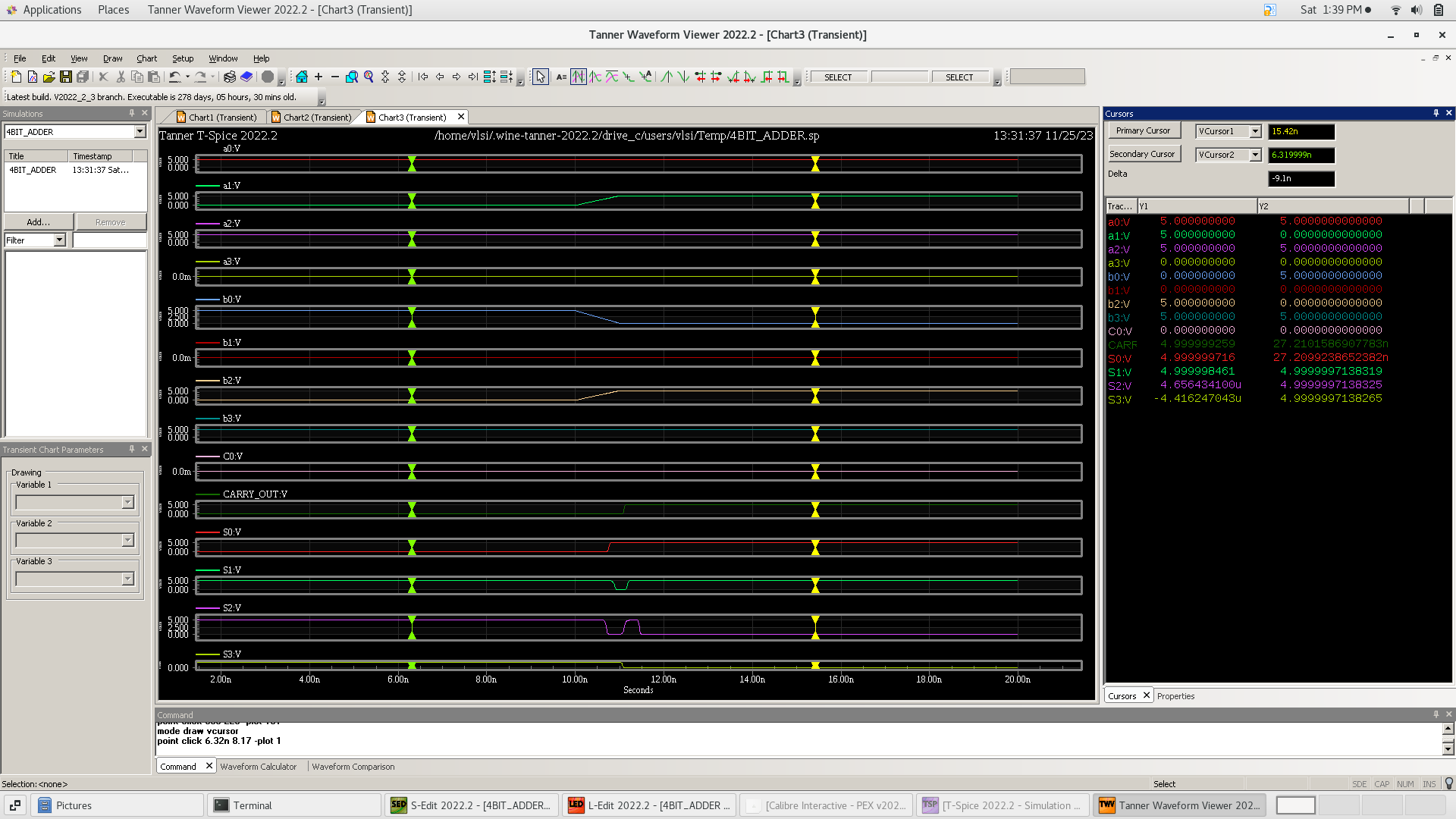
1. **Simulation results**

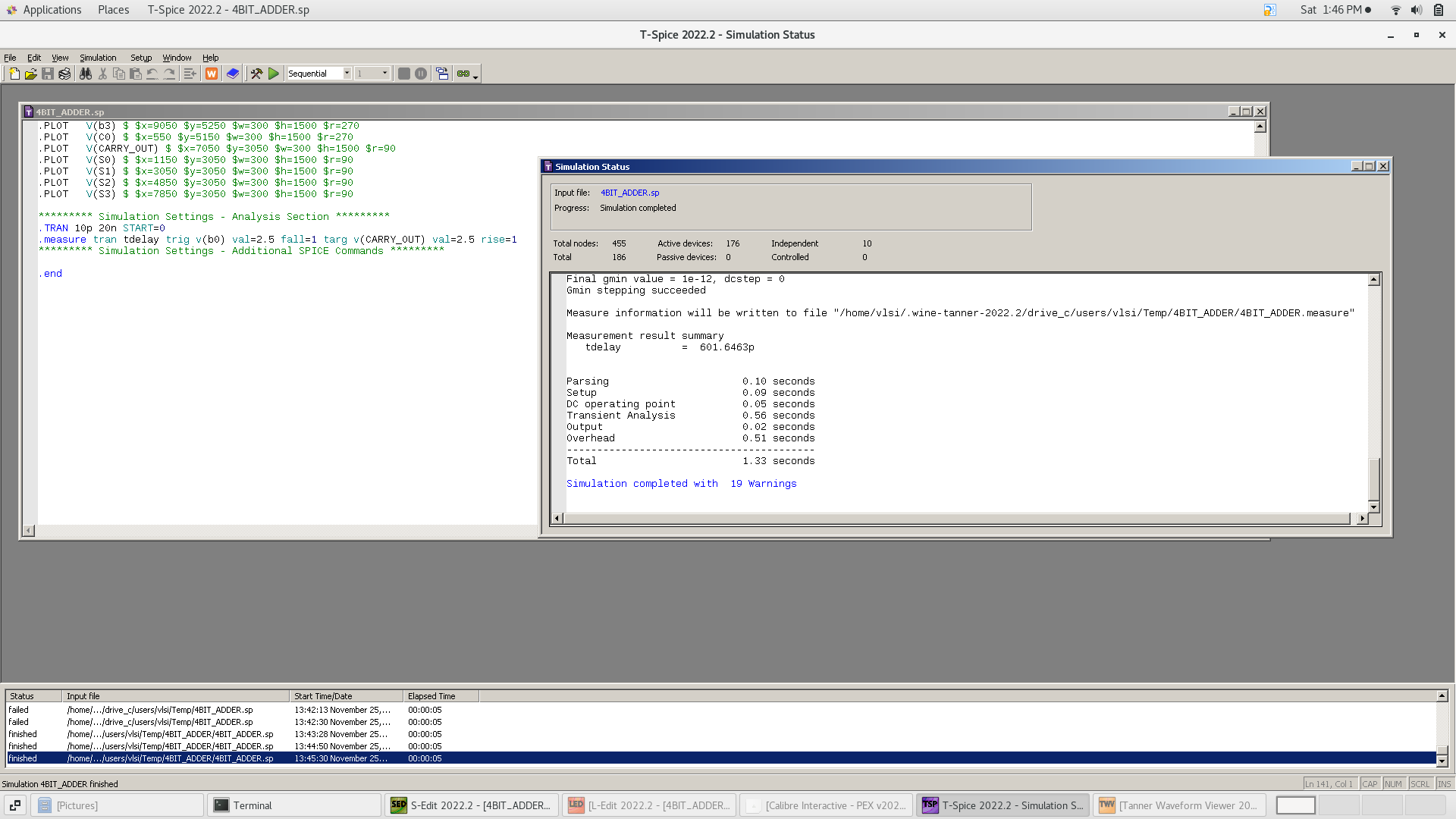
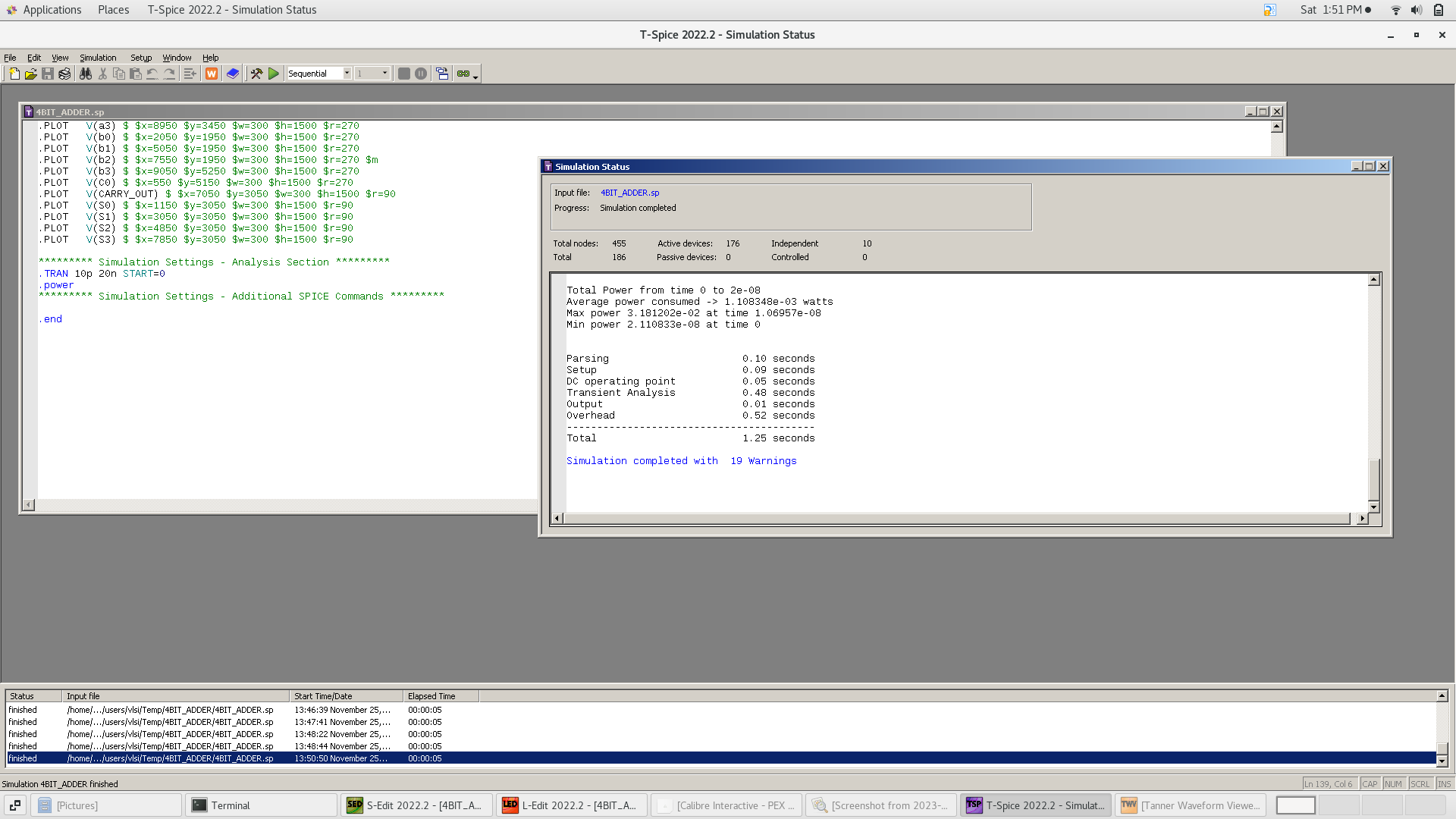
**🡺 first try** : adding pulse voltage sources to each input which are multiples from each others

As we show from the cursor : 0101 + 1110 +1 = 10100

**🡺 second try** : first try : adding known input pattern through v bit

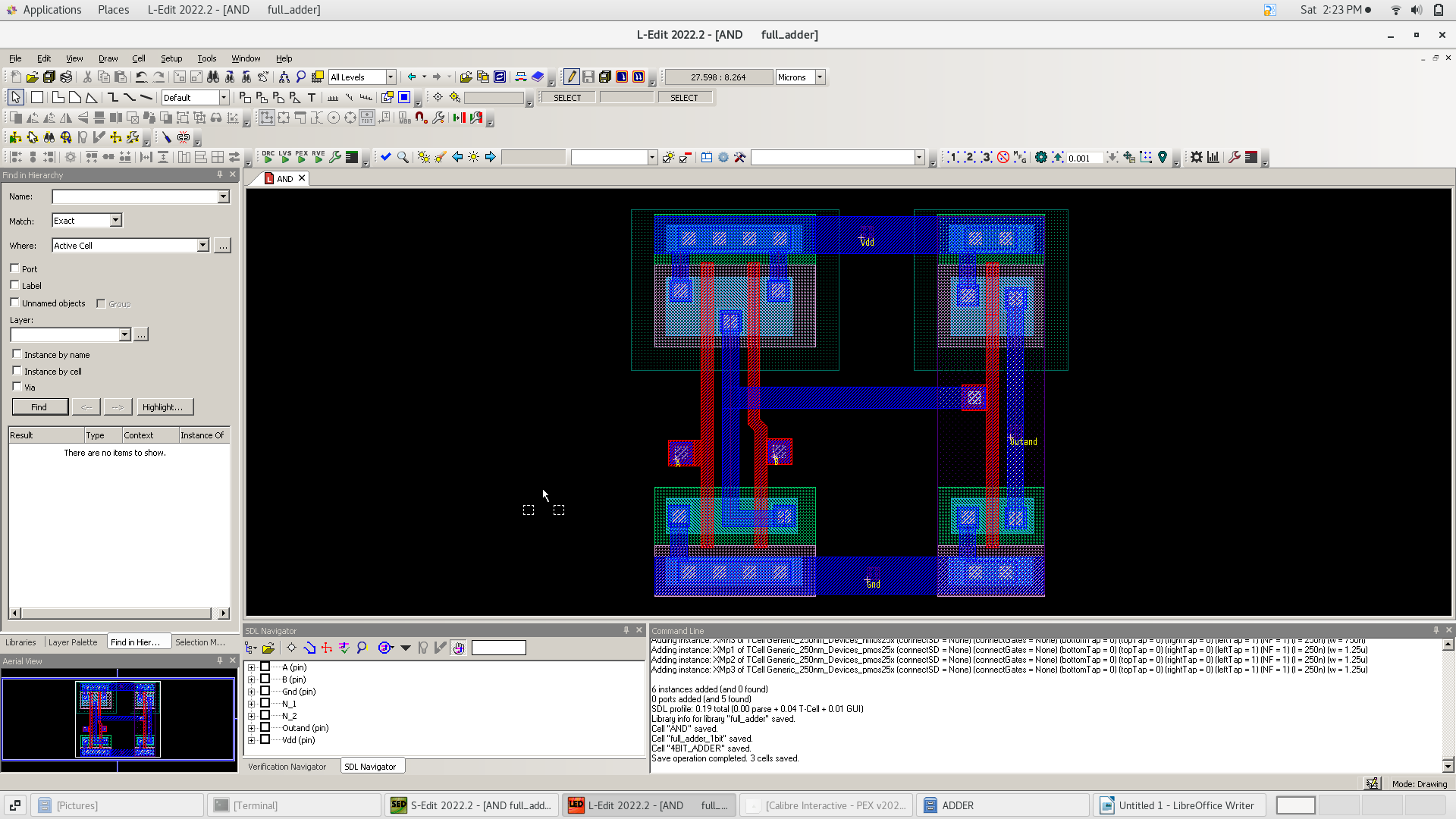
first pattern : 0101 + 1001 + 0 = 01110

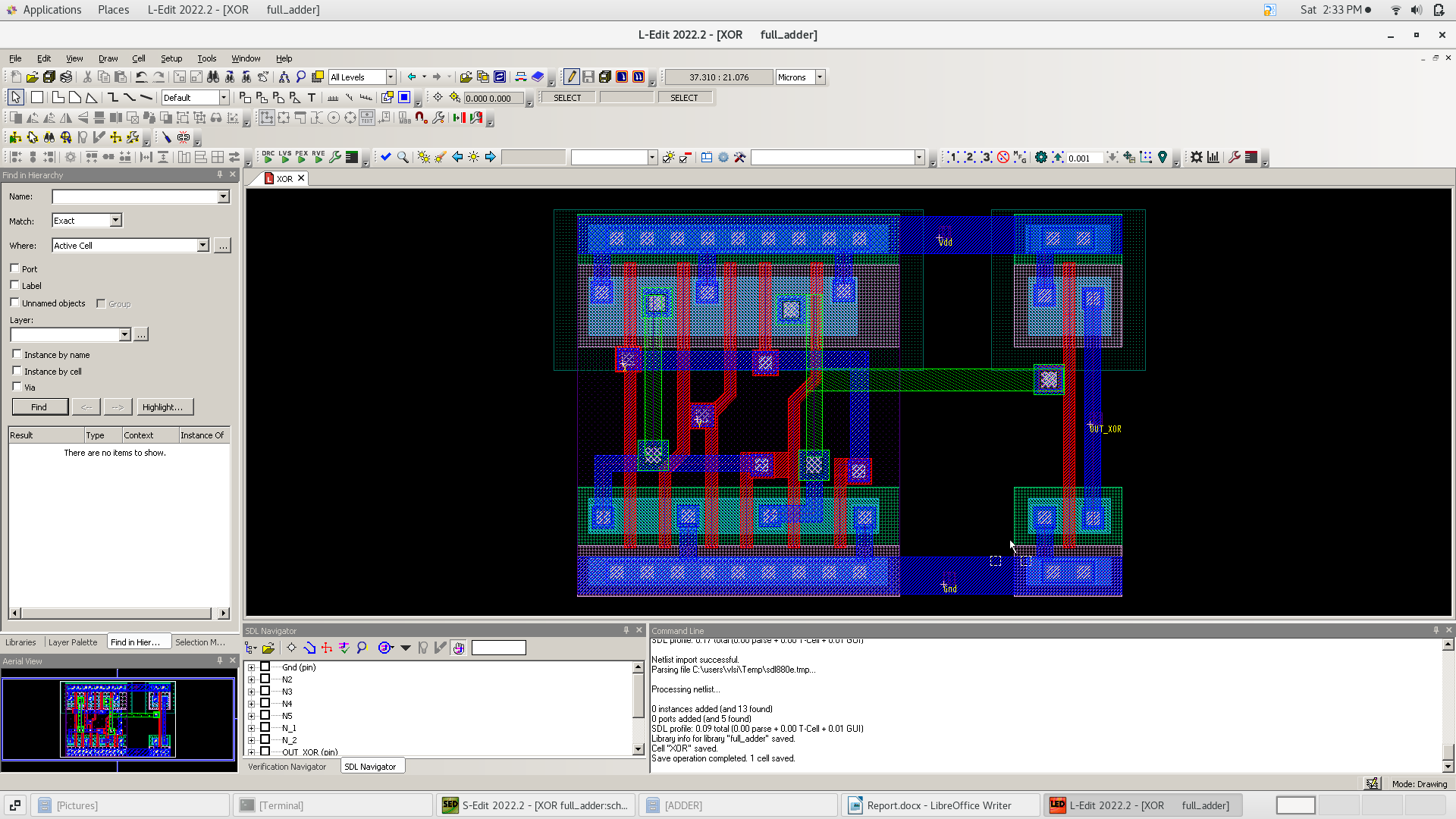
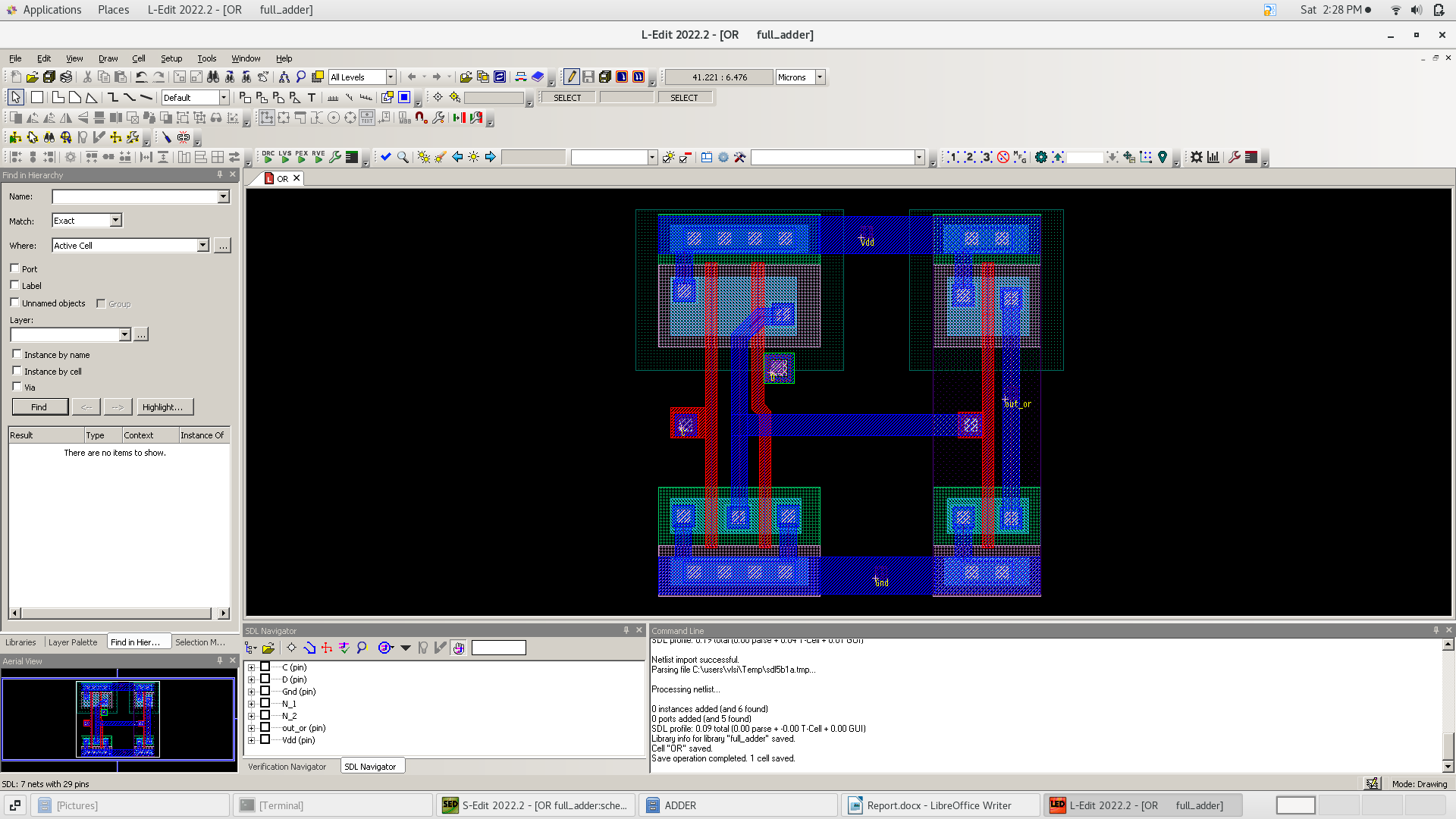
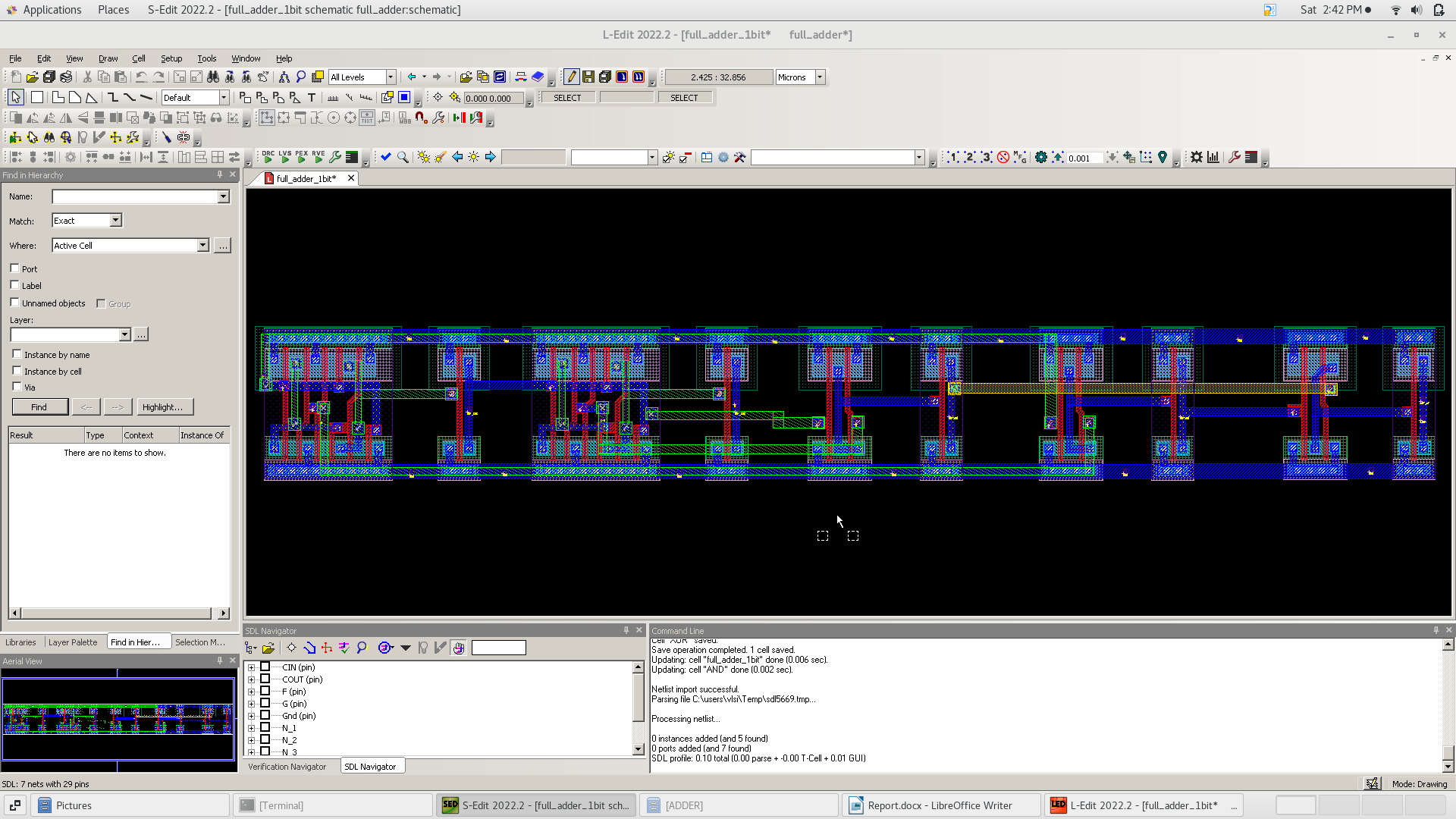
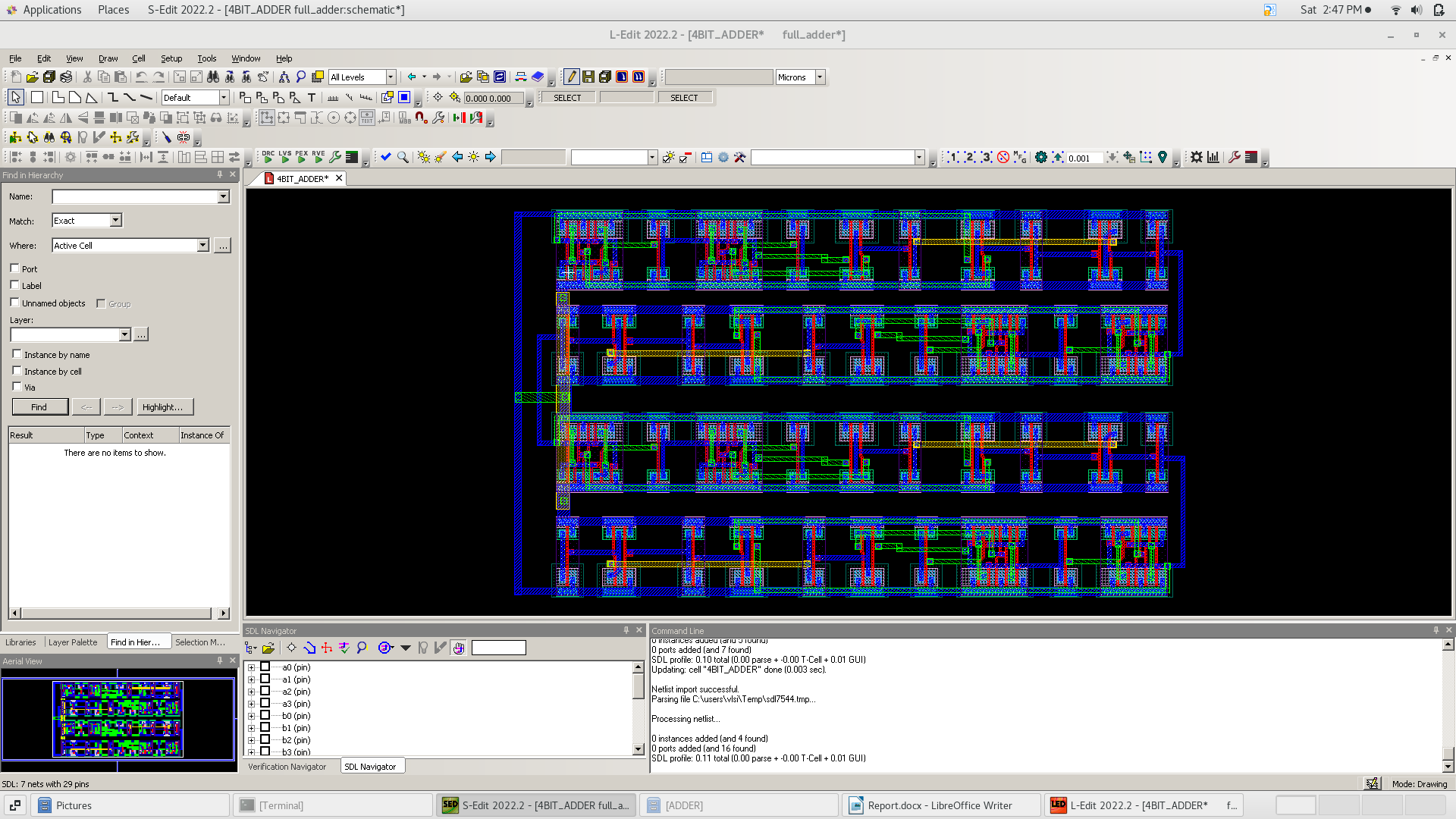
 second pattern : 0111 + 1100 + 0 = 10011

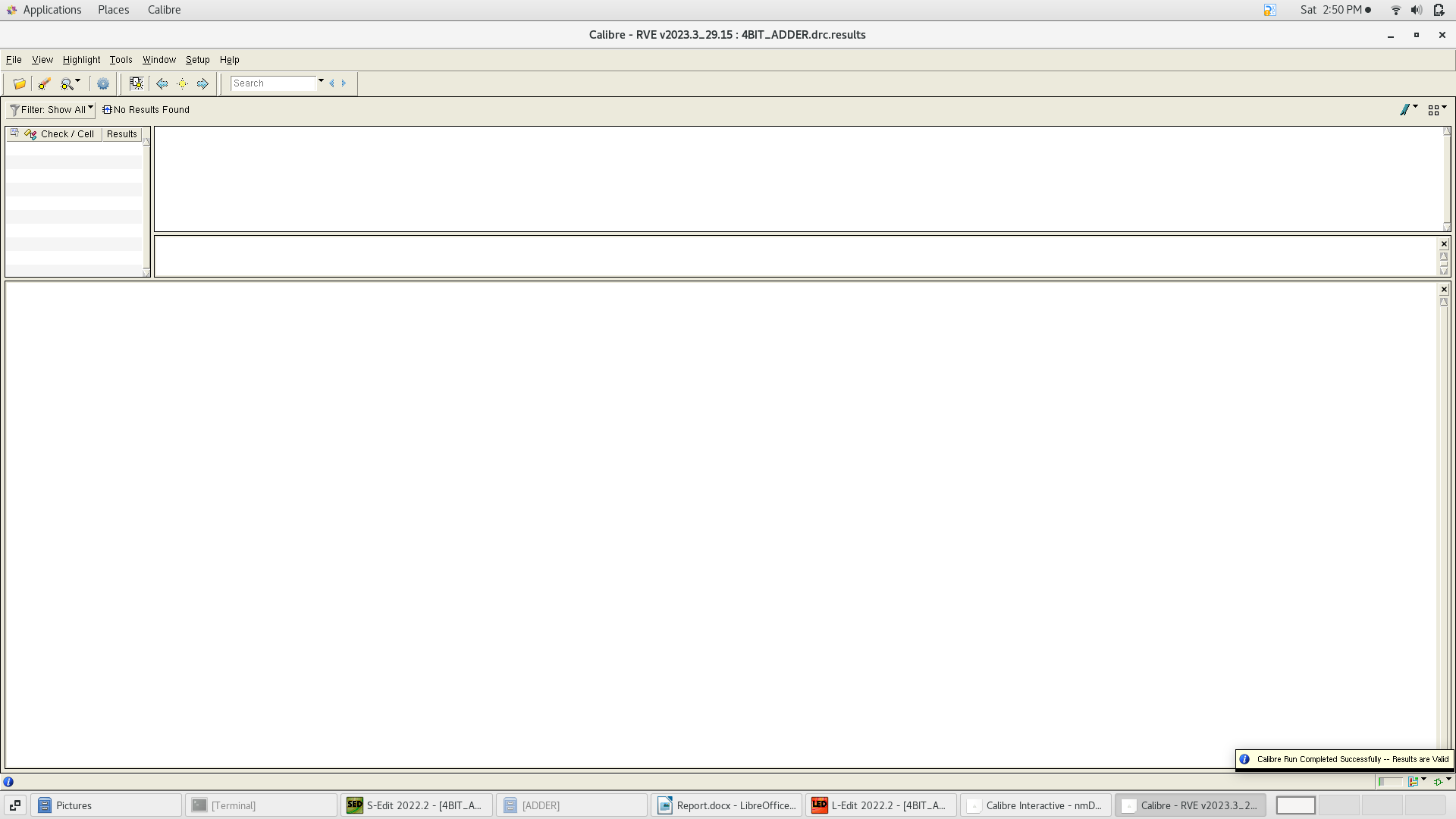
1. **Propagation Delay Calculation:** Worst case delay
2. **Power Calculations**
3. **Area**

Number of transistors = 100 Transistor

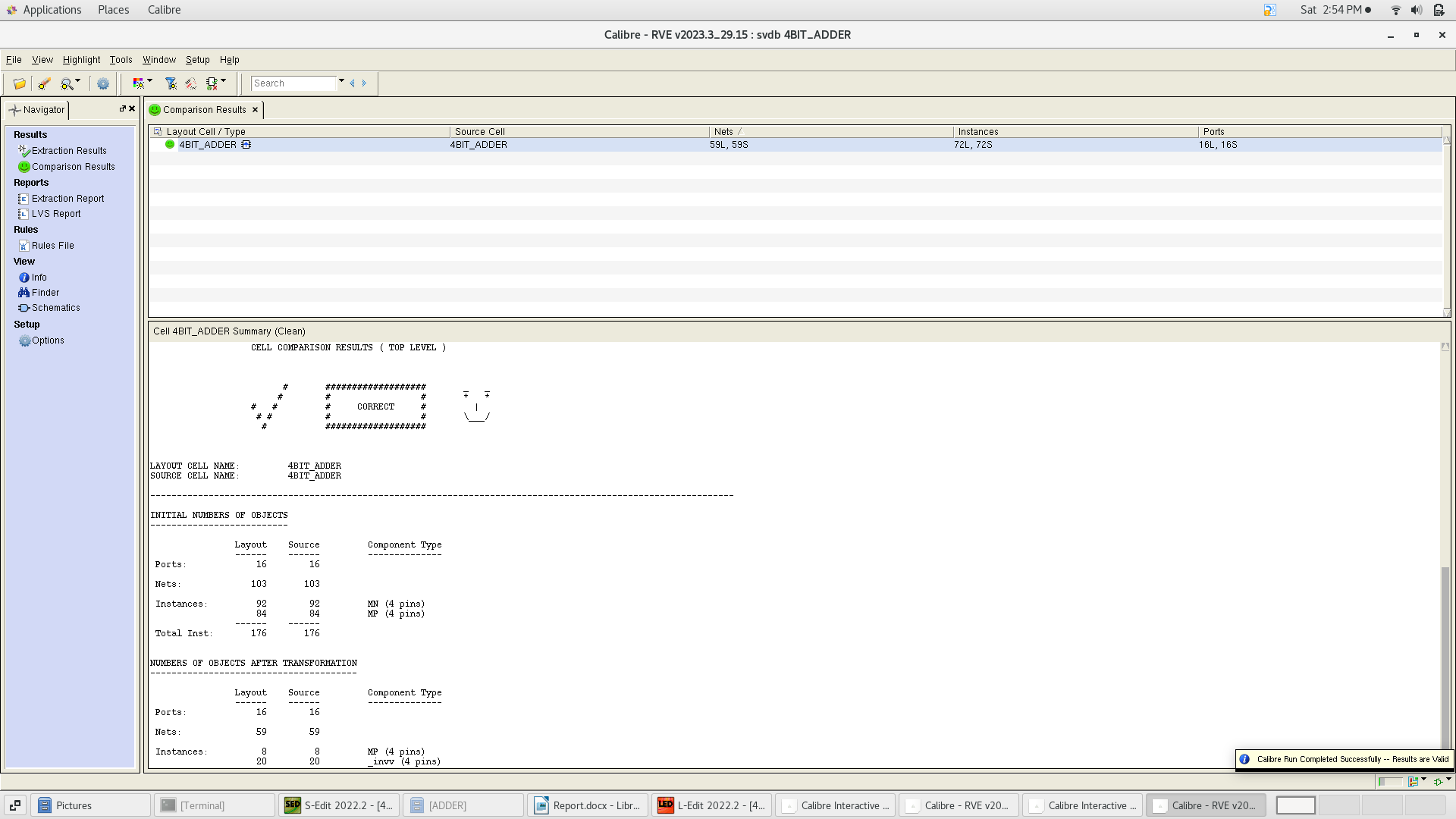
1. **AND Gate Layout**

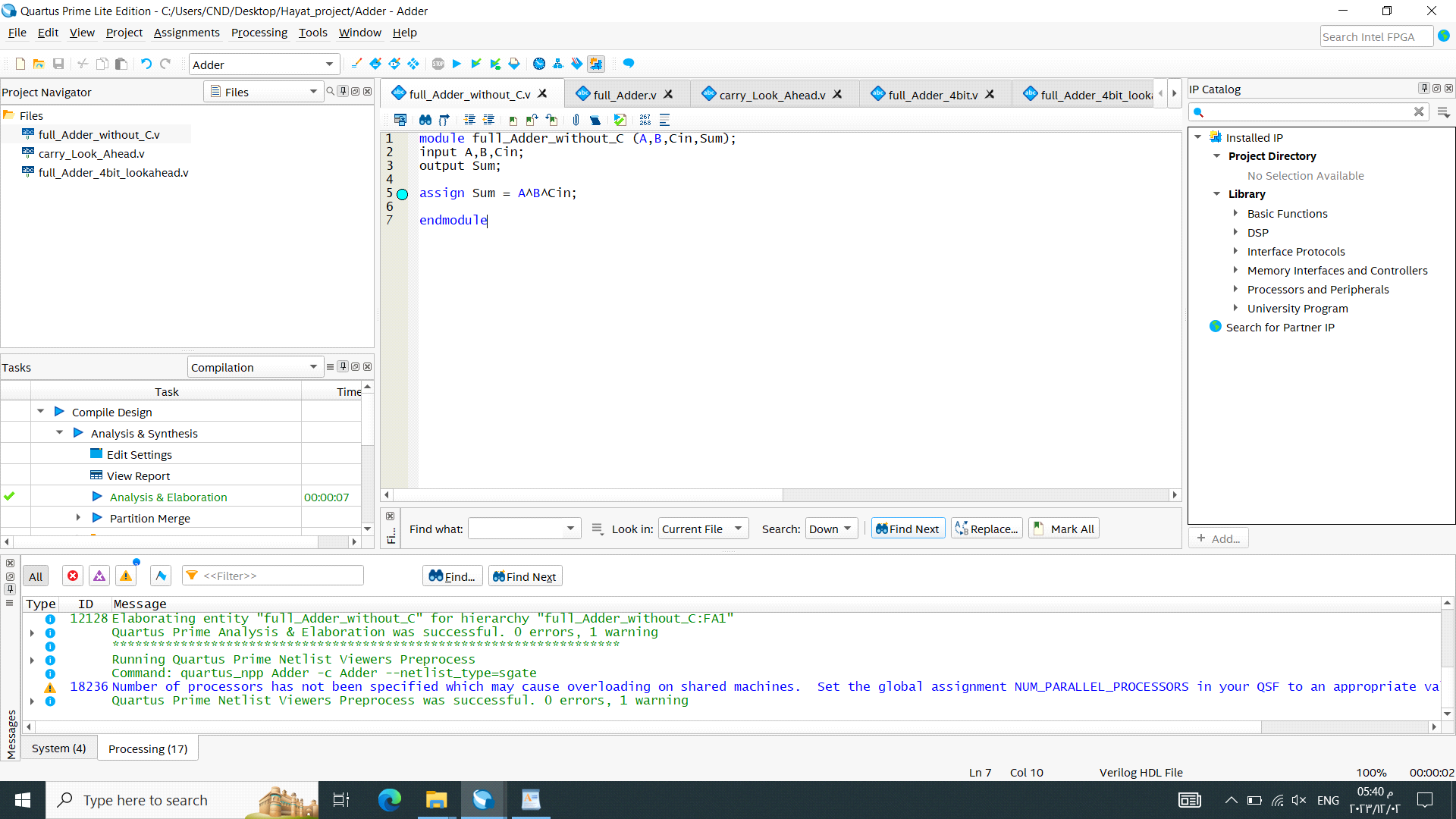
We made the layout for each block individually as hierarchy to make it easier

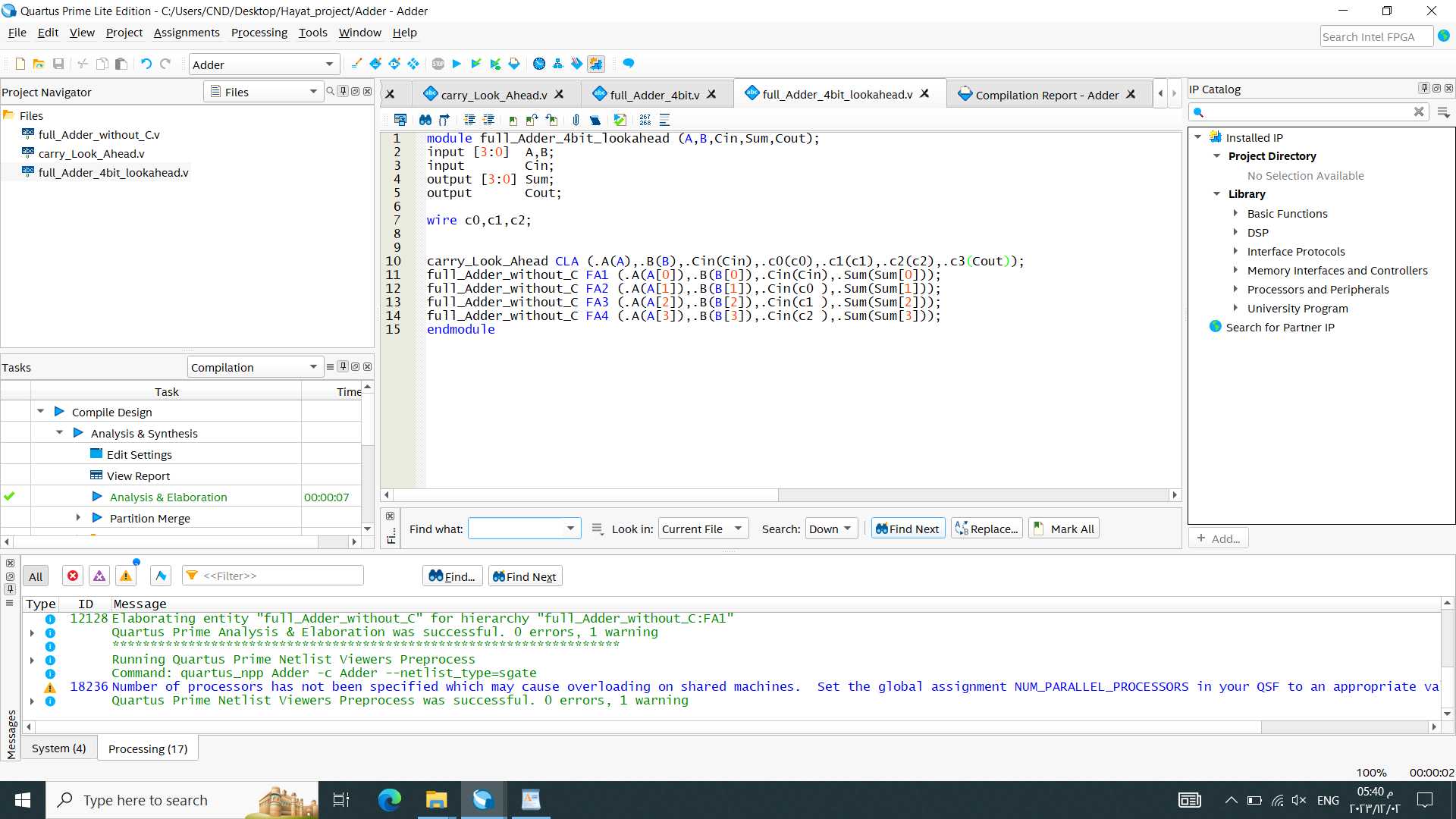
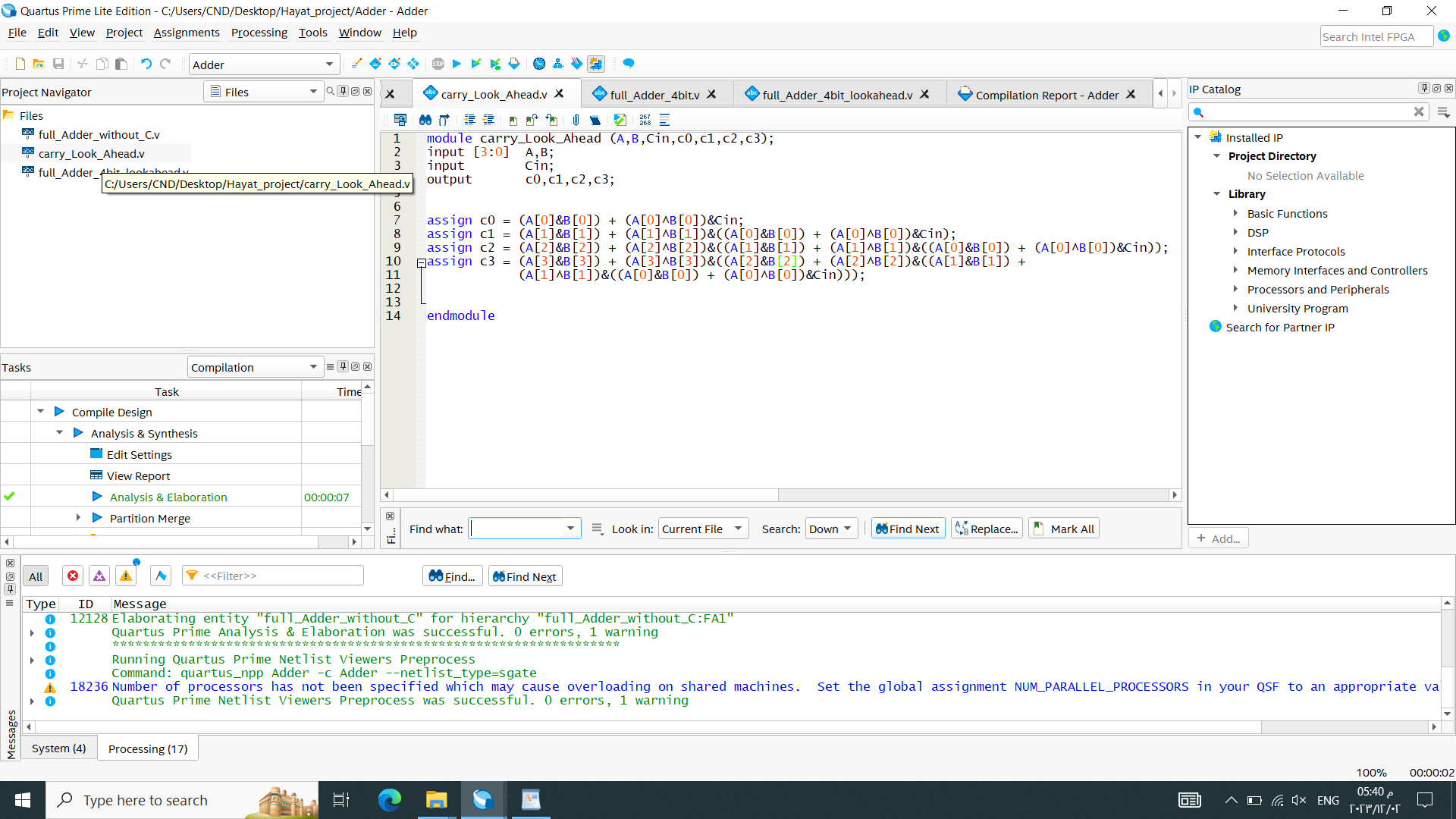
1. **OR Gate Layout**
2. **XOR Gate Layout**
3. **1-bit Full Adder Layout**
4. **4-bit Full Adder Layout**
5. **DRC Check**

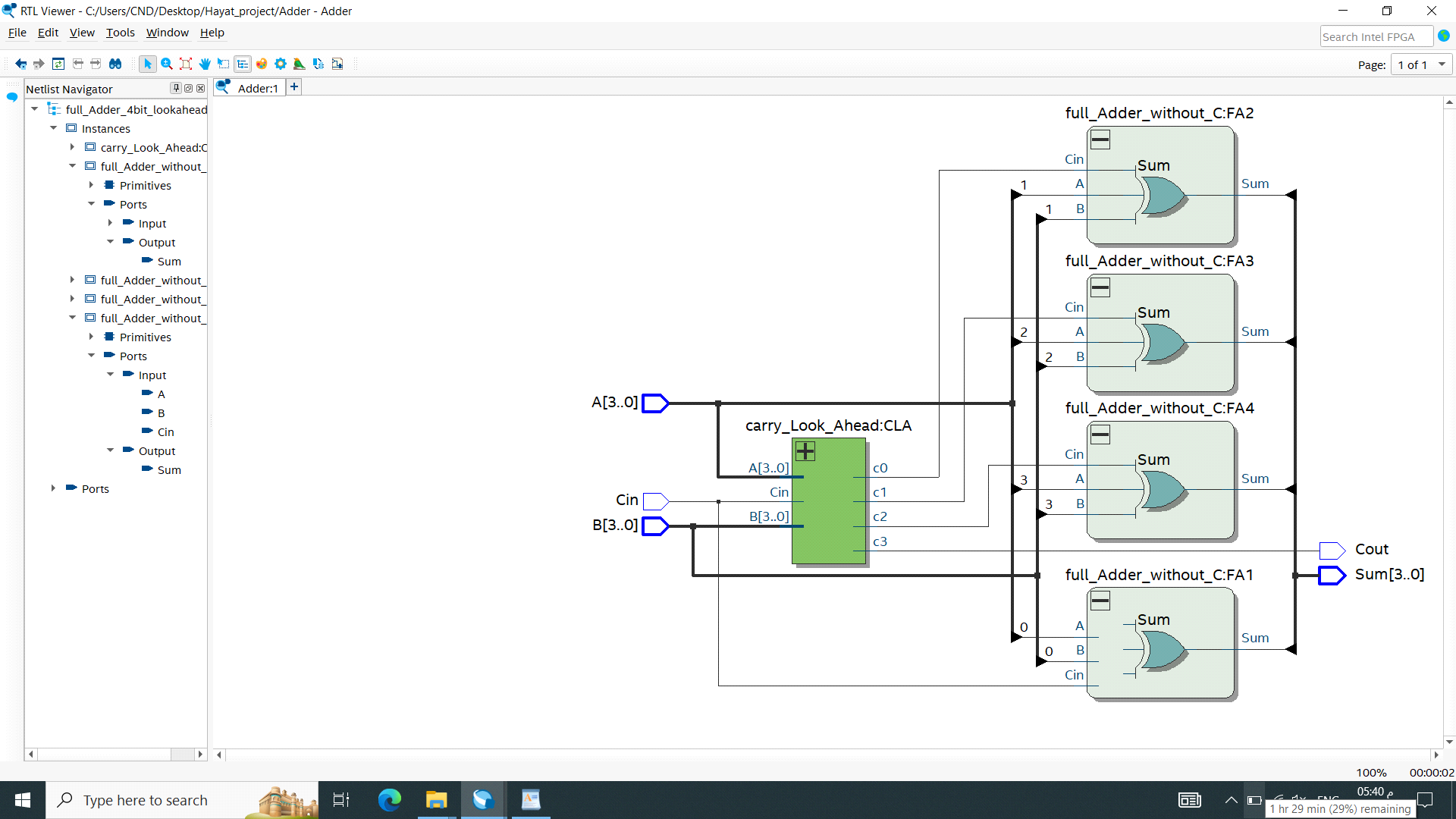
We did a DRC check for each block layout to make sure that there is no any design rule violation and there is the DRC of whole design

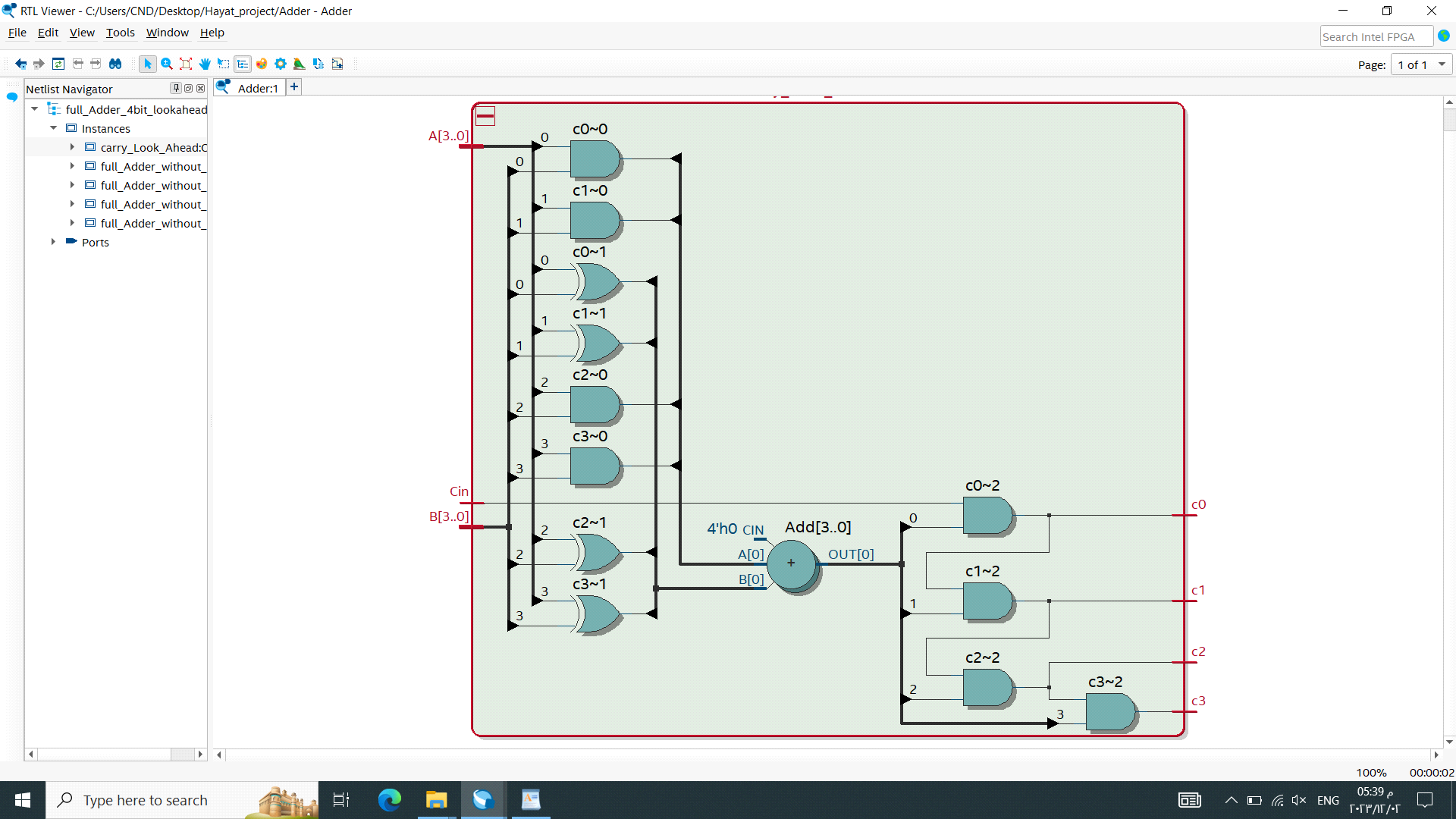
1. **LVS Check**

the final step is to do the LVS to check that the layout is identical to the schematic

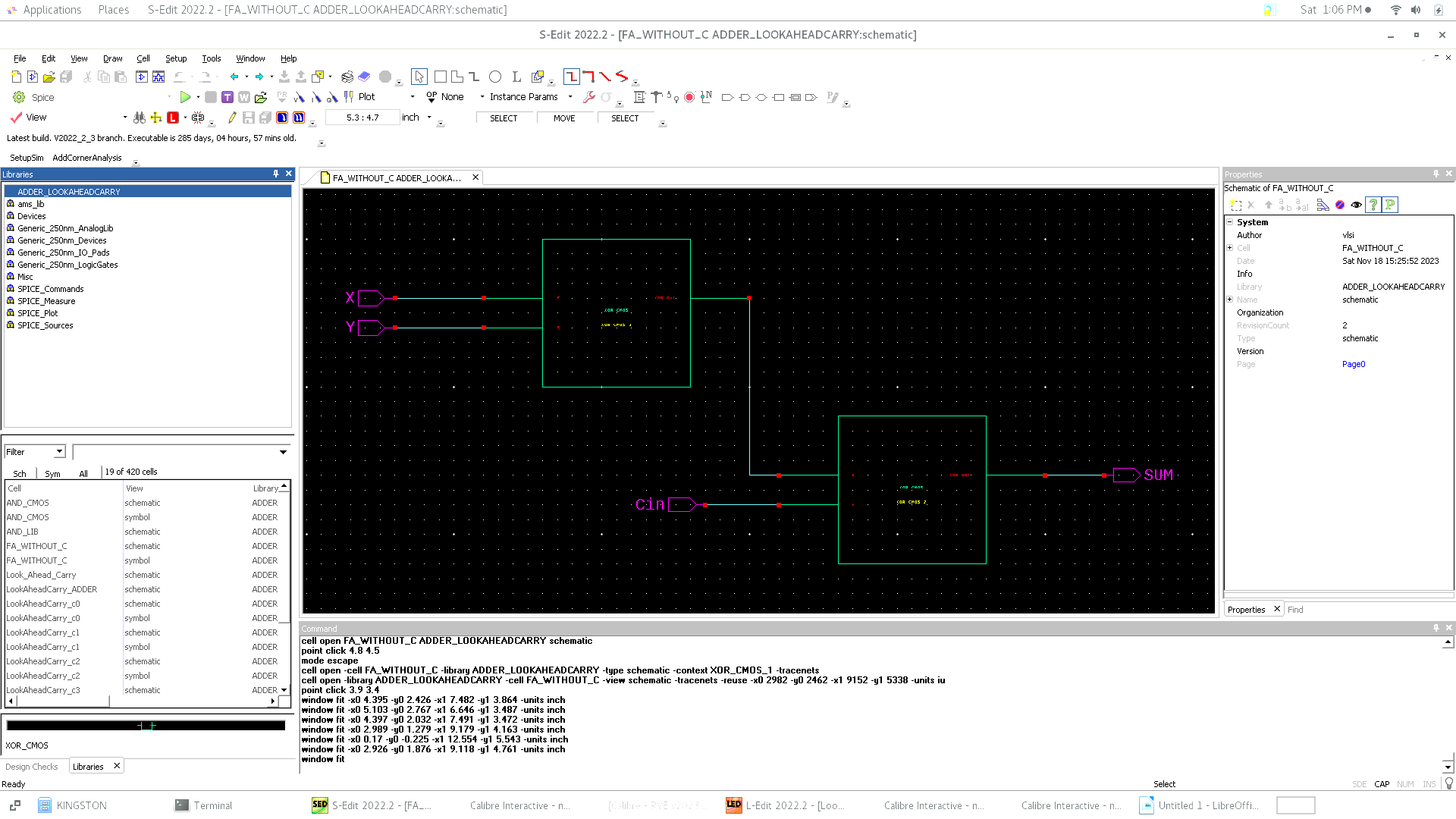
1. **Carry LookAhead:**
2. **RTL**



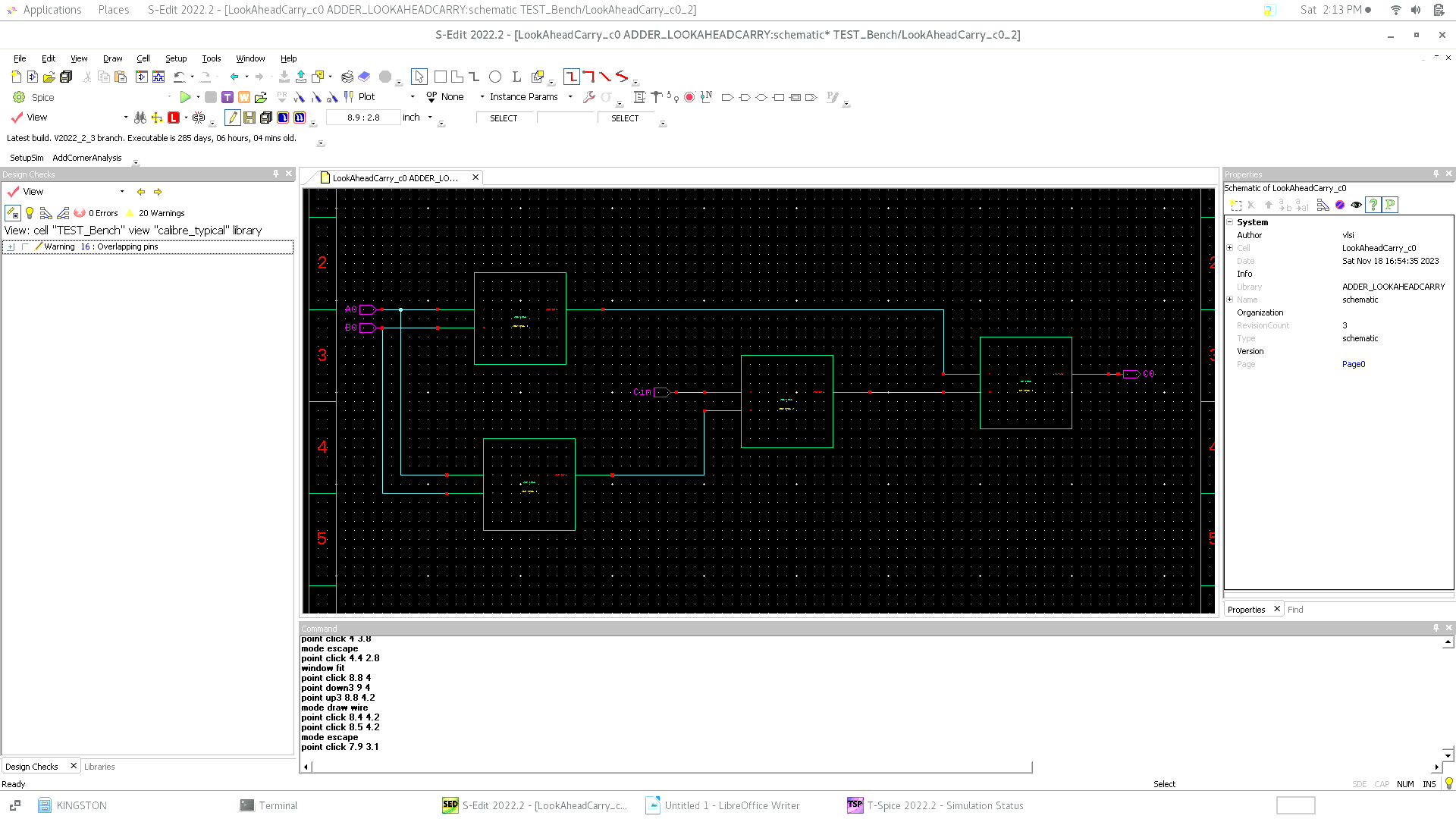
1. **Output netlist**

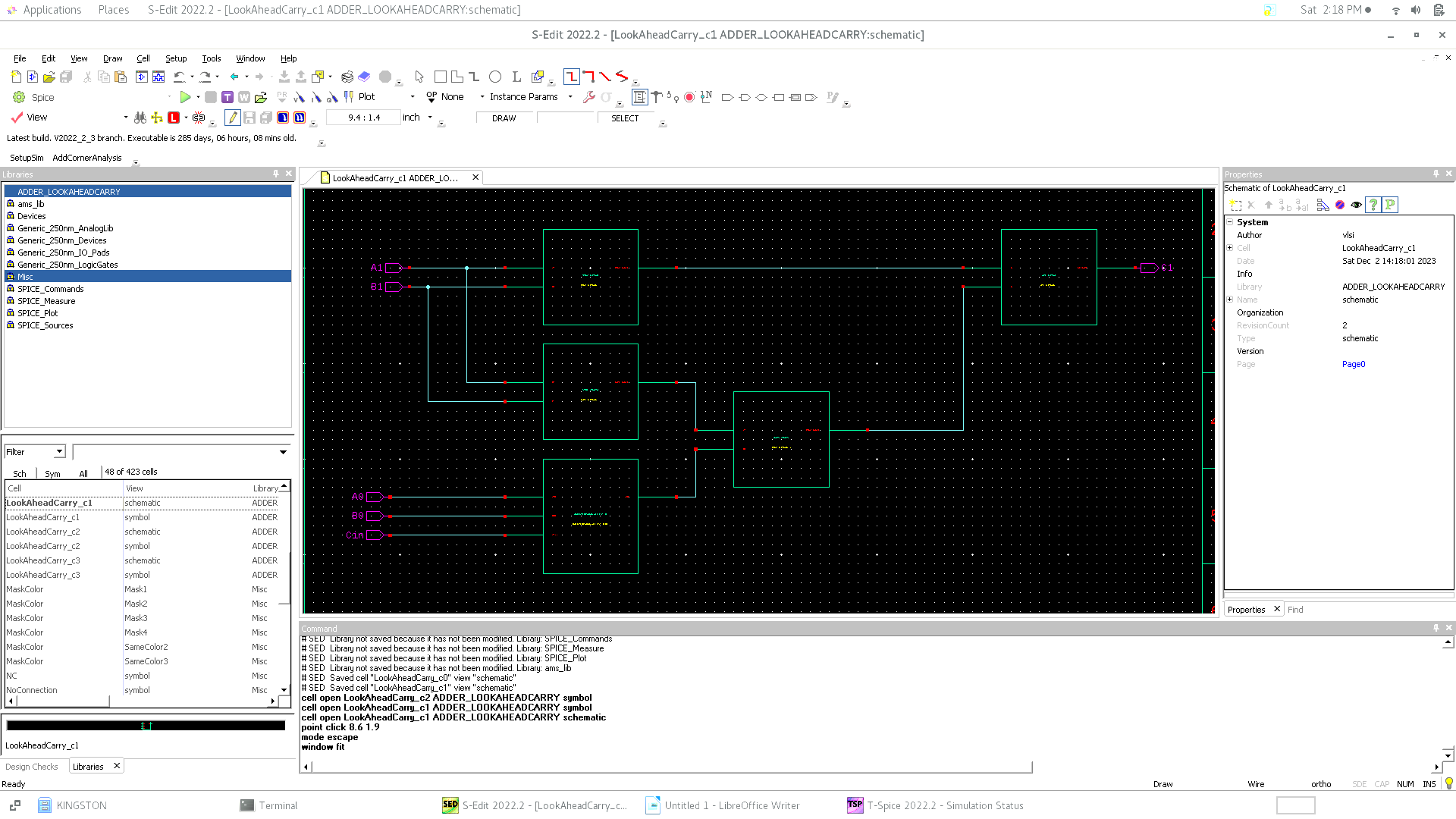
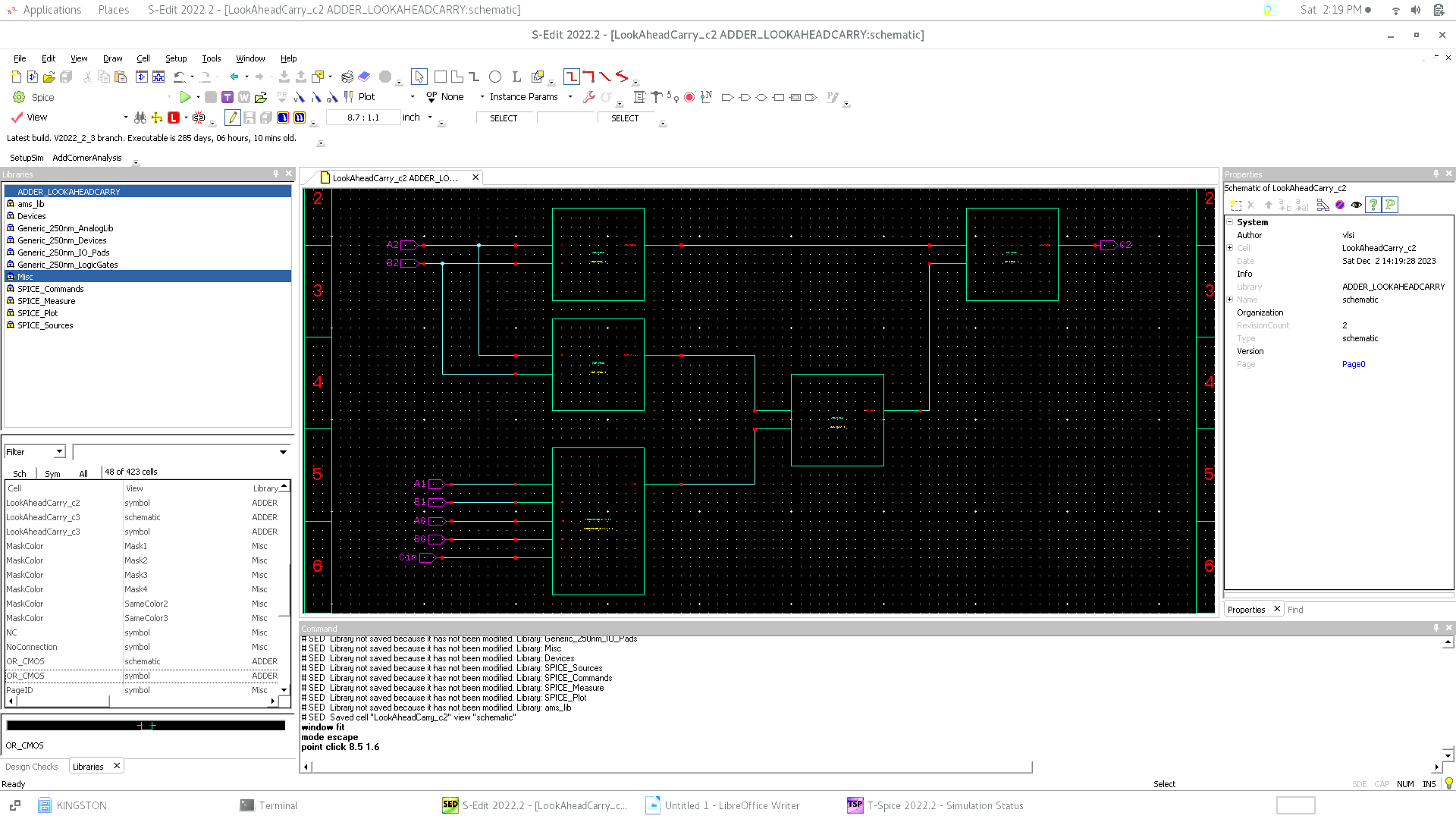
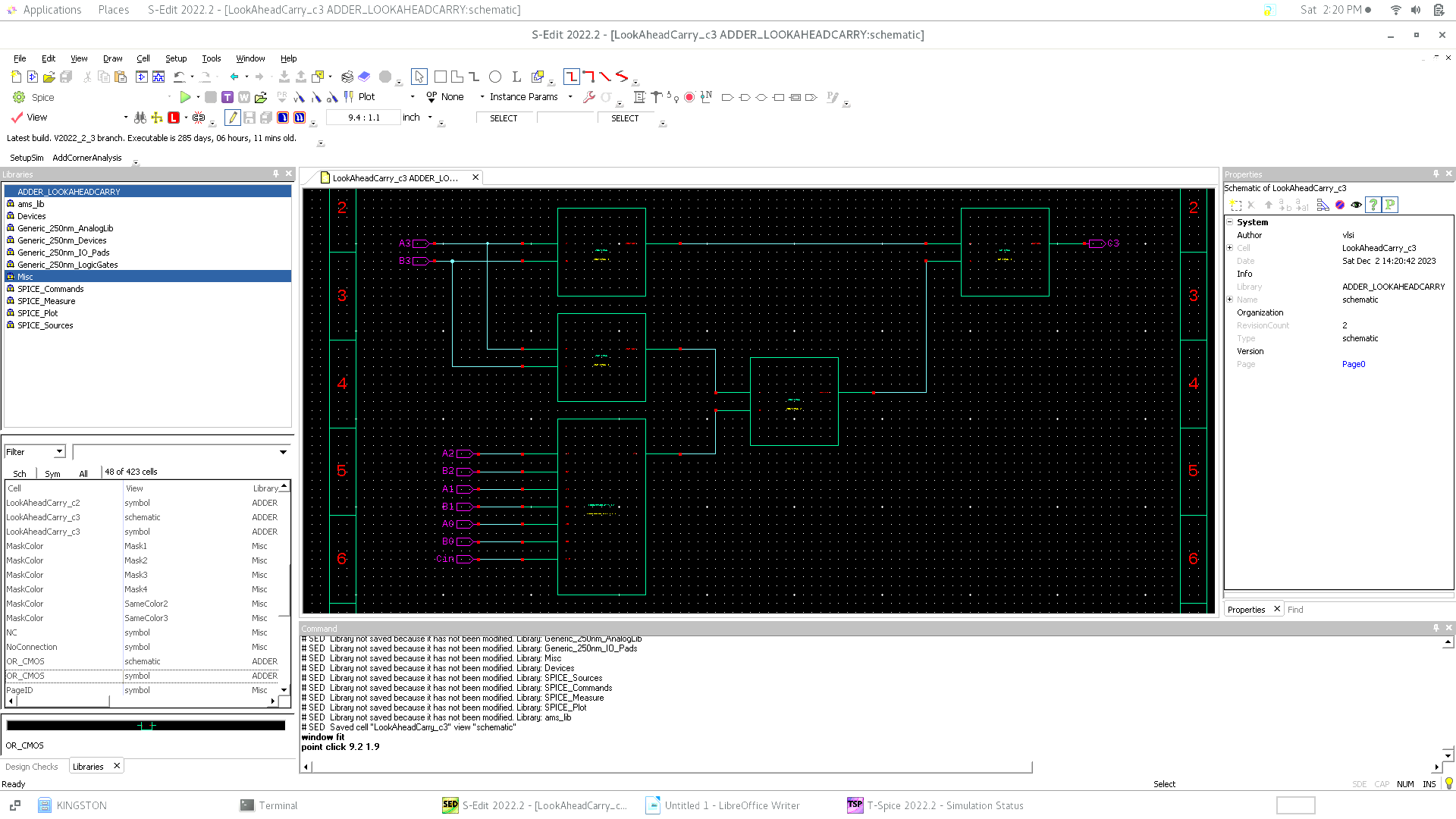
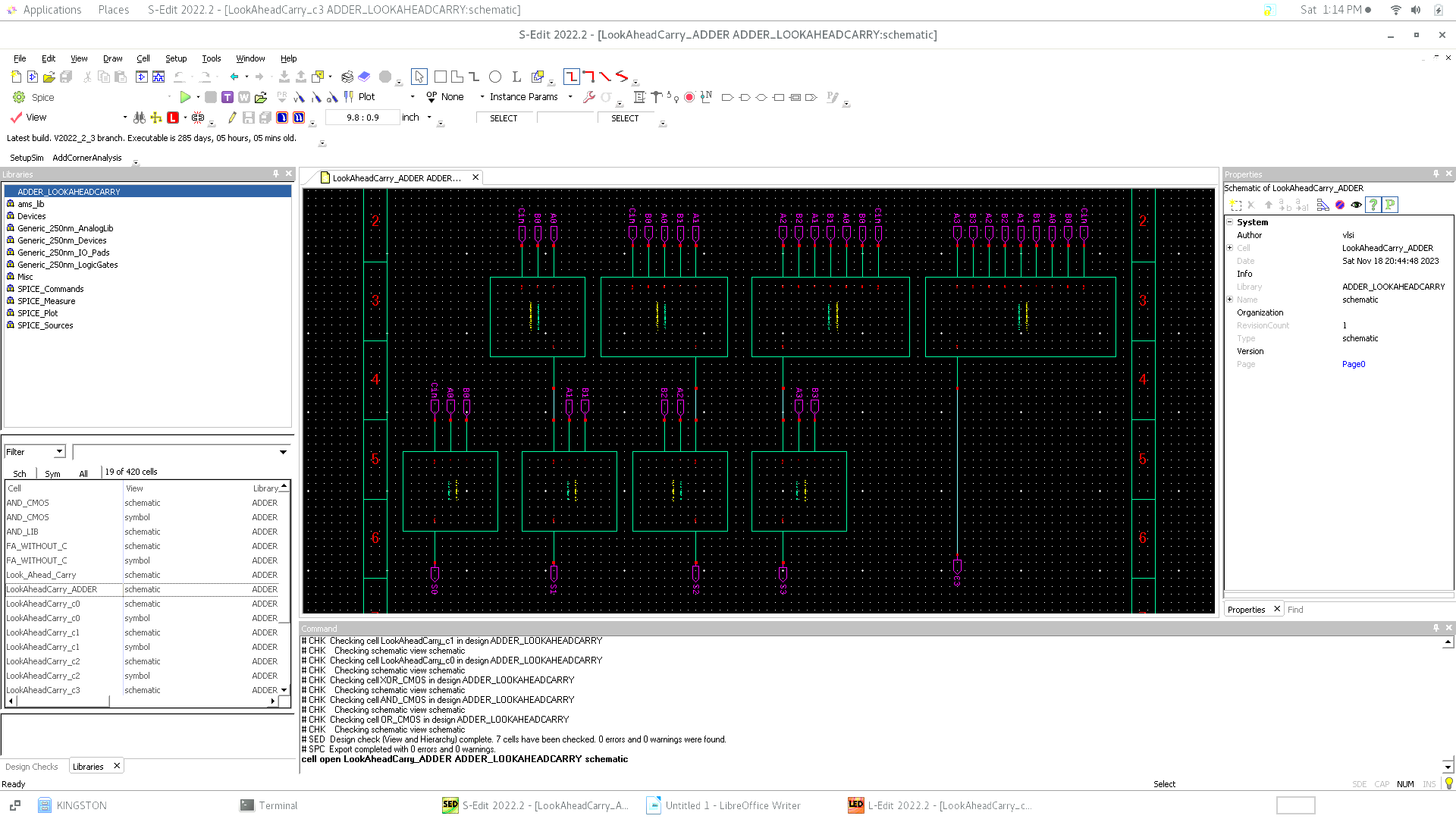
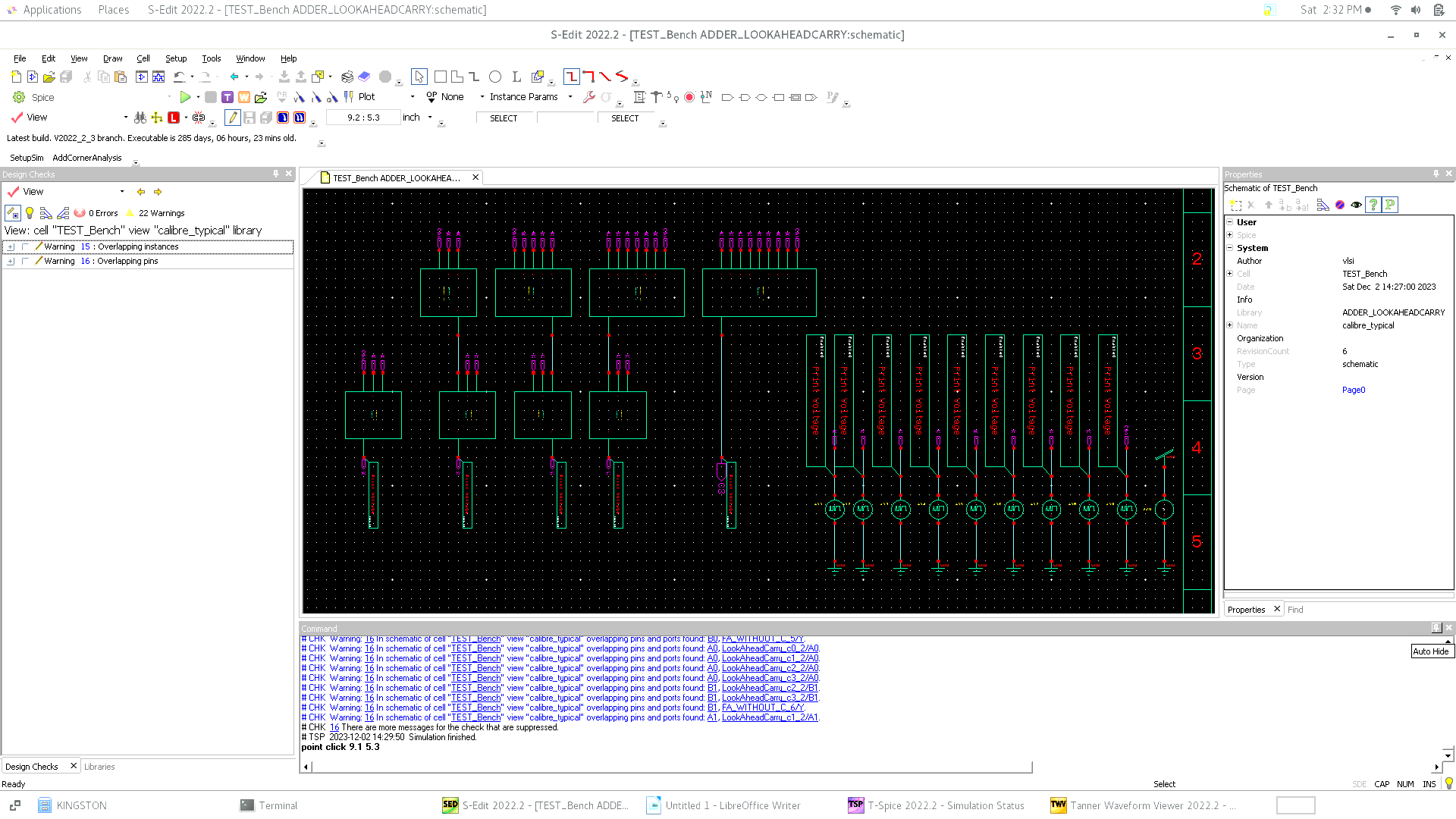


1. **1-bit Full Adder Schematic**

we used the same basic circuits that we made for Ripple Carry Adder (AND, OR, XOR)

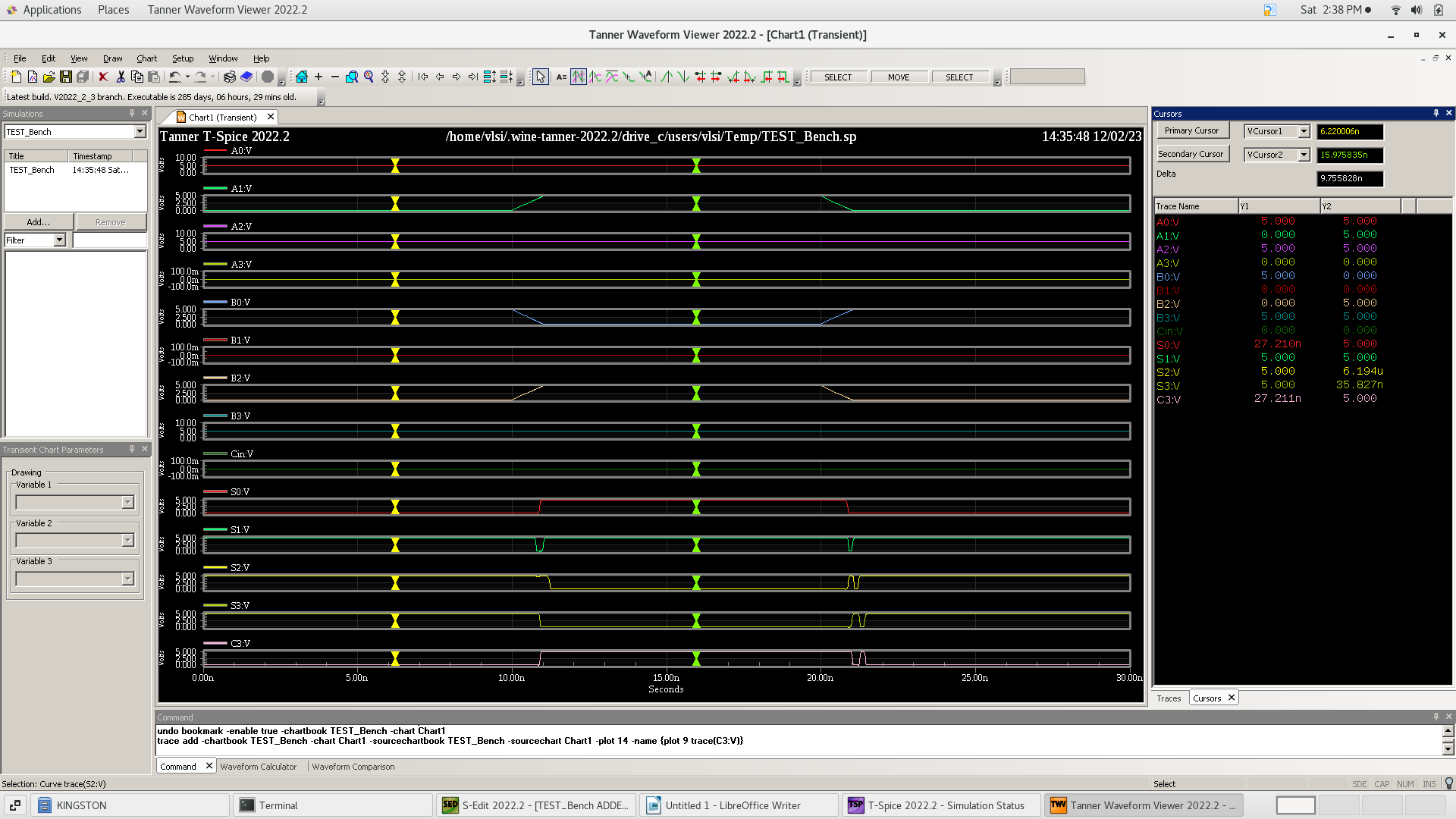
1. **Carry LookAhead Schematic for C0**

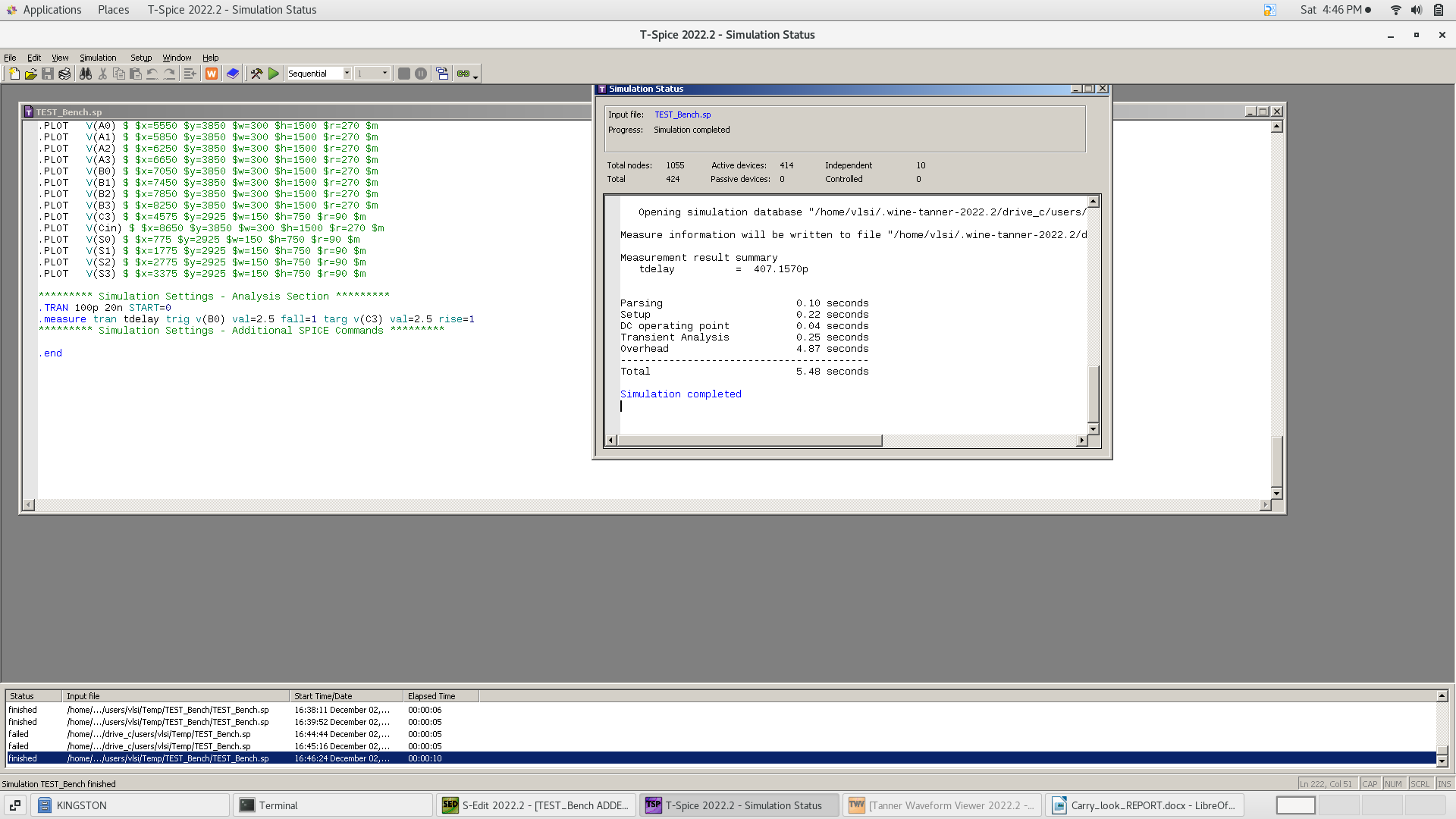
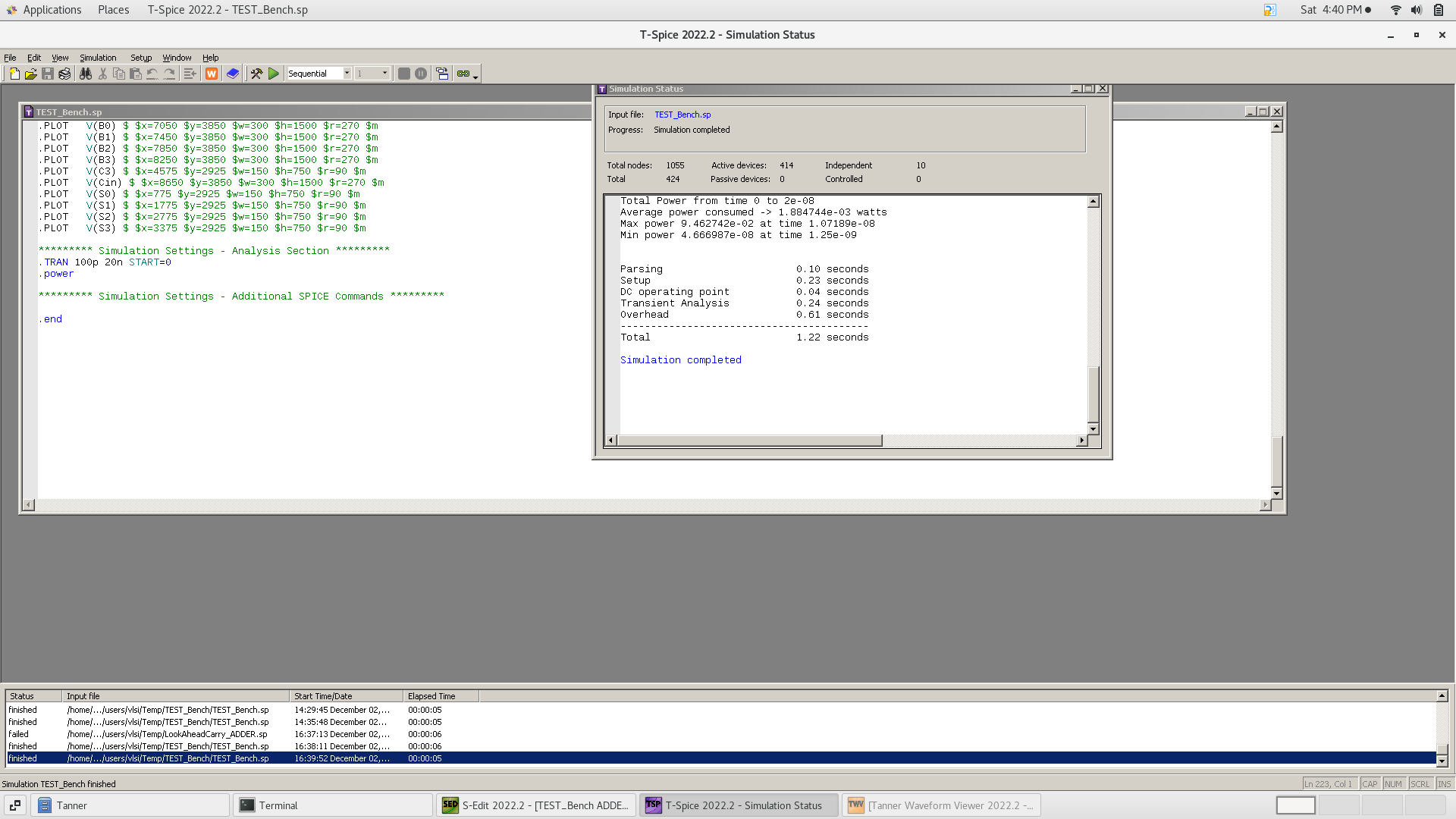


1. **Carry LookAhead Schematic for C1**
2. **Carry LookAhead Schematic for C2**
3. **Carry LookAhead Schematic for C3**
4. **4-bit Adder with Carry LookAhead**
5. **Test Bench of Ripple Carry Adder**
6. **Simulation results**

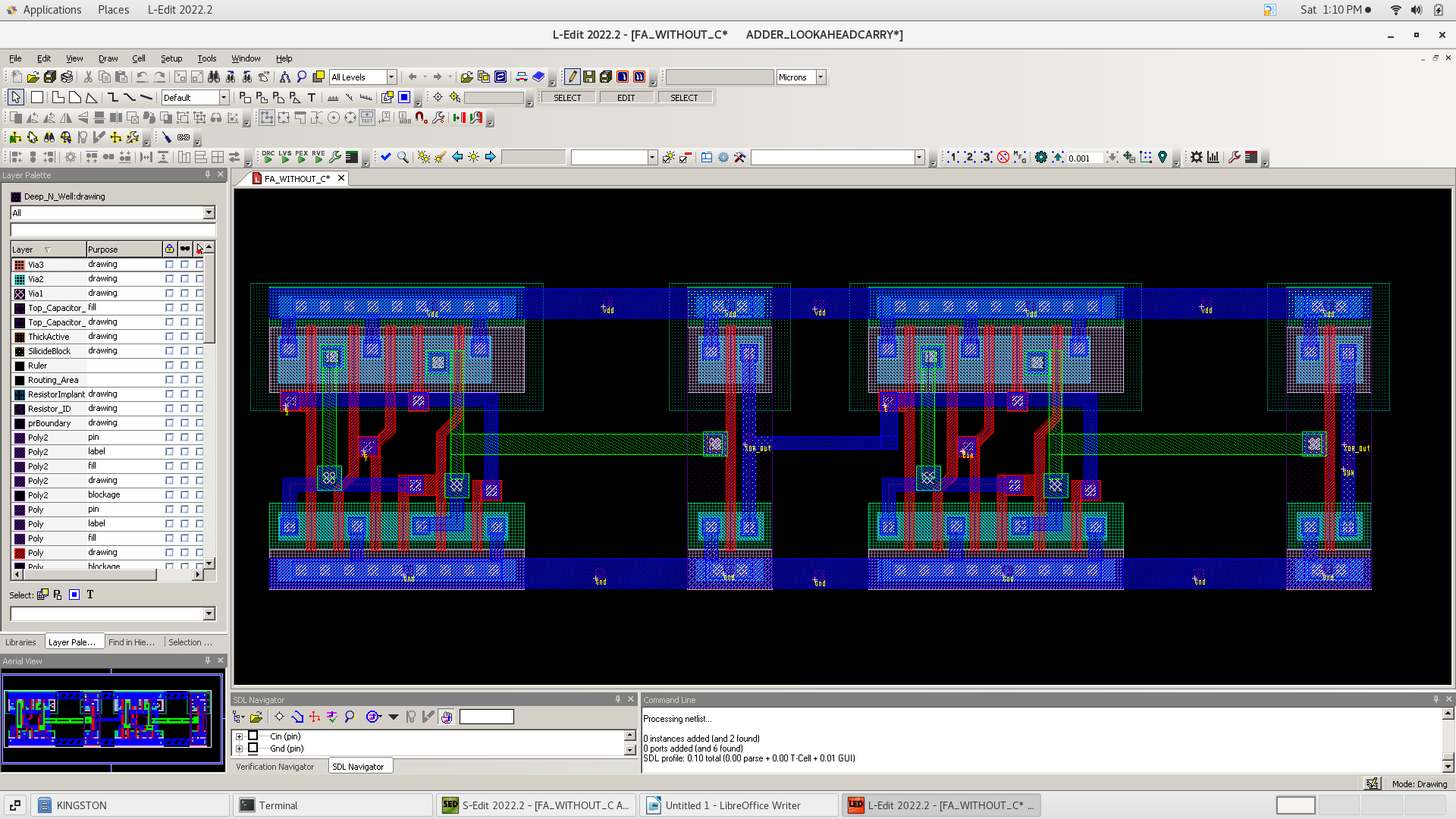
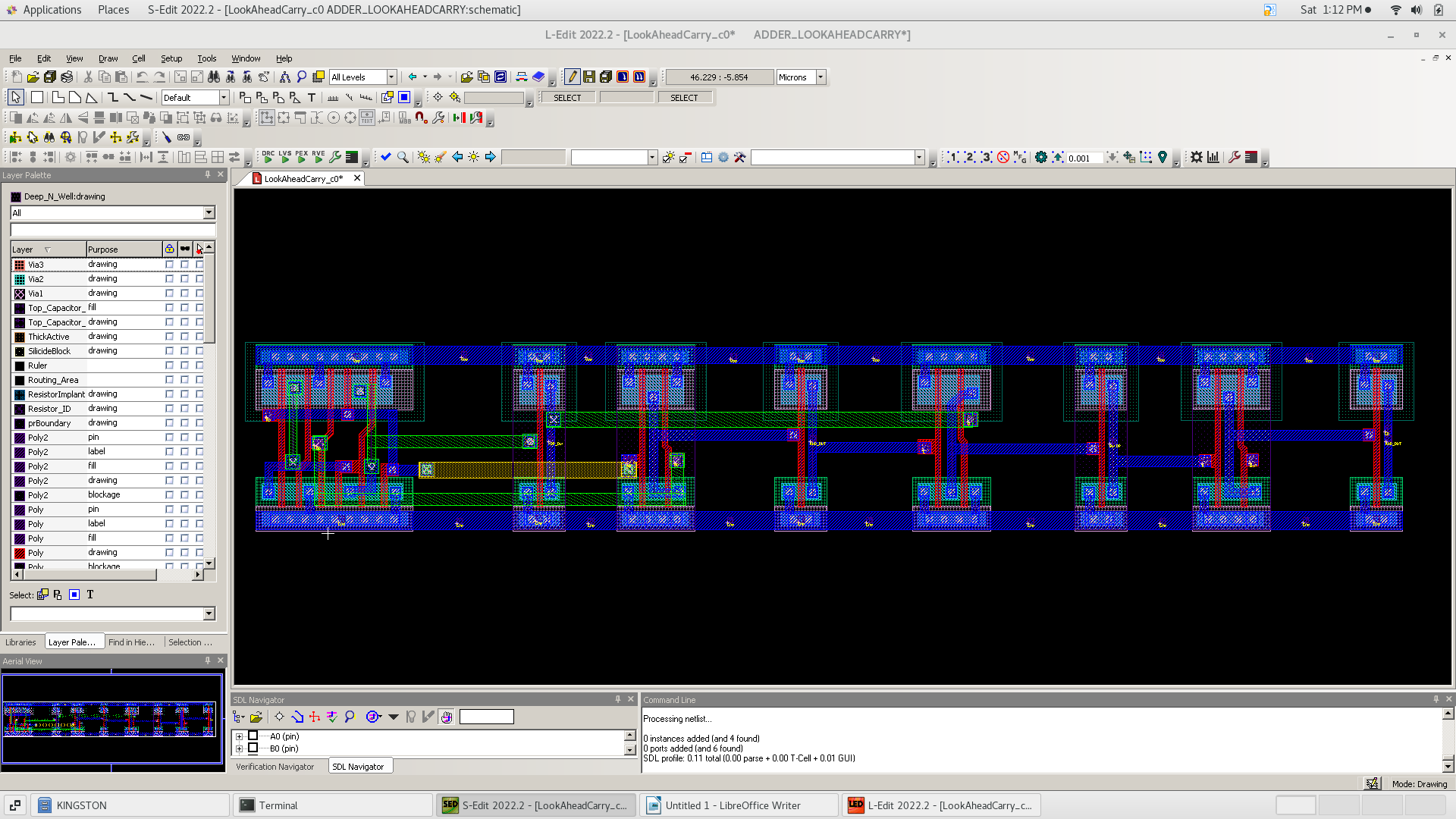
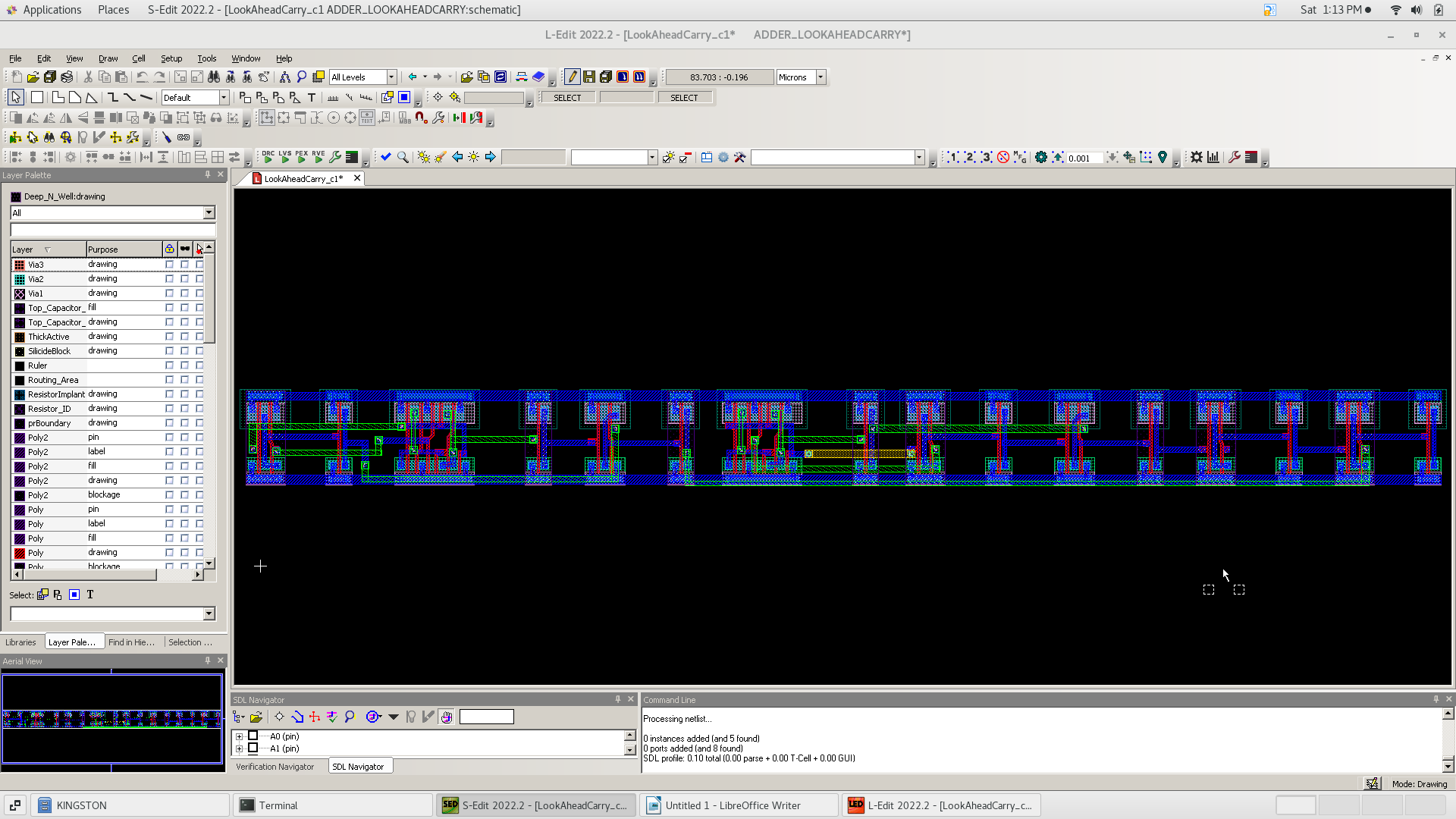
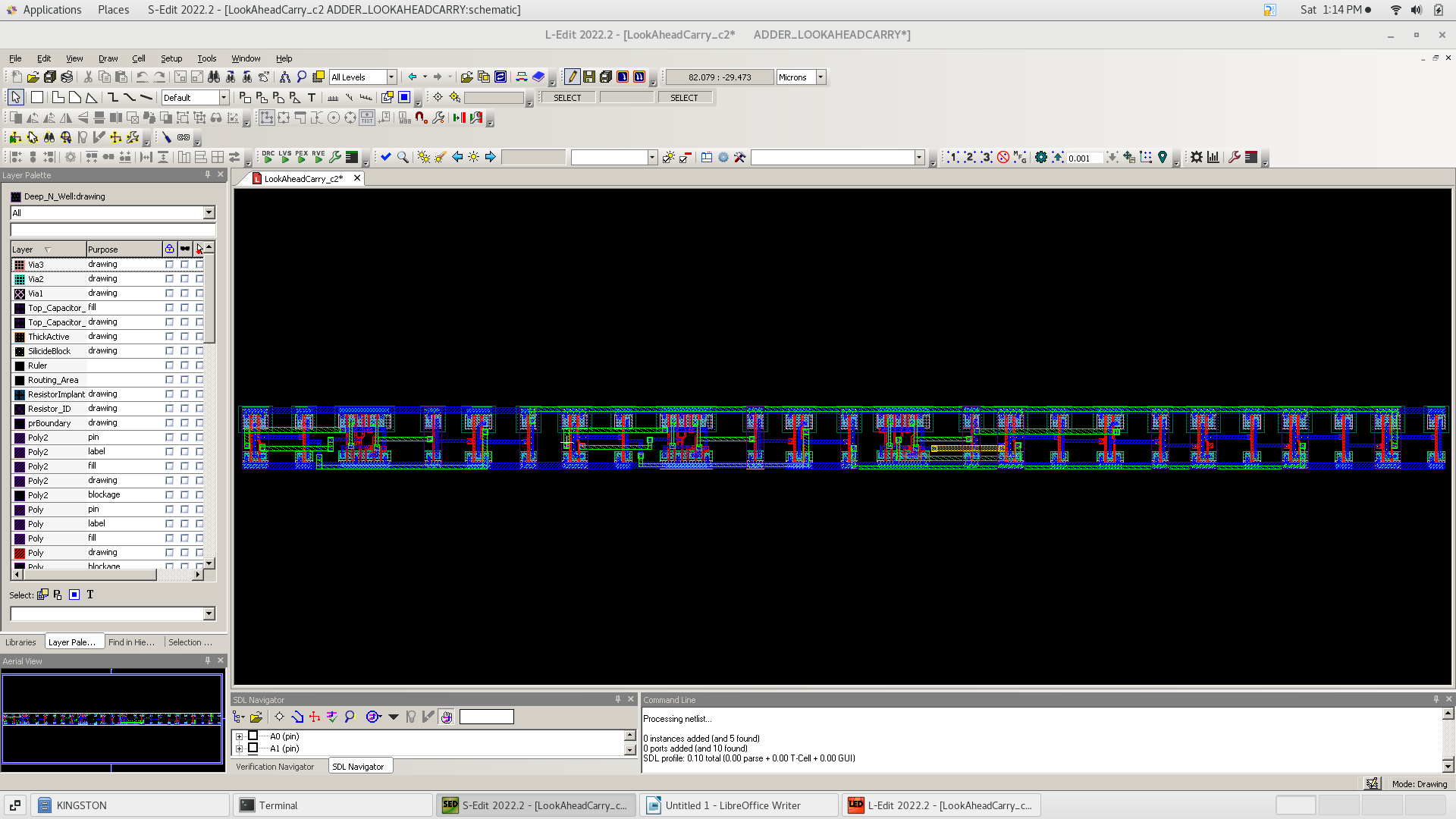
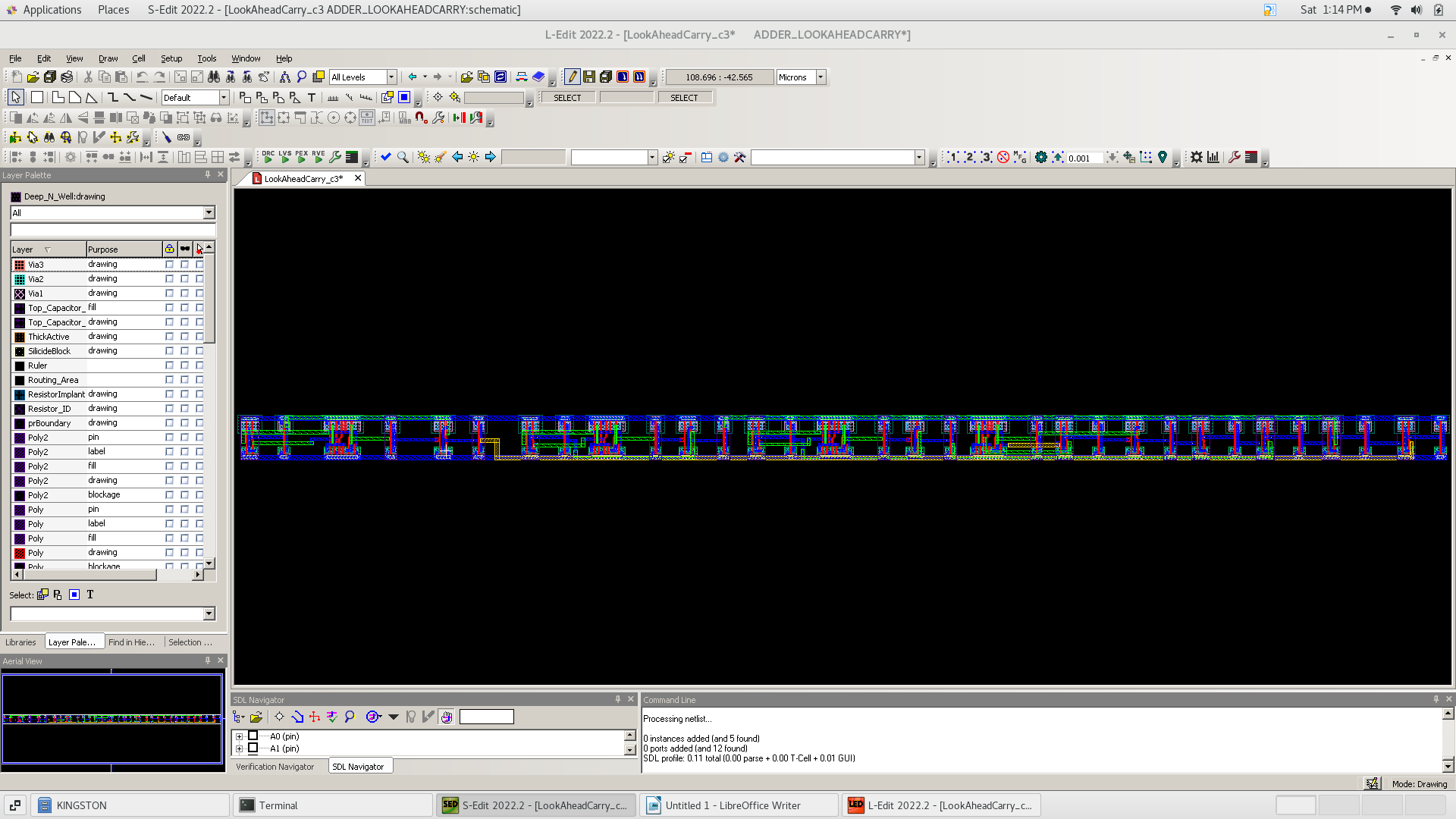
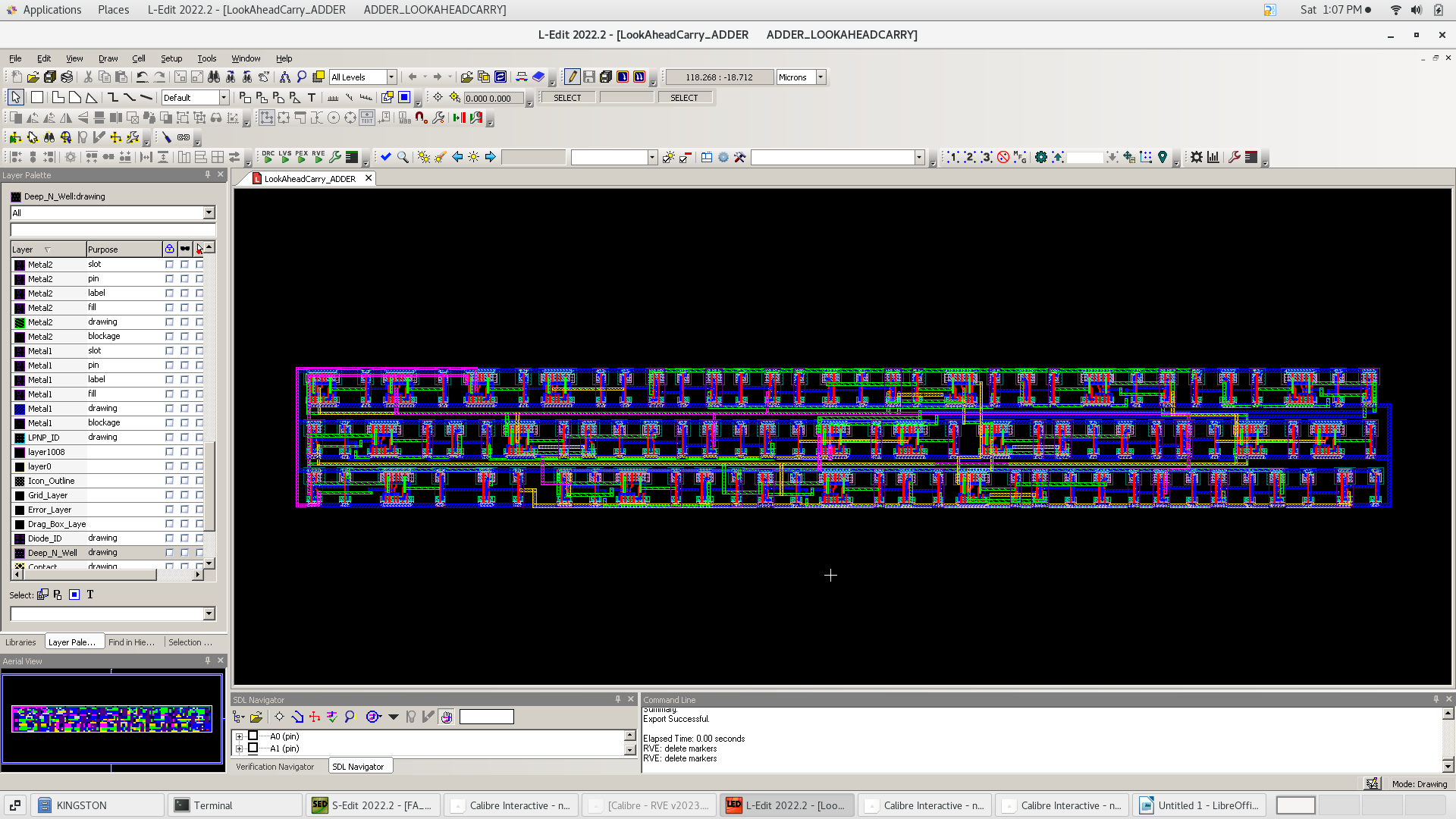
adding known input pattern through v bit with the same patteren as

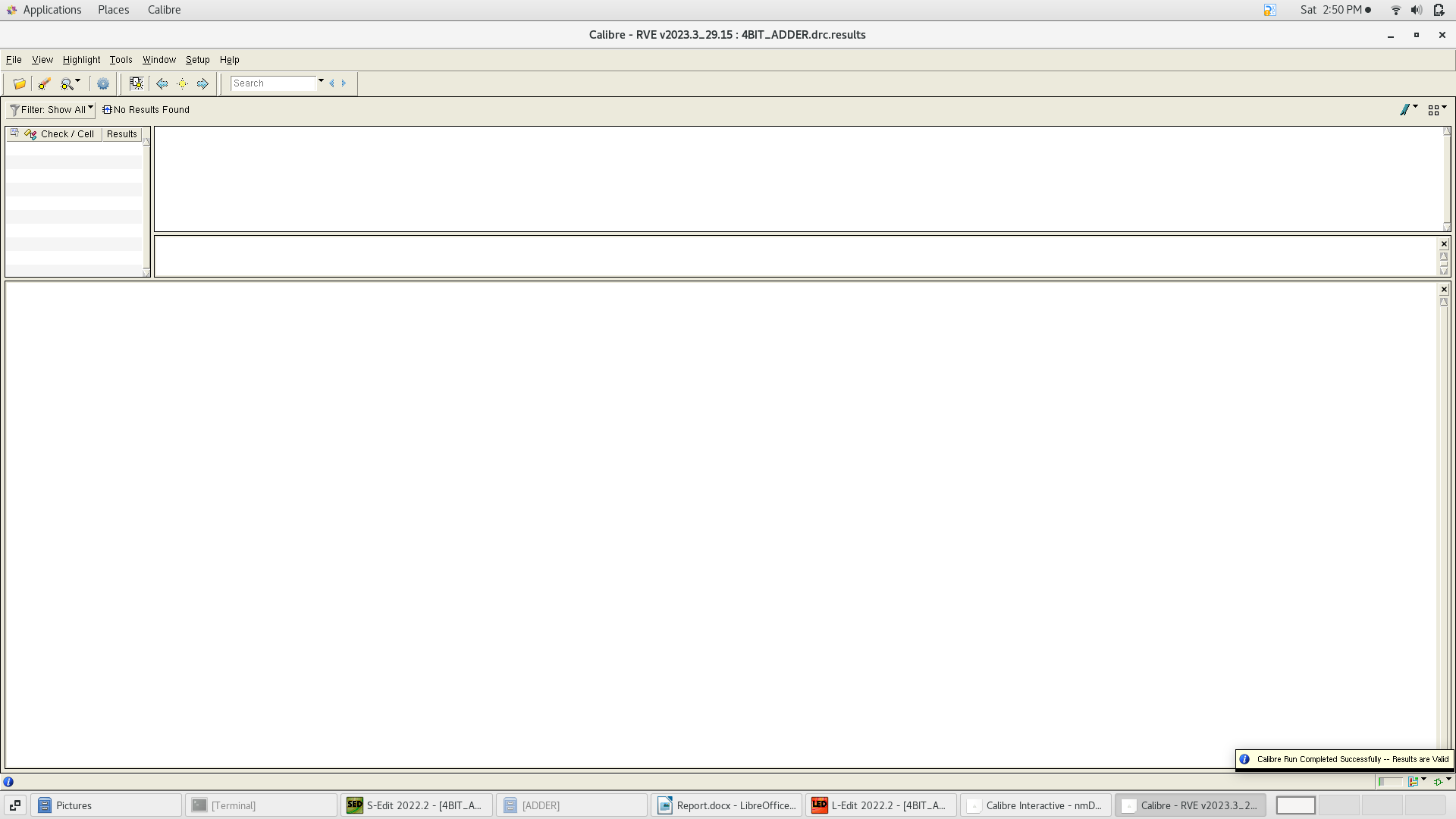
first pattern : 0101 + 1001 + 0 = 01110

 second pattern : 0111 + 1100 + 0 = 10011

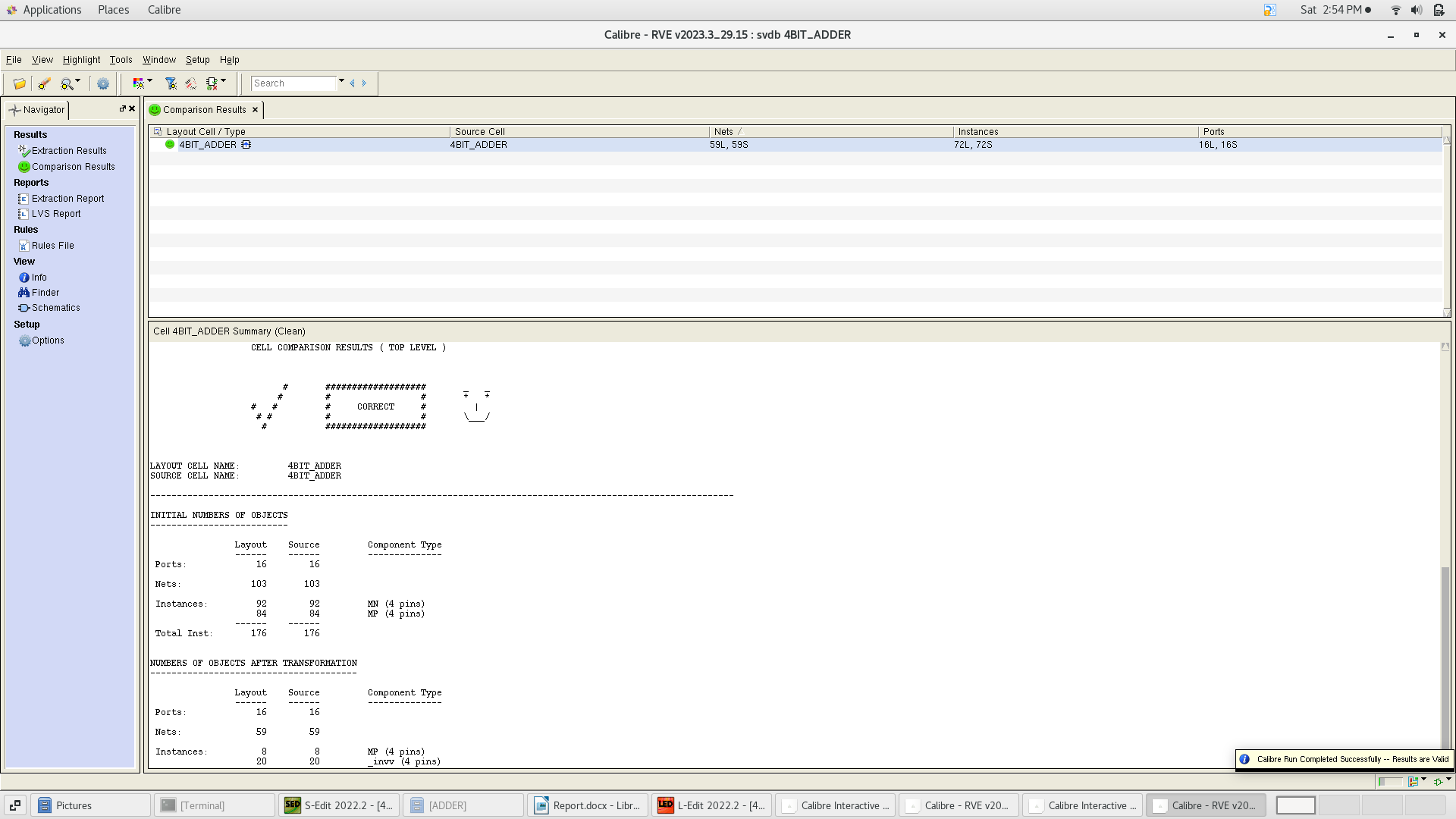
1. **Propagation Delay Calculation:** Worst case delay
2. **Power Calulation**
3. **Area**

Number of transistors = 444 Transistor

1. **1-bit Full Adder Layout**
2. **Carry LookAhead Layout for C0**
3. **Carry LookAhead Layout for C1**
4. **Carry LookAhead Layout for C2**
5. **Carry LookAhead Layout for C3**
6. **Carr4-bit Full Adder Layout**
7. **DRC Check**

We did a DRC check for each block layout to make sure that there is no any design rule violation and there is the DRC of whole design

1. **LVS Check**

the final step is to do the LVS to check that the layout is identical to the schematic

1. **conclusion**

Carry lookahead adder have more area than ripple carry adder ,it’s almost 4 times the ripple adder so it’s more complex in implementation but it’s advantage that it saves time as it’s propagation delay is less that the ripple by around 200 picosecond ,also the power of carry look ahead is more than ripple carry due to the higher area .

|  |  |  |
| --- | --- | --- |
|  | Ripple Carry | Carry LookAhead |
| Propagation delay (ps) | 600 | 400 |
| Avg. consumed power(mW) | 1.08 | 1.88 |
| Area (number of transistors) | 100 | 444 |
| Complexity | low | high |
| Turnaround time | less | more |