



```

1  `timescale 1ns/1ns
2
3  module datapath (clk, rst, read_file, file_index, line_index, write_reg, write_file);
4
5      input clk, rst, read_file, write_reg, write_file;
6      input [9:0] file_index;
7      input [5:0] line_index;
8
9      wire [24:0] reg25_in;
10     wire [24:0] reg25_out;
11     wire [24:0] perm_out;
12
13     read_file ReadFile (.clk(clk), .rst(rst),
14     |         |         |         |         .read_file(read_file), .file_index(file_index),
15     |         |         |         |         .line_index(line_index), .data_out(reg25_in));
16
17     reg25 Reg25 (.clk(clk), .rst(rst),
18     |         |         |         .ld(write_reg), .clr(rst),
19     |         |         |         .in(reg25_in), .out(reg25_out));
20
21     permutaion Permutation (.in(reg25_out), .out(perm_out));
22
23     write_file WriteFile (.clk(clk), .rst(rst),
24     |         |         |         |         .write_file(write_file), .file_index(file_index),
25     |         |         |         |         .data_in(perm_out));
26
27 endmodule

```