UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, 894, Fall 1400
Computer Assignment 1
Basic Switch and Gate Structures in Verilog
Week 3-4

Name:
Date:

1. Show switch level structure of a 2-input NAND gate and a NOT gate using nMOS and pMOS structures that have #(3,5,7) and #(4,7,9) delay values respectively.

a. Show the schematic diagram of the circuits.
b. Manually, hand simulate the circuits and, in a timing-diagram, show the two delay values To1 and To0 for each gate.
c. Write switch-level description of the NAND and NOT gates in SystemVerilog.
d. Write a testbench for the above circuits and using test data from the testbench apply inputs to cause the circuits' worst-case delays. Make sure the changes on inputs are far enough apart to put the circuits into a steady-state before the next input change.
e. Compare your hand-simulation and the SystemVerilog simulation and explain the differences, if any.

2. Show switch level structure of a 2-input NAND gate with a three-state control input and a NOT gate with such control. For the NAND gate, if the three-state control is 1, the output is the NAND of the two inputs, and if it is 0, the output is at Z. The three-state NOT gate works in a similar fashion. See the circuit in Homework 1.

a. Show the schematic diagram of the circuits.
b. Manually, hand simulate the circuits and, in a timing-diagram, show the three delay values To1, To0, and ToZ for each gate.
c. Write switch-level descriptions of the three-state NAND and NOT gates in SystemVerilog.
d. Write a testbench for the above circuits and using test data from the testbench apply inputs to cause the circuits' worst-case delays. Make sure the changes on inputs are far enough apart to put the circuits into a steady-state before the next input change.
e. Compare your hand-simulation and the SystemVerilog simulation and explain the differences, if any.

3. Using gates of Part 1 develop a circuit for implementing $w = d' \cdot c' + d \cdot (a.b)'$. The elements of this circuit are gates of Part 1.

a. Show the schematic diagram of the circuit.

b. Manually, hand simulate the circuit and, in a timing-diagram, show the delay values To1, and To0 for *w*. Use worst-case delay values calculated in Part 1.
c. Write a testbench for the above circuit and using test data from the testbench apply inputs to cause the circuits' worst-case delays. Make sure the changes on inputs are far enough apart to put the circuits into a steady-state before the next input change.
d. Compare your hand-simulation and the SystemVerilog simulation and explain the differences, if any.

4. Using gates of Part 2 develop a circuit for implementing $w = d' \cdot c' + d \cdot (a.b)'$. The elements of this circuit are gates of Part 2.
a. Show the schematic diagram of the circuit.
b. Manually, hand simulate the circuit and, in a timing-diagram, show the delay values To1, and To0 for *w*. Use worst-case delay values calculated in Part 1.
c. Write a testbench for the above circuit and using test data from the testbench apply inputs to cause the circuits' worst-case delays. Make sure the changes on inputs are far enough apart to put the circuits into a steady-state before the next input change.
d. Compare your hand-simulation and the SystemVerilog simulation and explain the differences, if any.

5. Show switch level structure of a CMOS Complex Gate for implementing $w = d' \cdot c' + d \cdot (a.b)'$. Use nMOS and pMOS structures that have #(3,5,7) and #(4,7,9) delay values respectively.
a. Show transistor level schematic diagram of the circuit.
b. Manually, hand simulate the circuit and, in a timing-diagram, show the delay values To1, and To0 for *w*.
c. Write a testbench for the above circuit and using test data from the testbench apply inputs to cause the circuits' worst-case delays. Make sure the changes on inputs are far enough apart to put the circuits into a steady-state before the next input change.
d. Compare your hand-simulation and the SystemVerilog simulation and explain the differences, if any.

6. Compare circuits of Part 3, 4 and 5. You are to develop a testbench and instantiate all three circuits.
a. Show block diagram of your testbench in which the three circuits are instantiated.
b. Write SystemVerilog description of the testbench examining the three circuits. Among all the date that you are using, make sure you apply data that causes the worst-case delays of the circuits.
c. Compare the circuits in terms of timing, number of transistors, and power consumption. Explain how you are estimating power consumptions of the three structures.

Deliverables:

Generate a report that includes all the items below:
A. For Parts 1 and 2, do Parts a and b on paper and Part c that corresponds to the circuit diagram. Calculate hand simulations and include your arithmetic in the report. On paper,

show your timing extractions from the waveforms. Show waveforms as proof of simulation. Your simulation run and the project built for this purpose must be demonstrated to the TA.

B. For Parts 3, 4, and 5, show circuit diagrams, hand calculations and waveforms. Your SystemVerilog descriptions must correspond to the circuit diagrams. Your simulation run and the project built for this purpose must be demonstrated to the TA.
C. For Part 6, project file and Waveforms must be demonstrated to the TA. Using waveforms, circuit diagrams, and other circuit representations justify your answers for transistor count, timing, and power usage of each structure.

Make a PDF file of your report and name it with the format shown below:

FirstinitialLastnameStudentnumber-CAnn-ECEmmm

Where *nn* is a two-digit number for the Computer Assignment, *mmm* is the three-digit course number under which you are registered, and hopefully you know the rest. For the *Firstinitial* use only one character. For *Lastname* and for the multi-part last names use the part you are most identified with. Use the last five digits of your student id (exclude 8101) for the *Studentnumber* field of the report file name.