UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367 / Digital Systems I, ECE 894
Fall 1400
Computer Assignment 5
Orthogonal State Machine, Pre- and Post-Synthesis
Week 24

Name:
Date:

A serial transmitter circuit searches on its *serIn* input for a start sequence of **10110** to begin transmitting its *serIn* on its *serOut*. When the start sequence is received, the *serOutValid* is asserted and for the next 177 clock cycles whatever appears on *serIn* will be transmitted on *serOut*. After the entire 177 bits are transmitted, the circuit returns to the state where search for the start sequence begins again. The initial state of this circuit is where it searches for the start sequence.

a. Write a complete behavioral SystemVerilog description of a Moore machine that detects the **10110** sequence. Use an asynchronous reset and the positive edge of the clock. This is your pre-synthesis design of the Moore **10110** detector.
   i. Using a SystemVerilog testbench in the ModelSim simulation environment completely simulate your circuit. This is your pre-synthesis description.
   ii. Import your Moore design in Quartus and build a symbol for it. Synthesize this design and see its timing, floor-plan and cells used. The synthesis process generates the post-synthesis description of your Moore **10110** detector. The .vo and .sdo files that are produced contain the netlist and timing of the synthesized circuit.
   iii. Instantiate the pre- and post-synthesis descriptions of the Moore machine in a SystemVerilog testbench and compare the timing of the two descriptions.

b. In Quartus, use existing library components, i.e., *lpm*, to design a divider circuit that divides its input frequency by 177. Use an asynchronous reset and the positive edge of the clock. This is your pre-synthesis design of the 177-divider circuit.
   i. Build a symbol for your 177-divider circuit. Synthesize this design and see its timing, floor-plan and cells used. The synthesis process generates the post-synthesis description of 177-divider circuit. The .vo and .sdo files that are produced contain the netlist and timing of the synthesized circuit.
   ii. Instantiate the post-synthesis 177-divider circuit in a SystemVerilog testbench and observe its timing.

c. In a new Quartus project, import the descriptions of Part a and Part b to build the serial transmitter circuit described in the problem description.

i. Synthesize this design and see its timing, floor-plan and cells used. The synthesis process generates the post-synthesis description of the serial transmitter circuit. The .vo and .sdo files that are produced contain the netlist and timing of the synthesized circuit.
ii. Instantiate the post-synthesis serial transmitter circuit in a SystemVerilog testbench and observe its timing and its functionality.

Deliverables:

Generate a report that includes all the items below:

A. Prior coming to the lab, for all the above problems hand-drawn schematic diagrams and partial timing diagrams are required. Your SystemVerilog descriptions must correspond to the circuit diagrams. Your simulation run and the project built for this purpose must be demonstrated to the TA.
B. Document your Quartus projects of Parts a, b, and c. Make sure you understand the synthesis outputs and their corresponding timings.
C. For all three parts, you should look at the FPGA layouts, device view and RTL view. Be able to explain the details of various views. In the layout be able to identify FPGA cells that use a memory element versus those that are purely combinational..
D. For all problems, be prepared to answer questions asked about the timings, generated hardware, pre- and post- synthesis, and FPGA mappings.

Make a PDF file of your report and name it with the format shown below:

FirstinitialLastnameStudentnumber-CAnn-ECEmmm

Where *nn* is a two-digit number for the Computer Assignment, *mmm* is the three-digit course number under which you are registered, and hopefully you know the rest. For the *Firstinitial* use only one character. For *Lastname* and for the multi-part last names use the part you are most identified with. Use the last five digits of your student id (exclude 8101) for the *Studentnumber* field of the report file name.