RELIABILITY BEHAVIORS OF HCI AND NBTI ON PLANAR MOSFET AND NOVEL FINFET

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RELIABILITY BEHAVIORS OF HCI AND NBTI ON PLANAR MOSFET AND NOVEL FINFET

RAHIMAH BINTI HASSAN

A report submitted in partial fulfilment of the
requirements for the award of the degree of
Bachelor Degree of Electrical-Electronic Engineering

Faculty of Electrical Engineering
Universiti Teknologi Malaysia

DECEMBER 2014

I declare that this report entitled *"RELIABILITY BEHAVIORS OF HCI AND NBTI ON PLANAR MOSFET AND NOVEL FINFET"* is the result of my own research except as cited in the references. The report has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

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Name	:	RAHIMAH BINTI HASSAN
Date	:	December 30, 2014

I owe my special thanks to my friend Zuriana Binti Auzar, who are give me constant kind help and moral support despite the hectic semester that we had to undergo. Last but not least, my deepest appreciation to my parents and family members, for all their guidance, love and care.

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Alhamdulillah and I am grateful to Allah SWT. that I am able to complete my first report of final year project. First and foremost, I would like to extend my highest gratitude and thanks to my supervisor Dr. Nurul Ezaila Binti Alias for supervise, guidance and also assist me throughout this semester. I expose myself to independent learning skill. Based on this project I have deep study about reliability issues of HCI and NBTI.

ABSTRACT

In this research, reliability issues of HCI in NMOS and NBTI in PMOS on planar MOSFET and novel FinFET is investigated. This research work is categorized into two part: design device structure model of planar MOSFET and 3D FinFET and compare the reliability issues of HCI and NBTI on both structure. Both device structure model are develop by using GTS Framework simulation software where this software are specification for reliability issues. Other than that, the software simulation also can obtained I-V graph. Based on I-V graph, physical parameter can be extract in order to analyze the threshold voltage (VT), subthreshold swing (S), ION and IOFF. Some optimization for both device structure model will be conducted due to the reliability issues of HCI in NMOS and NBTI in PMOS. In addition, there are two method that will be used in this project. These two method are, HCI stress application to the n-channel and NBTI stress application to the p-channel. There are many research about reliability issues of HCI and NBTI in MOSFET and FinFET that have been studied in this project. Most researcher are focusing about the mechanism and fundamental of HCI and NBTI issues. There are many different approach that have been done to do the research on these reliability issues

ABSTRAK

Ini adalah abstrak Bahasa Melayu

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LIST OF ABBREVIATIONS

XML	-	Extensible Markup Language
XML	-	Extensible Markup Language
XML	-	Extensible Markup Language
XML	-	Extensible Markup Language
XML	-	Extensible Markup Language
XML	-	Extensible Markup Language

LIST OF SYMBOLS

γ	-	Whatever
γ	-	Whatever
γ	-	Whatever
γ	-	Whatever
γ	-	Whatever

CHAPTER 1

INTRODUCTION

1.1 PROJECT BACKGROUND

In 1975, Gordon Moore, co-founder of industry leader Intel, predicted that the number of transistors on a chip would double about every two years [1]. This is known as Moore's law. In 1971, the revolutionary Intel 4004 processor contained 2300 transistors [1]. At the end of 2009, Intel launched their Westmere processor containing over 1.9 billion transistors [1]. Over the next decade, processors will contain 50-100 billion transistors [1]. As a conclusion, Moore's law has fuelled a technology revolution. This is due to the number of transistors integrated into microprocessor chips increases for greater computing power.

There are four terminal in metal-oxide-semiconductor-Field Effect Transistor (MOSFET) device which are gate, source, drain and body terminal. MOSFET are also consists MOS capacitor where either it is highly doped at source or drain region. Other than that, MOSFET has two types of mode operation which are "enhancement mode" and "depletion mode". P- substrate, n+ source and n+ drain region consists on n-channel "enhancement mode" MOSFET while for p-channel MOSFET consists n-substrate and p+ source and p+ drain region [1]. Figure 1.1 is a schematic of n-channel MOSFET with their electrical connection [1]. Based on Figure 1.1, the source and substrate are grounded [1]. Voltage can be applied at gate terminal, to ensure current can flow between source and drain terminal.

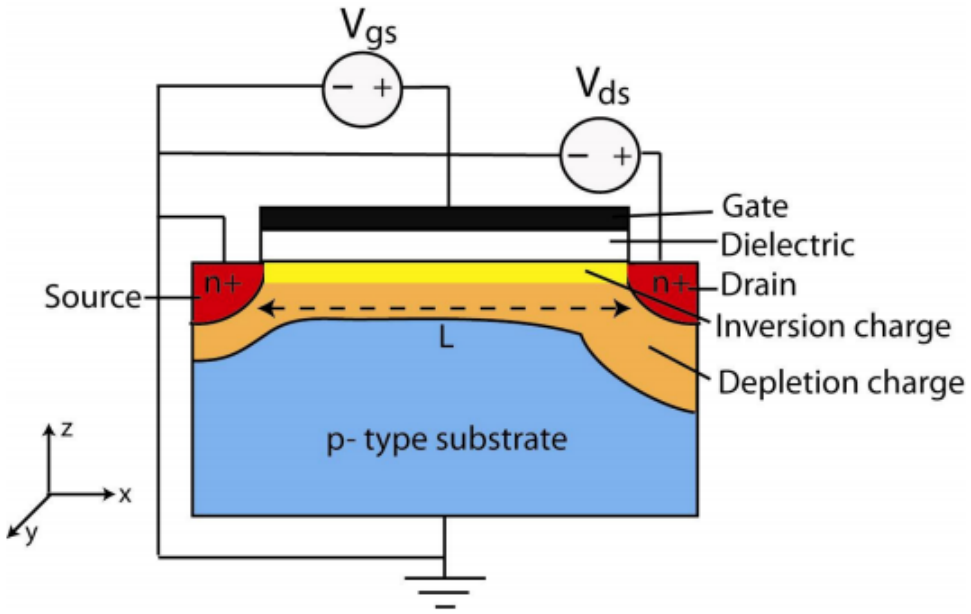

Figure 1.1: Schematic of n-channel MOSFET with their Electrical Connection.

When $V_{GS} > V_T$, the device will become n-type MOSFET. Normally, source terminal for n-channel MOSFET is biased at zero volt than the drain terminal. When drain voltage (V_{DS}) is applied, electron will flow from source to the drain terminal. If gate voltage increases, the concentration of electron at the surface of device also increases. Due to this, more current are allow to flow. When $V_{GS} < V_T$, the source terminal for p-channel MOSFET is biased at high potential which is connected to supply voltage (V_{DD}) and there is no current can flow between the source and drain terminal. There is only holes flow from source to the drain. For body terminal, it is connected to a fixed point where for n-channel MOSFET, the body terminal connected to zero volt and for p-channel MOSFET, the body terminal connected to V_{DD}.

By changing the MOSFET structure design, short channel effects, current leakage can be reduced and novel FinFET can be created. Novel FinFET are also forming by using multiple gates. Basically, the operation of planar MOSFET and novel FinFET are almost same. There are differences between structure design of planar MOSFET and novel FinFET. Figure 1.2 shows, the design structure of novel FinFET. It is clear from Figure 1.2, the structure of 3D FinFET is contained fin shaped body that form the source and drain terminal. Along the source and drain terminal, there is path provided for current to flow when switched is ON for the transistors [2]. There are three gates that surrounding the fin body where it control the switching operation

or it is function as electrostatic control. The gates also wraps around the fin to form 3-D structure [2]. As the width of the fin is scaled down, the short channel effect and current leakage can be suppressed [1]. The vertical nature of a finFET provides a greater device width per wafer area [1]. Due to this, FinFET can be packed more densely than planar MOSFET [1].

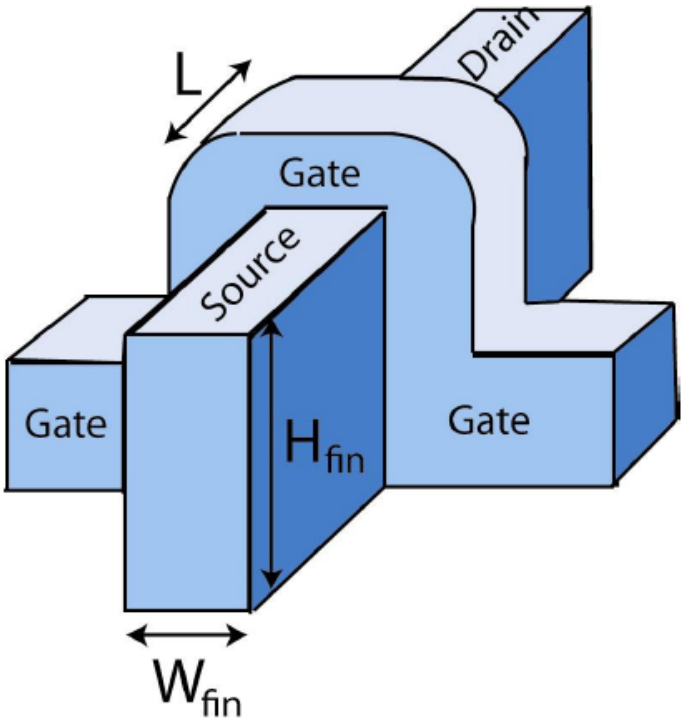

Figure 1.2: Design Structure of 3D FinFET

Due to the size of MOSFET's shrink, the integrated circuit performance become improve in terms of speed, and power consumption. At the same time, the reliability issues are also become the most important challenges for digital and analog complementary-metal-oxide-semiconductor (CMOS) circuits. In this project there are two reliability issues that will focusing which are Hot Carrier Induced (HCI) in NMOS and Negative Bias Temperature Instability (NBTI) in PMOS. HCI is happen when higher stress voltage is applied at drain terminal. For this project, value of V_D is given more than 1.2V for saturation region and more than 0.1V for linear region at the drain terminal of the devices. Then, higher electric field will occurs and attributed the creation of carriers such as holes and electrons.

Based on Figure 1.3, high electric fields will accelerated the carriers to high velocities and the charge carriers will become trapped in the oxide near the edge of drain terminal [3]. These trapped charges is the major issues where it can cause the device degradation. Other than that, threshold voltage (V_{TH}), linear (I_{DLIN}) and saturation (I_{DSAT}) drain current will be shifted or changes before and after high stress voltage applied. The charge carrier will be heating due to high electric field and it will causes ionization near the drain terminal. After that, electron-hole pairs were created.

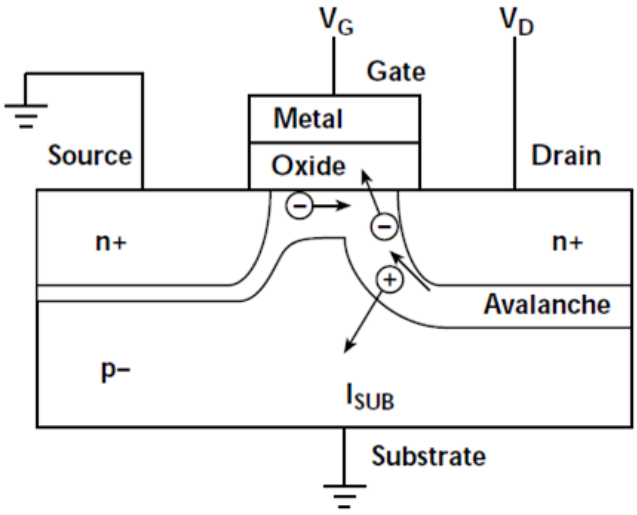

Figure 1.3: Hot Carrier Induced in N-Channel MOSFET

NBTI has been known for decades [4],[5], [6] and recently, it become most important reliability issues that need to be more concern [7]. When stressed with high negative gate voltage at elevated temperature is applied to the gate oxide of p-channel MOSFET, NBTI will occurs. High electric fields will occur too and it will attributed the creation of interface trap and oxide charge where holes become majority carriers. The interface trap will occur between surface of silicon dioxide (SiO_2) and silicon (Si) substrate. Initially, there are many source hydrogen bonds at interface between Si and SiO_2 when high stress negative gate voltage is start to applied. Other than that, at the Si-SiO_2 interface, dangling-bond will created if hole reacts with silicon hydrogen bond (Si-H) [8]. As an addition, in planar MOSFET the dangling Si bond will be passivate during manufacture when the transistors are annealed in hydrogen ambient [9].

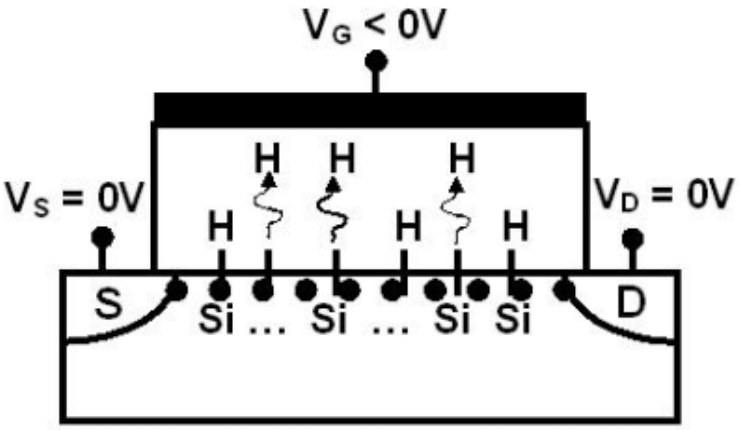

Figure 1.4: Negative Bias Temperature Instability in P-Channel MOSFET

When stress given is too high to the gate oxide of p-channel MOSFET, the silicon hydrogen bond will broken. Due to this, hydrogen ion ($H+$) will be diffused away into the oxide and captured. The vacancy at Si bond will be filled with charge carrier. As the result from this phenomena, I_{DLIN} and I_{DSAT} will be decreased and V_{TH} will be shifted. Figure 1.5, shows the value of V_{TH} will be shifted after NBTI stress application[10].

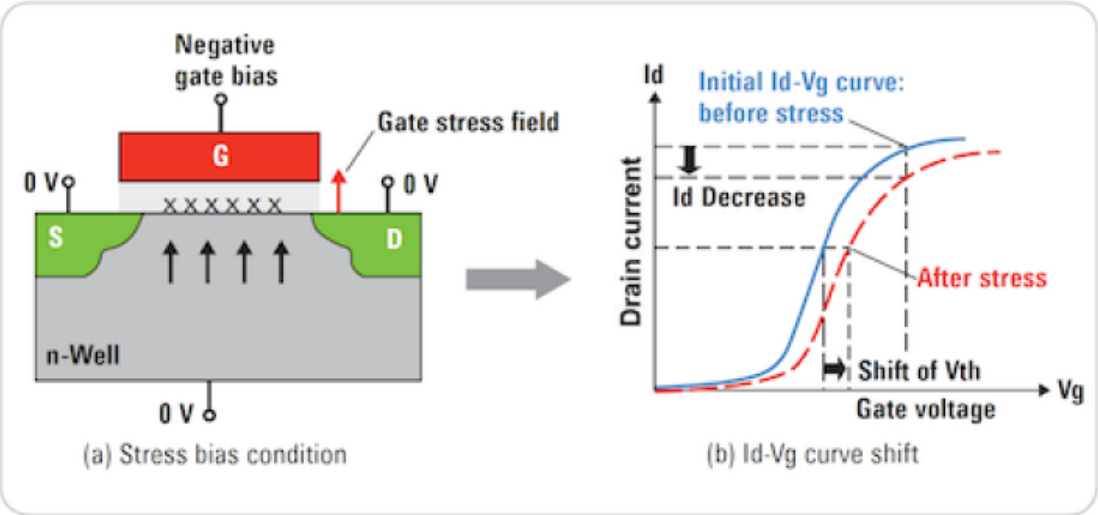

Figure 1.5: NBTI effect on P-Channel MOSFET a) Negatively Gate Bias is Applied to PMOS at Elevated Temperature b) I-V Characteristics Shifted After NBTI Sress Application

Both HCI and NBTI has become the most important reliability issues because it will reduce lifetime estimation of the device. For example, if the device can be operates for 20 years, due to reliability issues the device will be operates less than 20 years which is not good for technology revolution.

1.2 PROBLEM STATEMENTS

As technology of MOSFET are scaling down, the reliability issues of n-channel and p-channnel affecting the device performances. Scaling down MOSFET means decreased MOSFET gate length towards tens of nanometers to become smaller MOSFET. When the transistors become smaller, more devices can be pack in a given chip area and the costs of the device can be reduced but short channel effect will occur. The most important reliability concerns are HCI in NMOS and NBTI in PMOS. These reliability issues become one of the challenges for VLSI design. Further study on reliability issues were conducted on both planar MOSFET and novel FinFET in this project. The purpose of this study, to make conclusion between planar MOSFET and novel FinFET which one give less impact device performance regarding their reliability issues.

1.3 OBJECTIVES

The specific objectives of this project are:

1. To design an optimized 3D FinFET device structure using GTS Framework
2. To compare the reliability behaviors of planar MOSFET and novel FinFET
3. To compare reliability issues of n-channel and p-channel FinFET.

1.4 PROJECT SCOPE

The aim of this project is to investigate the reliability behaviours of HCI and NBTI on planar MOSFET and novel FinFET. The scope of this project are:

1. Literature review on MOSFET and FinFET device structure including their reliability issues.
2. Design an optimized MOSFET and FinFET device by using GTS Framework.
3. Further study on previous research related to reliability (specifically HCI & NBTI) for planar MOSFET and novel FinFET.

1.5 THESIS ORGANIZATION

This thesis is divide into five chapters. Chapter one is introduction of the project. It consists of project background, problem statements, objectives, project scope, thesis organization and planning work for semester one and two.

Chapter two is literature review based on previous past published paper, journal and thesis. All of these source give a detailed description on reliability issues of HCI and NBTI on planar MOSFET and novel FinFET. The theory and mechanisms of reliability issues well described in this chapter.

Chapter three deals with methodology and approach to complete this project. The design flowchart of project are provided in this chapter .

Next, the result and discussion will be discussed in chapter four. The result consists of 3D devices structure FinFET and planar MOSFET. The electrical characteristics will be obtained from the simulation of GTS Framework.

Lastly, chapter five is the conclusion of the project. There are suggestion and recommendation in this chapter for future improvement.

1.6 PLANNING WORK FOR SEMESTER 1 AND 2

Planning work for semester one and two had been outlined and shown in the Gantt chart.

WEEK / ACTIVITIES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Meeting with Coordinator																
Meet the supervisor																
Get and Confirm the Title																
Analyze the Title																
Research and Study on Reliability of MOSFET (HCI and NBTI)																
Research and Study on Reliability of FinFET (HCI and NBTI)																
Literature Review																
Preparation for Presentation FYP1																
Presentation of FYP1																
Report Writing																
Submission of report and logbook																

Figure 1.6: Gantt Chart for Semester 1

WEEK / ACTIVITIES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Meet the supervisor																
Get Used with GTS Framework Software																
Design and optimized FinFET Device (Channel Length, Oxide Thickness)																
Design a Conventional MOSFET Device (Channel Length, Oxide Thickness)																
Analyze and Compare FinFET Design with Conventional MOSFET (IV-Characteristics, charge trapping at Oxide, Threshold Voltage and Current Leakage)																
Submit Project Summary																
Preparation for Presentation of FYP2																
Presentation of FYP2																
Writing Thesis																
Submission of Thesis and logbook																

Figure 1.7: Gantt Chart for Semester 2

CHAPTER 2

LITERATURE REVIEW

2.1 RELIABILITY OF MOSFET's

In 1991, James E. Chung et. al. had done the research on performance and reliability design issues for deep-submicrometer MOSFET's. They are also examined on device design constrains. It were included threshold voltage variation due to short-channel and drain-induced-barrier-lowering effects [11]. Other than that, hot-carrier effects such as hot-electron degradation and avalanche breakdown were considered too [11].

The finding from this paper are about hot-electron degradation and design guidelines for the curves. They used hot electron lifetime prediction model[12]. Drain current measured at a bias condition of V_G = 3V and V_{DS} = 0.1V and all MOSFET's device were stressed under peak substrate conditions [11]. Other than that, MOSFET with a thinner gate oxide possesses will be at a higher peak lateral electric field E_m. It will be happens when stressed given is under an identical drain bias [13], [14]. As a result of E_m is higher, more interface states and electron traps are generated [11].

Next for the design curve findings, they use three methods. First method is about fixed power-supply voltage where value of V_{DS} = 3.3V [11]. The MOSFET's with channel length (L_{eff})=0.40um and oxide thickness (T_{ox})= 8.6nm are used for digital design window [11]. Fixed oxide thickness is a second method for design curve where value of Tox = 8.6nm [11]. The MOSFET's device with L_{eff} = 0.35um and V_{DS} = 2.9 V were used [11]. All these value also, for digital design window [11]. Lastly, they used fixed channel length where L_{eff} = 3.0um [11]. MOSFET's with T_{ox} = 7.0nm and V_{DS} = 2.6V were used for allowable digital design window [11]. As a conclusion from this paper, they are able to compare the channel length, oxide thickness and power supply voltage by different performance and reliability constraint [11]. Device curve

design also successfully done.

In 1995, Moussumi et. al. was finished the research on electrical properties and reliability of MOSFET's with rapid thermal NO-Nitrided SiO2 gate dielectrics. Basically this research about the performance and hot carrier reliability of N- and P-channel MOSFET's with oxynitride gate dielectrics fabricated by rapid thermal nitridation (RTN) of thermally grown SiO_2 in pure nitric oxide (NO) ambient [15]. Method that was used in this research is about fabrication on N- and P- channel MOSFET's by using CMOS twin-well-technology [15]. Both devices were received a post-oxidation anneal of 20 seconds at 1050°C in N_2 ambient [15]. Other than that, CV measurements on a capacitor adjacent were used to determined the gate oxide thickness [15].

The findings from this paper are about N- and P- MOSFET's device reliability. Shorter gate length (Lg) was used for both device, which is 60nm and it is used to study about HCI reliability. Besides that, all N-MOSFET devices were stressed at fixed V_d = 7V and V_g is approach to 2V [15]. The result of the degradation drive current will compared with control oxide where NO-annealed oxynitride devices show significantly low degradation under channel hot-carrier stress [15]. For P-MOSFET device, HCI degradation is due to electron trapping. All P-MOSFET devices were stressed at fixed V_D = 7V for 1600 second with different value of gate voltages [15]. The result for degradation of NO-nitrided oxides is observed where NO-nitrided oxides is lower than SiO_2 gate oxides [15]. As a conclusion for this paper, the performance and hot-carrier immunity for both N- and P- channel MOSFET with NO-nitrided SiO_2 gate dielectrics have been done [15].

2.2 HOT CARRIERS DEGRADE N-CHANNEL MOSFET's

In 2001, Radwan Dandeh has proposed how do hot carrier degrades N-channel MOSFET's. This paper was discussed about theory of hot carrier degradation in n-MOSFET's device. In this research work, he is focusing on carrier injection process where electrons and holes are injected into the oxide [16]. Other than that, the damage creation process and the impact of the damage on the MOSFET's terminal are also examined [16].

Carrier injection process is the first findings from this paper, where the carrier

will be injected into the oxide. It will happens if only hot carrier have energies greater than the Si-SiO_2. By measuring gate current (I_g) that across the gate oxide, the carrier injection can be determined. There is two phenomena that caused I_g increase as V_g increase [16]. First, more electrons are obtainable to be injected into the gate if the inversion charge in the channel is increase [16]. Second, few electrons are accelerated back towards the channel once in the oxide if the vertical electric field in the oxide becomes more favorable [16].

Second findings from this paper are about damage creation process. Usually, at low and medium value of V_g , the interface trap generation rate is largest. The trap creation process requires holes and electrons energy that not larger than energy released from interfacial trapped hole where is neutralized already by electron capture [16]. This is because holes and electrons energy required to overcome the Si-SiO_2 barrier [16]. Holes is the most carrier that will be injected to the oxide, at the low gate voltage state. Due to this, many holes will be trapped at defect sites on oxide [16].

Third findings from this paper is about effects of interface traps and bulk oxide trapped charge. Hot carrier stress will created damage that near the edge drain terminal where electric field at maximum. This will contributed the carriers to be hottest [16]. Figure 2.1, shows I_d versus V_g graph. A MOSFET's with L_g = 0.75um, V_g = 1.8V and V_{ds} = 0.5V, stress were applied for 1000seconds [16]. Based on Figure 2.1, threshold voltage will be increases or shifted and drive current will be decreases after stress given [16]. As a result, interface trap generation is builds up. The conclusion from this paper, by increasing the immunity of the gate insulator to damage during hot carrier injection, the hot carrier reliability of N-MOSFET can be improved [16].

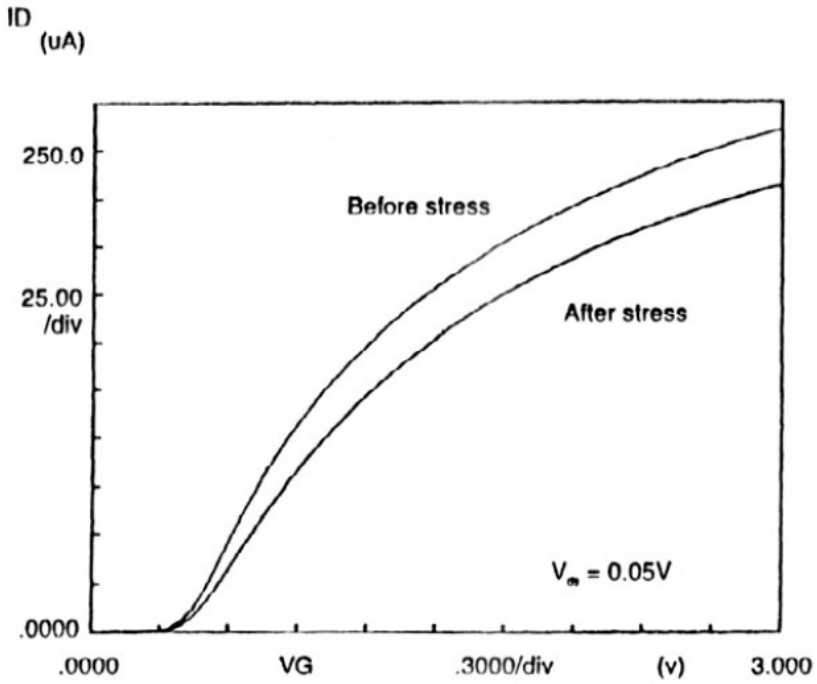

Figure 2.1: I_d versus V_g Graph for MOSFET Device Before and After Stress with L_g = 0.75um, V_g = 1.8V and V_{ds} = 0.5V

2.3 RELIABILITY CMOS FinFET's

In 2003, Yang-Kyu Choi et. al. was finished their research on reliability study of CMOS FinFET's with 2.1nm-thick gate SiO_2. In this work, the reliability of FD-SOI CMOS FinFET's were investigated [17]. They reported that hot-carrier immunity improves as the fin width of FinFET device decreases [17]. Other than that, it is degrades at elevated temperature. This is because, due to self-heating effect[17]. They also used two method for their experiment. First, fabrication of e-beam lithography were used for P+ poly-SiGe gate FinFET with channel length down to 23nm[17]. Second method is, fabrication by using spacer lithography for N+ poly-Si gated FinFET's with gate length 120nm [17].

There are several findings in this paper, where it happens in a double-gate n-channel MOSFET. In this design structure there are energetic electrons that generate by impact ionization [17]. It happens near the drain terminal of double-gate n-channel MOSFET under hot-carrier stress bias conditions, and all energetic electrons will become trapped at the gate oxide interface[17]. This situation can be seen in Figure 2.2. Due to electron trapping at the gate oxide interface, Vg will increases and generated

holes flows to the region of lowest potential [17].

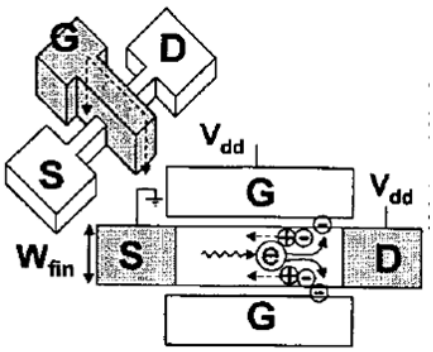

Figure 2.2: Carrier Movement in an N-Channel Double Gate MOSFET

Next finding is about, gate-underlapped n-channel FinFET's. V_t decrease with increasing stress time, due to holes that trapped in the gate-oxide while interface at this region[17]. Besides that, at higher value of V_d, electrons trapping become dominant, then eventually value of V_t is increases with increasing stress time [17]. This can be shown in Figure 2.3 where V_t shifts versus stress time for different bias stress voltages. Moreover, for p-channel FinFET of gate-overlapped the value of V_t decreases slowly with increasing value of V_d [17]. It is sown in Figure 2.4 where V_t shifts versus stress time for different drain bias stress voltages. As a conclusion from this paper, HCI will improves when fin width decreases [17].

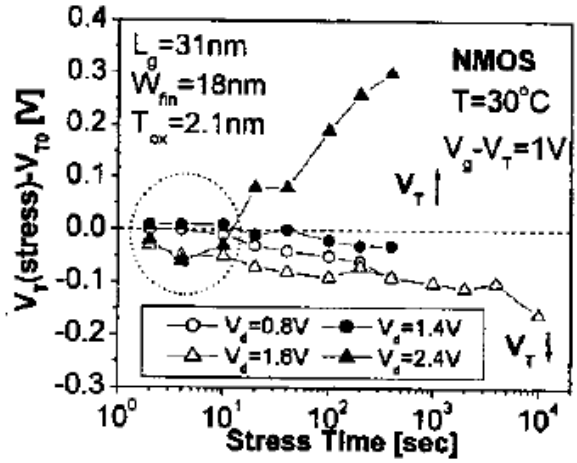

Figure 2.3: Gate Underlapped Structure of NMOS FinFET

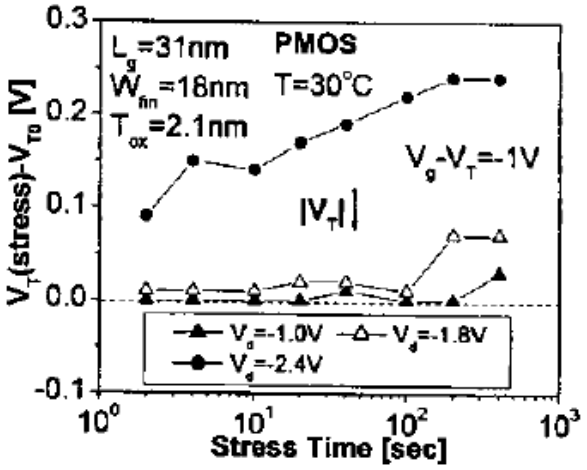

Figure 2.4: Gate Overlapped Structure of PMOS FinFET

CHAPTER 3

METHODOLOGY

3.1 INTRODUCTION

In this chapter, method to conduct this project is briefly explain. The general block diagram and the flow chart of the project are presented. There is example of device FinFET structure that was design in GTS Framework. This aim of this example is to give an overview of the project that lead to the final result.

3.2 PROJECT OVERVIEW

The objectives of this project are to design 3D structure of novel FinFET and planar MOSFET, to compare reliability issues of n-chanel and p-channel of FinFET device and reliability behaviors of planar MOSFET and novel FinFET. In order to achieved that objectives, the GTS Framework software is used to make the design. The general block diagram of the project is shown in Figure 3.1.

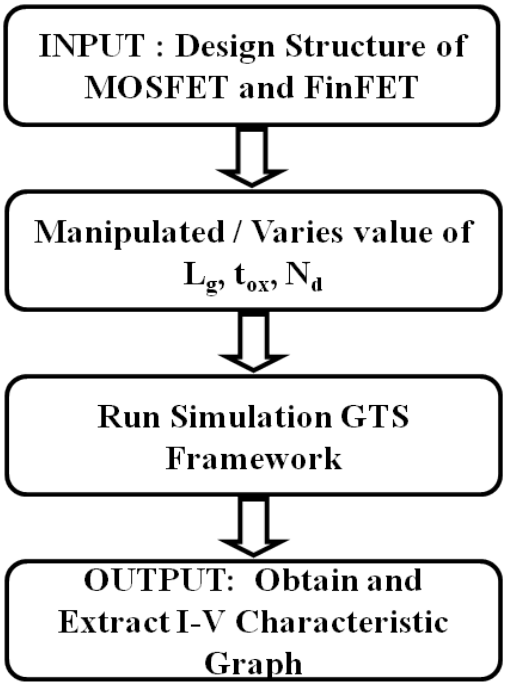

Figure 3.1: General Block Diagram of the Project

At first, structure of planar MOSFET and novel FinFET will be design as an input for this software. Then, value of channel length, oxide thickness and doping concentration were manipulated due to literature review. After that, simulation can be run to get the output of I-V graph. Due to this, threshold voltage, Ion and Ioff can be obtained and analyzed as a results. Based on Figure 3.2, the structure design of the template "nmos_32nm_finfet.ipd"

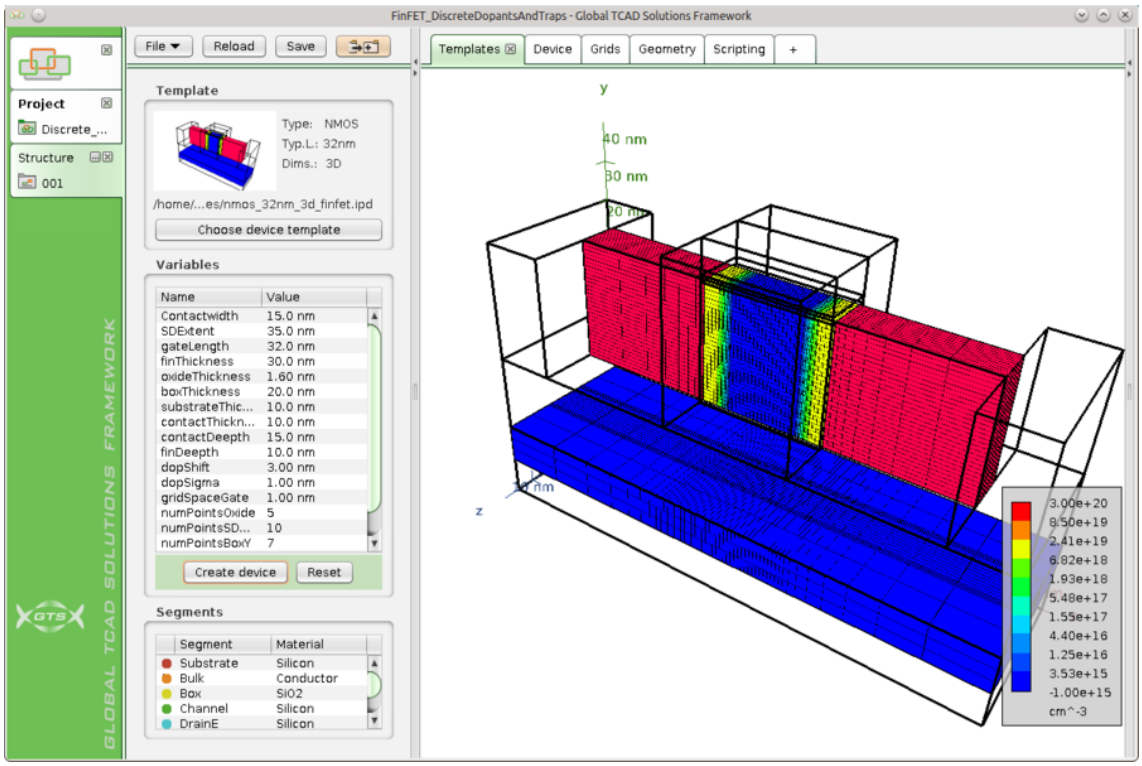

Figure 3.2: Structure Design of nmos_32nm_finfet.ipd

3.3 FLOW CHART

Figure 3.3 shows the flow chart of this project. In completing the project, there must be a standard steps that need to obey. First and foremost, the fundamental of reliability issues (HCI and NBTI) for planar MOSFET and novel FinFET were deeply studied by doing literature review. Regarding to this, a lot of effort need to put on focusing the research that related to reliability issues (HCI and NBTI) for planar MOSFET and novel FinFET. Other than that, to develop design structure of planar MOSFET and novel FinFET, the device simulation that using GTS Framework software were exposed. By doing the device simulation, electrical properties of both structure can be obtained.

Electrical properties that will be obtained are I-V characteristics, threshold voltage, subtreshold swing, Ion, and Ioff. The next step is, optimization for both device. If the device structure cannot be optimized, perform back the steps at development of device simulation and obtaining electrical properties. If the device structure for planar MOSFET and novel FinFET can be optimized, the reliability

simulations in GTS module can be performed. After getting the result from reliability simulation, make comparison with literature review.

In order to compare the degradation of short channel effect for both device, higher stress voltage will be applied. There are two sections for device application stress, where HCI stress were applied to n-channel while NBTI stress were applied to p-channel. This device application stress will be applied for planar MOSFET and novel FinFET. After this step completed, result from device application stress can be analyzed and make comparison again with literature review. Then the important step where, reliability n-channel and p-channel of FinFET need to compare and lastly, finalized the result to make a conclusion between HCI and NBTI which one will be more degrade. At the same time, another conclusion will come out where between planar MOSFET and novel FinFET which one will give better performance. Troubleshoots and improvement will be done after make up with two conclusions.

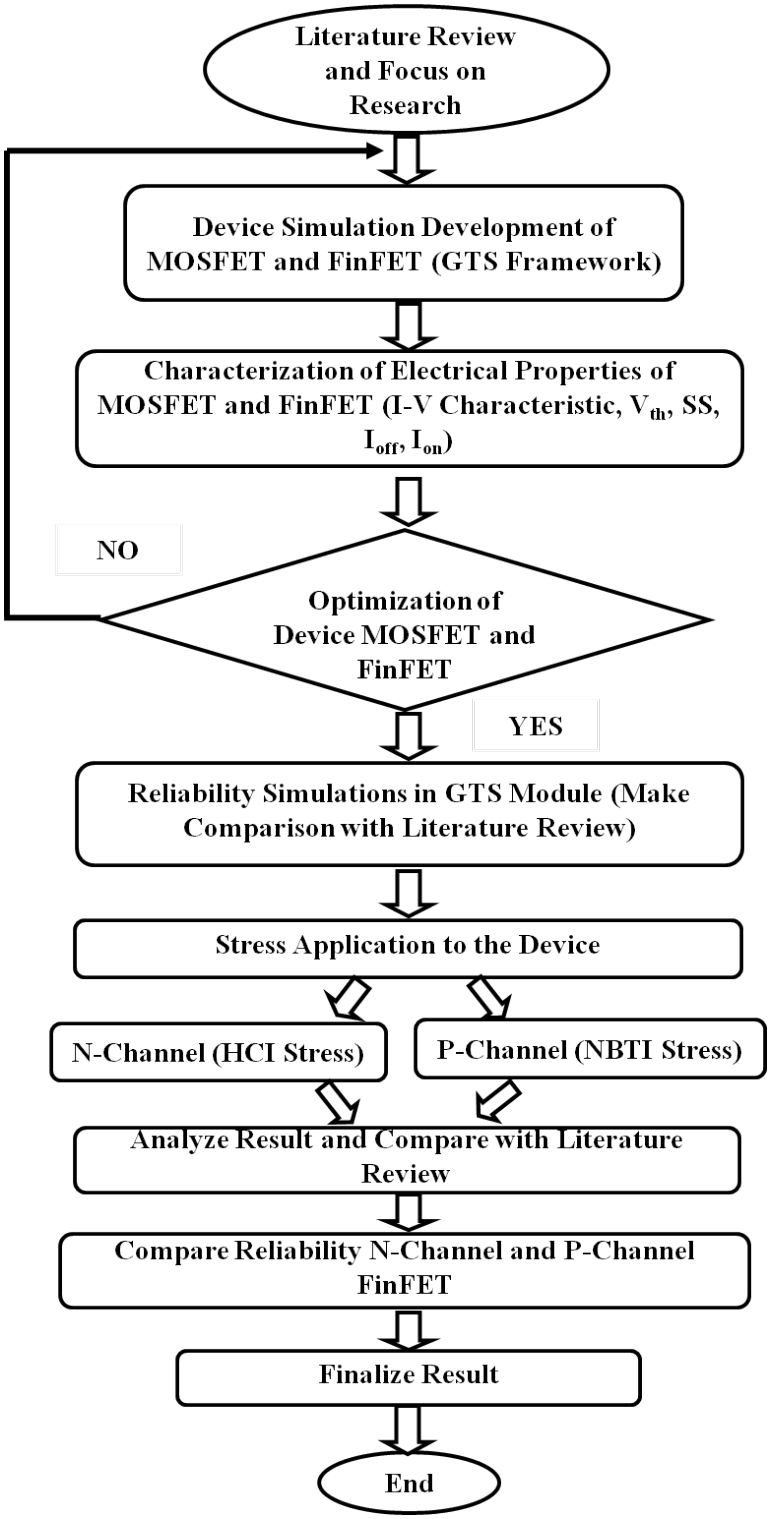

Figure 3.3: Flowchart of the Project

CHAPTER 4

RESULT AND DISCUSSION

4.1 INTRODUCTION

This chapter will briefly explained about expected outcome only, due to this project still under progress. There is no preliminary result, regarding to GTS Framework software constraints where the software still under process purchase and did not set up yet on lab.

4.2 EXPECTED OUTCOME

At the end of this project there is three expected outcome that need to accomplish. First expectation from this project is, an optimized 3D FinFET device structure is able to design using GTS Framework software. Second, the reliability behaviors between planar MOSFET and novel FinFET will be able to analyze and compare. Lastly, the reliability behaviors between n-channel and p-channel of FinFET are also be able to compare.

CHAPTER 5

CONCLUSION

As a conclusion, literature review on FinFET device structure and its reliability issues have been studied. Other than that, the stress method and conditions for both n-channel and p-channel on MOSFET and FinFET have been investigated. The device properties like channel length, oxide thickness and doping concentration have been explored too.

There are many benefits that can be obtained in term of electrical properties when the reliability behaviors of planar MOSFET and novel FinFET is compared. Besides that, it will help to finalized between planar MOSFET and novel FinFET which one can make the transistor become smaller due to their reliability behaviors and short channel length. Regarding to this, more devices can be packed in a given chip area. As a result, when the given chip area is smaller, the functionality of the chip is still same and it will obey Moore's law. Hence, the price per chip can be reduced. Therefore all procedure and work flow will be well developed in order to achieved this goal.

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