Mechatronics Engineering

SPI Communication Protocol

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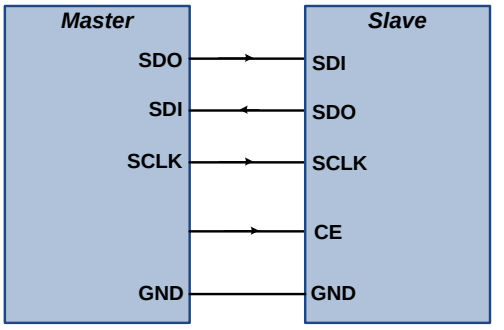
SPI Protocol

- Synchronous
- Full-duplex
- Serial
- Fast communication
- For short distances
- Pins
  - SDO (Data Out)
  - SDI (Data In)
  - SCLK (shift clock)
  - CE (chip enable)



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Master vs. Slave

- Master begins the communication by pulling down the CE pin of slave.
- Master makes the clock for communication

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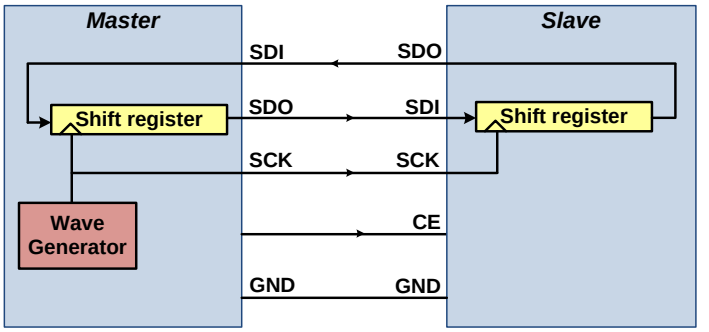
SPI internal circuit

- A shift register in the master and another in the slave
- By each clock, a bit is shifted out from the master's shift register into the slave shift register and a bit is shifted from slave to master.



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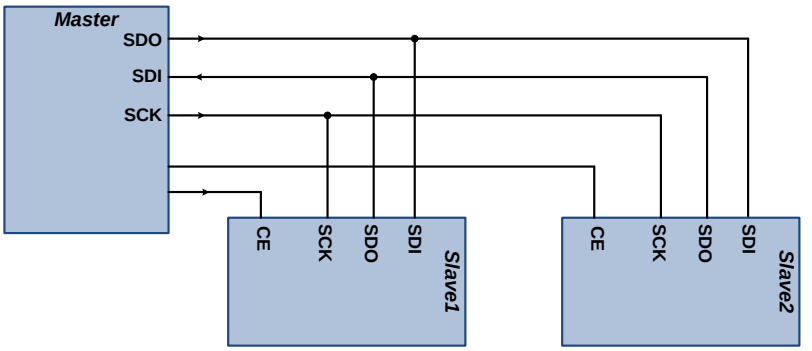
Multi-slave communication



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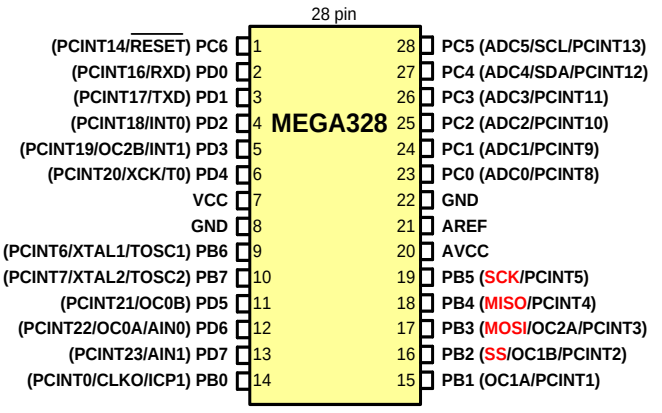
SPI pins in AVR

- MOSI (Master Out Slave In)
- MISO (Master In Slave Out)
- SCK
- SS



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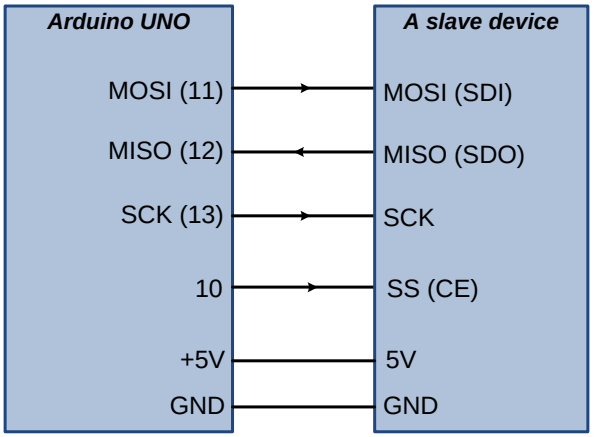
Connecting a slave device to an AVR



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AVR registers

- Control register:
  - SPCR (SPI Control Register)
- Status Register:
  - SPSR (SPI Status Register)
- Data Register:
  - SPDR (SPI Data Register)

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SPSR (SPI Status Register)

SPSR:	SPIF	WCOL	-	-	-	-	-	SPI2X

- SPIF (SPI Interrupt Flag)
  - A serial transfer is completed.
  - The SS pin is driven low in slave mode
- WCOL (Write Collision)
- SPI2X (Double SPI Speed)

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SPCR

SPCR:	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0

- SPIE (SPI Interrupt Enable)
- SPE (SPI Enable)
- DORD (Data Order)
- MSTR (Master)
- CPOL (Clock Polarity)
- CPHA (Clock Phase)
- SPR1, SPR0 :SPI Clock Rate

SPI2X	SPR1	SPR0	SCK Freq.
0	0	0	Fosc/4
0	0	1	Fosc/16
0	1	0	Fosc/64
0	1	1	Fosc/128
1	0	0	Fosc/2 (not recommended)
1	0	1	Fosc/8
1	1	0	Fosc/32
1	1	1	Fosc/64

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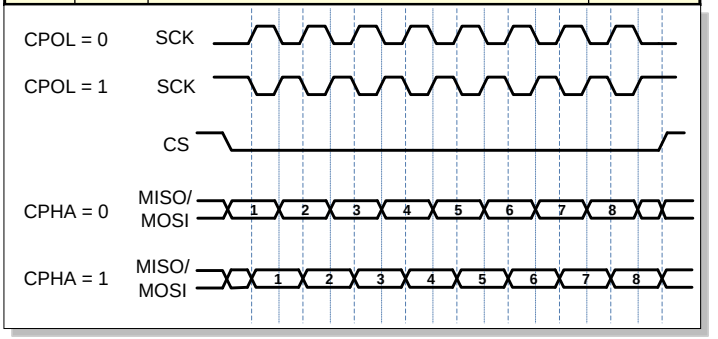
SPCR

SPCR:	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0

CPOL	CPHA	Data Read and Change Time	SPI Mode
0	0	Read on rising edge, changed on a falling edge	0
0	1	Read on falling edge, changed on a rising edge	1
1	0	Read on falling edge, changed on a rising edge	2
1	1	Read on rising edge, changed on a falling edge	3



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Program 1: Sending 'G' through SPI as a master

```
#include <avr/io.h>

#define MOSI 3
#define SCK 5
#define SS 2

int main (void)
{
 DDRB = (1<<MOSI)|(1<<SCK)|(1<<SS); //MOSI and SCK are output
 DDRD = 0xFF; //Port D is output
 SPCR = (1<<SPE)|(1<<MSTR)|(1<<SPR0); //enable SPI as master
 while(1) //do for ever
 {
  PORTB &= ~(1<<SS); //enable slave device
  SPDR = 'G'; //start transmission
  while(!(SPSR & (1<<SPIF))); //wait transfer finish
  PORTD = SPDR; //move received data to PORTD
  PORTB |= (1<<SS); //disable slave device
 }
 return 0;
}
```


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Program 2: Sending 'G' through SPI as a slave

```
#include <avr/io.h>

#define MISO 4

int main (void)
{
 DDRD = 0xFF; //Port D is output
 DDRB = (1<<MISO); //MISO is output
 SPCR = (1<<SPE); //enable SPI as slave
 while(1)
 {
  SPDR = 'G';
  while(!(SPSR &(1<<SPIF))); //wait for transfer finish
  PORTD = SPDR; //move received data to PORTD
 }
 return 0;
}
```