Mechatronics Engineering

CCP

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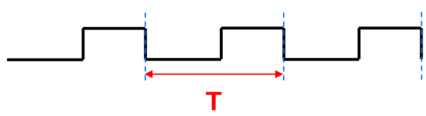
Wave characteristics

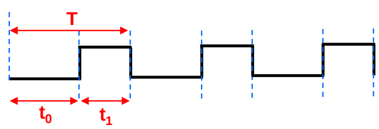
- **Period**
  - Frequency

$$f = \frac{1}{T}$$

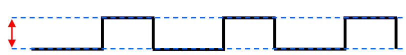


- **Duty cycle**

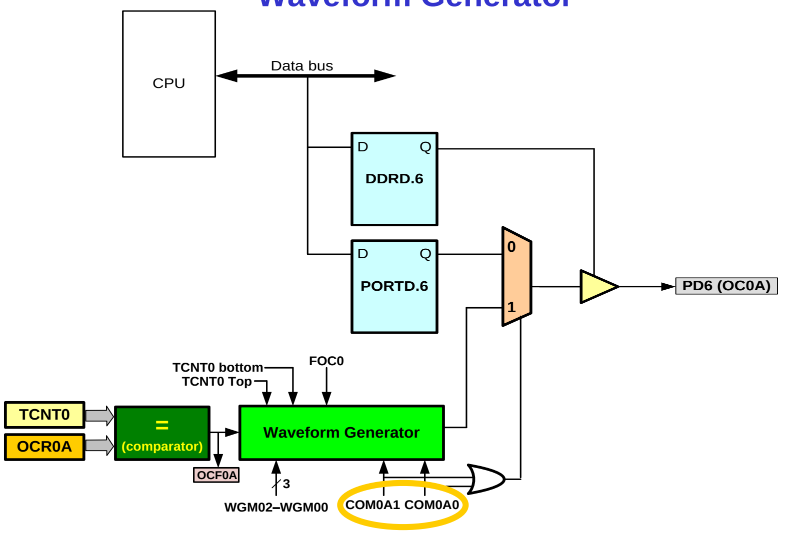
$$\text{duty cycle} = \frac{t_1}{T} \times 100 = \frac{t_1}{t_0 + t_1} \times 100$$



- **Amplitude**



Waveform Generator



COM0A1	COM0A0	COM0B1	COM0B0	-	-	WGM01	WGM00	TCCR0A

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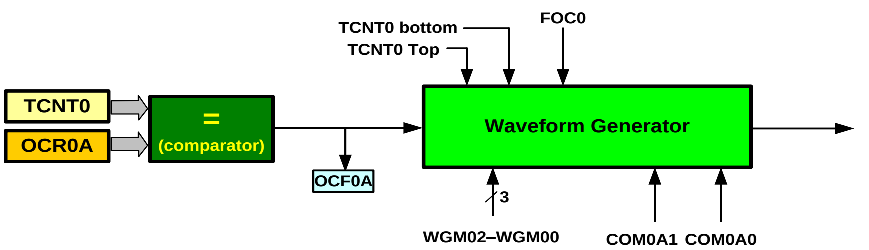
Waveform Generator



COM0A1	COM0A0	COM0B1	COM0B0	-	-	WGM01	WGM00	TCCR0A
FOC0A	FOC0B	-	-	WGM02	CS02	CS01	CS00	TCCR0B

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COM0A1	COM0A0	COM0B1	COM0B0	-	-	WGM01	WGM00	TCCR0A
FOC0A	FOC0B	-	-	WGM02	CS02	CS01	CS00	TCCR0B

Timer Mode (WGM)

WGM02	WGM01	WGM00	Comment
0	0	0	Normal
0	0	1	Phase correct PWM
0	1	0	CTC (Clear Timer on Compare Match)
0	1	1	Fast PWM
1	0	0	Reserved
1	0	1	Phase correct PWM
1	1	0	Reserved
1	1	1	Fast PWM

COM0x1	COM0x0	Description
0	0	Normal port operation, OC0 disconnected
0	1	Toggle OC0 on compare match
1	0	Clear OC0 on compare match
1	1	Set OC0 on compare match

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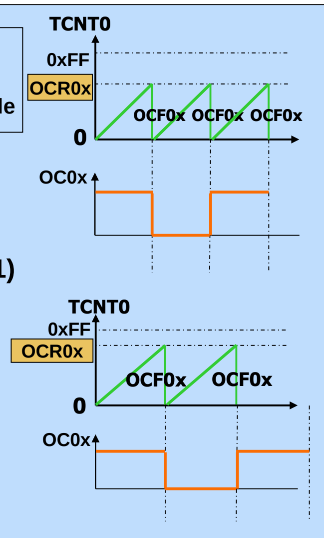
CTC, Toggle Mode
Duty cycle = 50%
Frequency = changeable

$$F_{OC0} = \frac{f_{clk}}{2N(OCR0x+1)}$$



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Assuming XTAL = 16 MHz, make a pulse with duty cycle = 50% and frequency = 1MHz

$$F_{OC0}=\frac{f_{clk}}{2N(OCR0x+1)} \Rightarrow 1MHz=\frac{16MHz}{2N(OCR0x+1)} \Rightarrow N(OCR0x+1)=\frac{16MHz}{2MHz}$$

$$\Rightarrow N(OCR0+1) = 8 \Rightarrow \begin{cases} N = 1 \text{ and } OCR0 = 7 \\ N = 8 \text{ and } OCR0 = 0 \end{cases}$$

```
OCR0A = 7;
TCCR0A = (1<<COM0A0)|(1<<WGM01); //toggle, CTC
TCCR0B = 0x01; //prescaler = 1
```

```
OCR0A = 0;
TCCR0A = (1<<COM0A0)|(1<<WGM01); //toggle, CTC
TCCR0B = 0x02; //prescaler = 8
```

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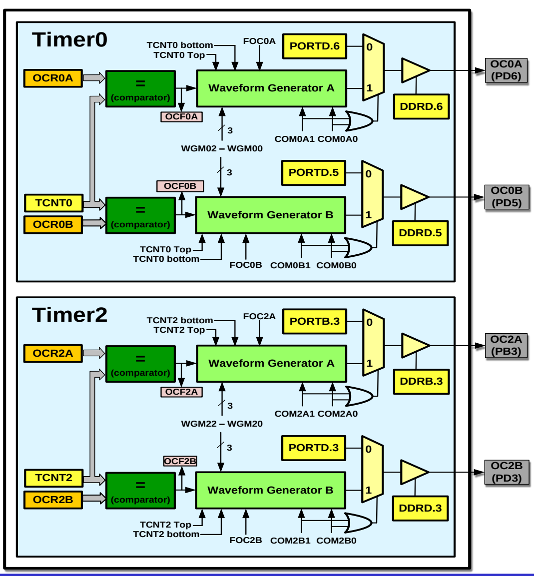
Wave generating in Timer2

- Like Timer0



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The difference between Timer0 and Timer2

- Timer0

COM0A1	COM0A0	COM0B1	COM0B0	-	-	WGM01	WGM00	TCCR0A
FOC0A	FOC0B	-	-	WGM02	CS02	CS01	CS00	TCCR0B

CS02	CS01	CS00	Comment
0	0	0	Timer/Counter stopped
0	0	1	clk (No Prescaling)
0	1	0	clk / 8
0	1	1	clk / 64
1	0	0	clk / 256
1	0	1	clk / 1024
1	1	0	External clock (falling edge)
1	1	1	External clock (rising edge)

- Timer2

COM2A1	COM2A0	COM2B1	COM2B0	-	-	WGM21	WGM20	TCCR2A
FOC2A	FOC2B	-	-	WGM22	CS22	CS21	CS20	TCCR2B

CS22	CS21	CS20	Comment
0	0	0	Timer/Counter stopped
0	0	1	clk (No Prescaling)
0	1	0	clk / 8
0	1	1	clk / 32
1	0	0	clk / 64
1	0	1	clk / 128
1	1	0	clk / 256
1	1	1	clk / 1024

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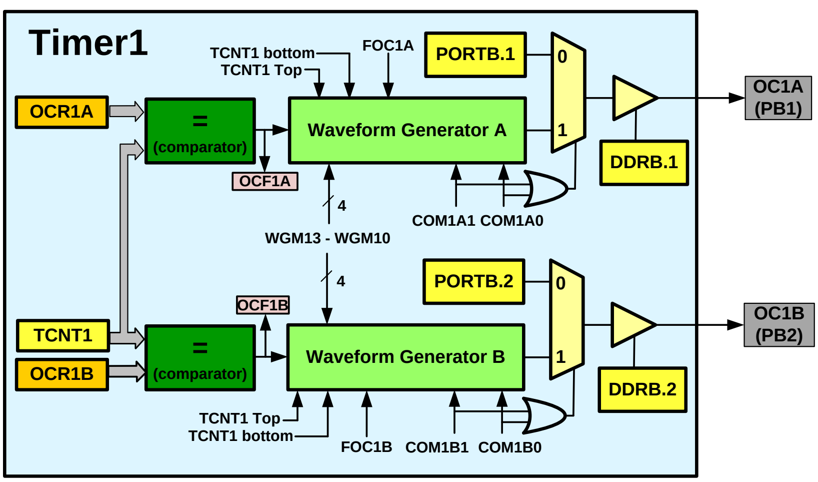
Timer1

- Timer1 has two waveform generators



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COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10	TCCR1A
ICNC1	ICES1	-	WGM13	WGM12	CS12	C	C	TCCR1B

Mode	WGM13	WGM12 (CTC1)	WGM11 (PWM11)	WGM10 (PWM10)	Timer/Counter Mode of Operation	TOP	Update of OCR1x	TOV1 Flag Set on
0	0	0	0	0	Normal	0xFFFF	Immediate	MAX
1	0	0	0	1	PWM, Phase Correct, 8-bit	0x00FF	TOP	BOTTOM
2	0	0	1	0	PWM, Phase Correct, 9-bit	0x01FF	TOP	BOTTOM
3	0	0	1	1	PWM, Phase Correct, 10-bit	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCR1A	Immediate	MAX
5	0	1	0	1	Fast PWM, 8-bit	0x00FF	TOP	TOP
6	0	1	1	0	Fast PWM, 9-bit	0x01FF	TOP	TOP
7	0	1	1	1	Fast PWM, 10-bit	0x03FF	TOP	TOP
8	1	0	0	0	PWM, Phase and Frequency Correct	ICR1	BOTTOM	BOTTOM
9	1	0	0	1	PWM, Phase and Frequency Correct	OCR1A	BOTTOM	BOTTOM
10	1	0	1	0	PWM, Phase Correct	ICR1	TOP	BOTTOM
11	1	0	1	1	PWM, Phase Correct	OCR1A	TOP	BOTTOM
12	1	1	0	0	CTC	ICR1	Immediate	MAX
13	1	1	0	1	Reserved	–	–	–
14	1	1	1	0	Fast PWM	ICR1	TOP	TOP
15	1	1	1	1	Fast PWM	OCR1A	TOP	TOP

COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10	TCCR1A
TC 1	TC 1		W 3	WGM12	CS12	CS11	CS10	TCCR1B

In non PWM modes

COM1A1:COM1A0 D7 D6 Compare Output Mode for Channel A

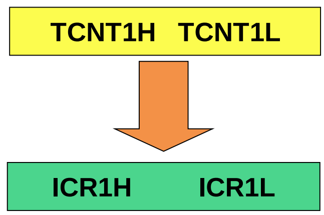
COM1A1	COM1A0	Description
0	0	Normal port operation, OC1A disconnected
0	1	Toggle OC1A on compare match
1	0	Clear OC1A on compare match
1	1	Set OC1A on compare match

COM1B1:COM1B0 D5 D4 Compare Output Mode for Channel B

COM1B1	COM1B0	Description
0	0	Normal port operation, OC1B disconnected
0	1	Toggle OC1B on compare match
1	0	Clear OC1B on compare match
1	1	Set OC1B on compare match

Capturing

- Usages
  - Measuring duty cycle
  - Measuring period



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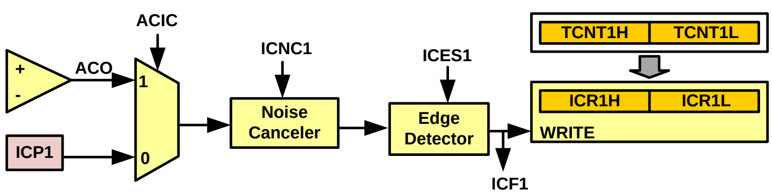
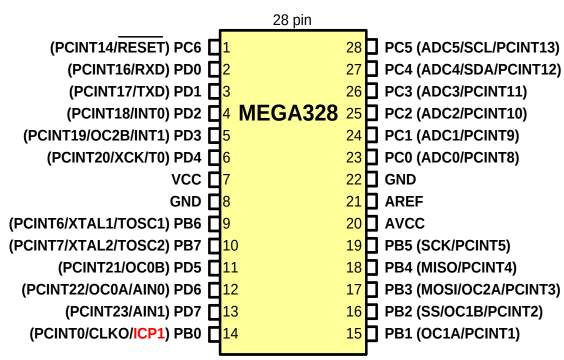
Capturing





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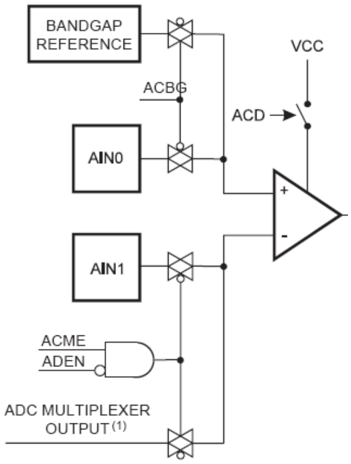
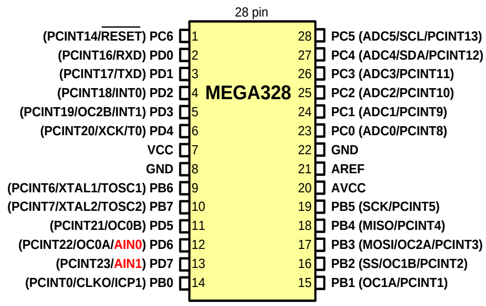
Comparator





Copied from ATmega328 datasheet page 239

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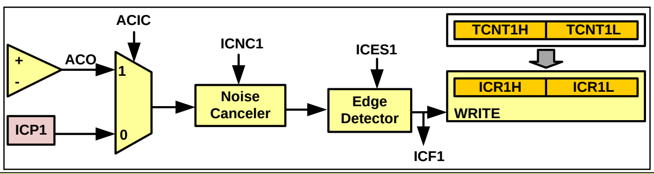

ICNC1	ICES1	-	WGM13	WGM12	CS12	CS11	CS10	TCCR1B

ICNC1: Input Capture Noise Canceller
- **0:disabled**
- **1:Enabled (captures after 4 successive equal valued samples)**

ICSES1: Input Capture Edge Select
- **0: Falling edge**
- **1: Rising edge**

	7	6	5	4	3	2	1	0	
	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	ACSR
	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	

ACIC: Analog Comparator Input Capture Enable
- **0: ICP1 provides the capture signal**
- **1: analog comparator is connected to the capturer**

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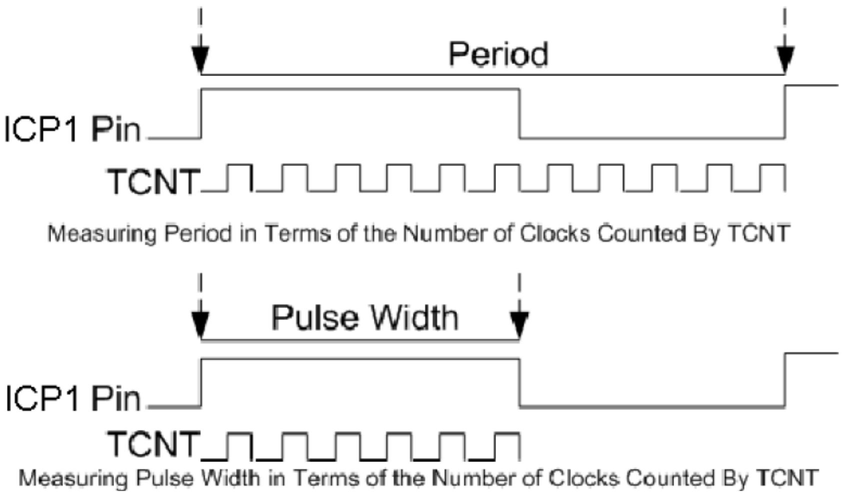
Measuring duty cycle and period



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Example: Measuring the frequency of a wave which is between 1 μs and 250 μs.

```
#include <avr/io.h>

int main ( )
{
unsigned char t1;

DDRD = 0xFF; //Port D as output
PORTB |= (1<<0);

TCCR1A = 0; //Timer Mode = Normal
TCCR1B = 0x42; //rising edge, prescaler = 8, no noise canc.

while ((TIFR1&(1<<ICF1)) == 0);

t1 = ICR1L;
TIFR1 = (1<<ICF1); //clear ICF1 flag
TCCR1B = 0x02; //falling edge

while ((TIFR1&(1<<ICF1)) == 0);

PORTD = ICR1L - t1; //pulse width = falling - rising
TIFR1 = (1<<ICF1); //clear ICF1 flag

while (1); //wait forever
return 0;
}
```

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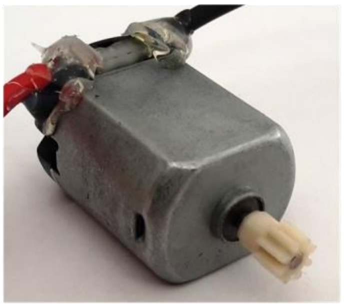
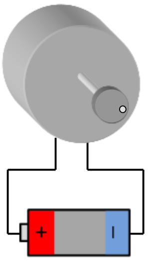
DC motor





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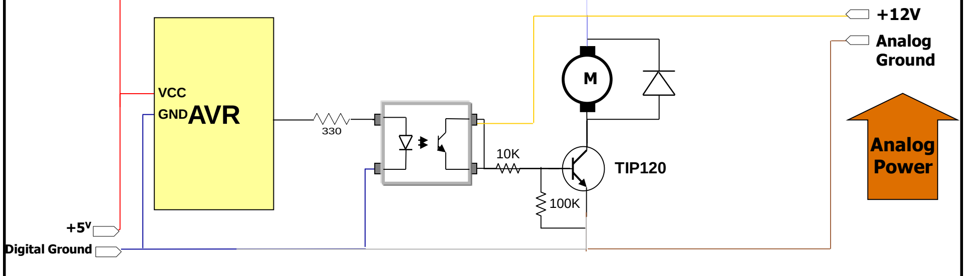
Unidirectional control



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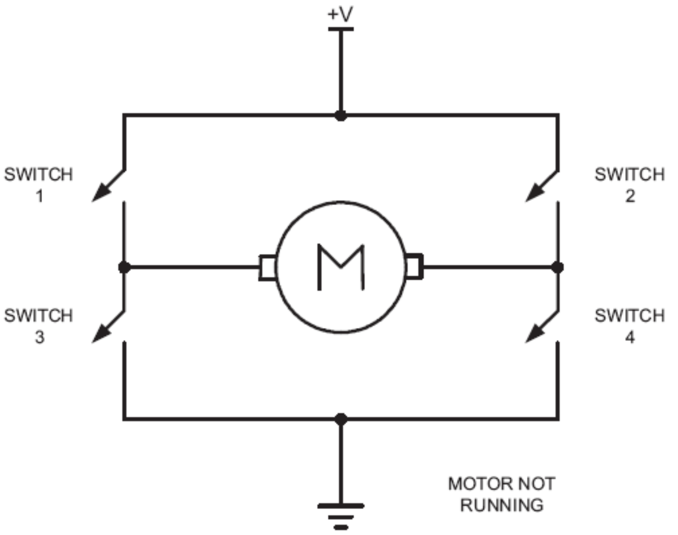
Bidirectional control



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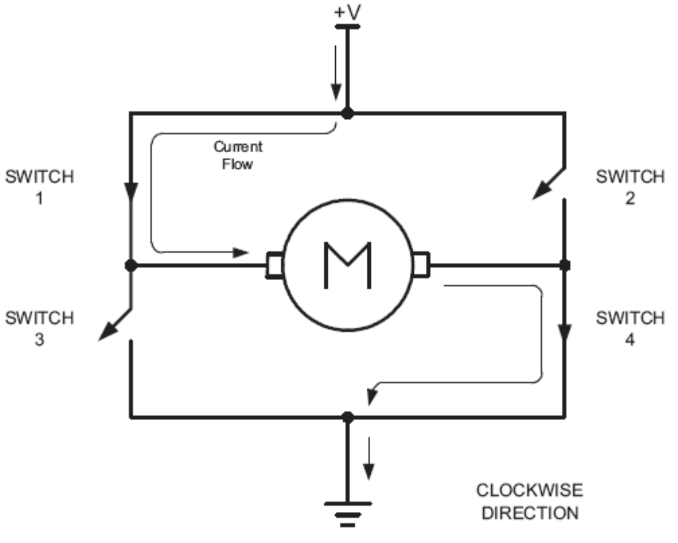
Bidirectional (clock wise)



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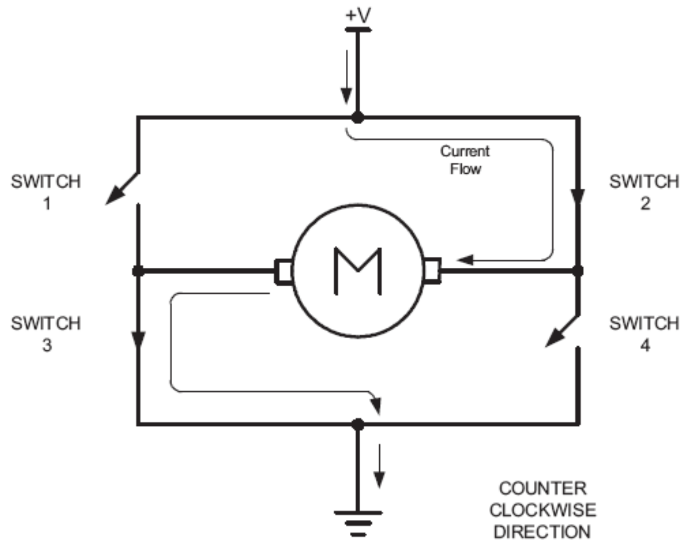
Bidirectional (counter clockwise)



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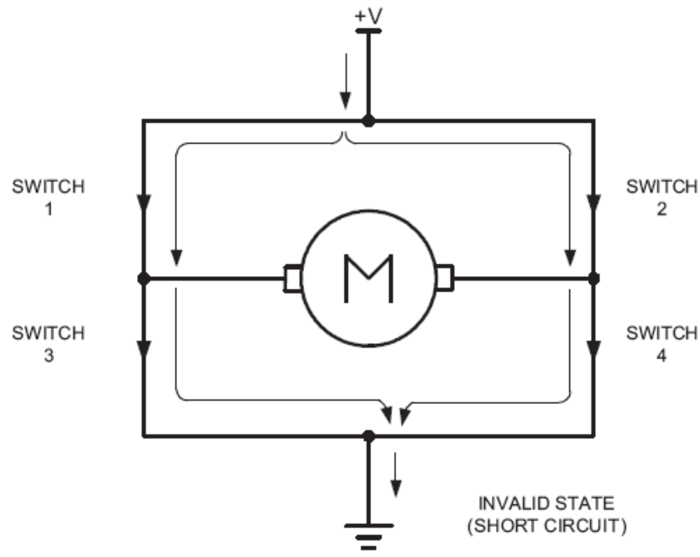
Bidirectional



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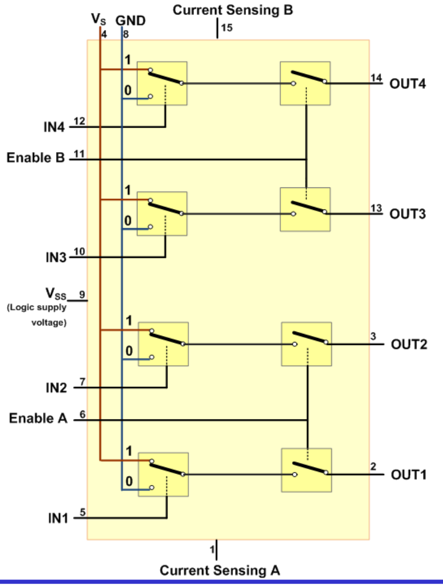
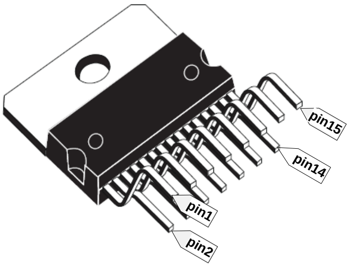
L298





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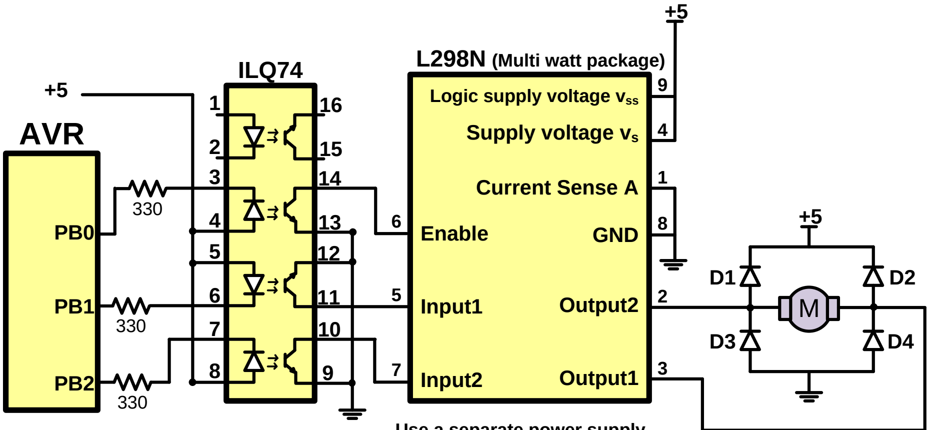
Using L298N



The optoisolator provides additional protection of the AVR

Use a separate power supply for the motor and L298N than for the AVR

D1, D2, D3, D4 are 1N4004

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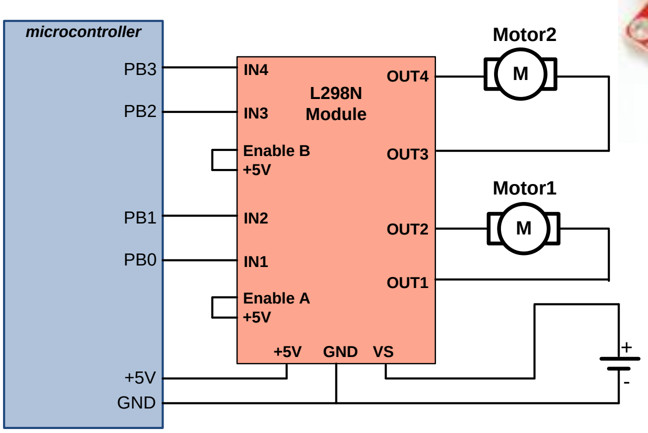
L298 module



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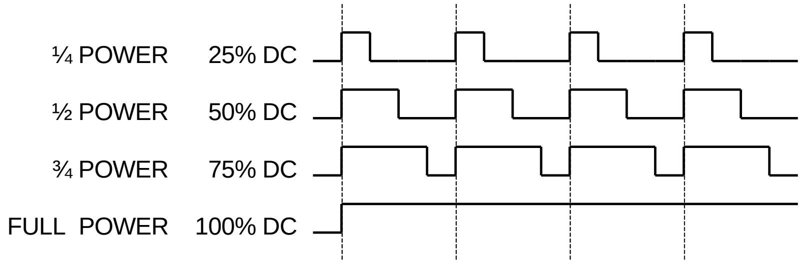
PWM and Duty Cycle



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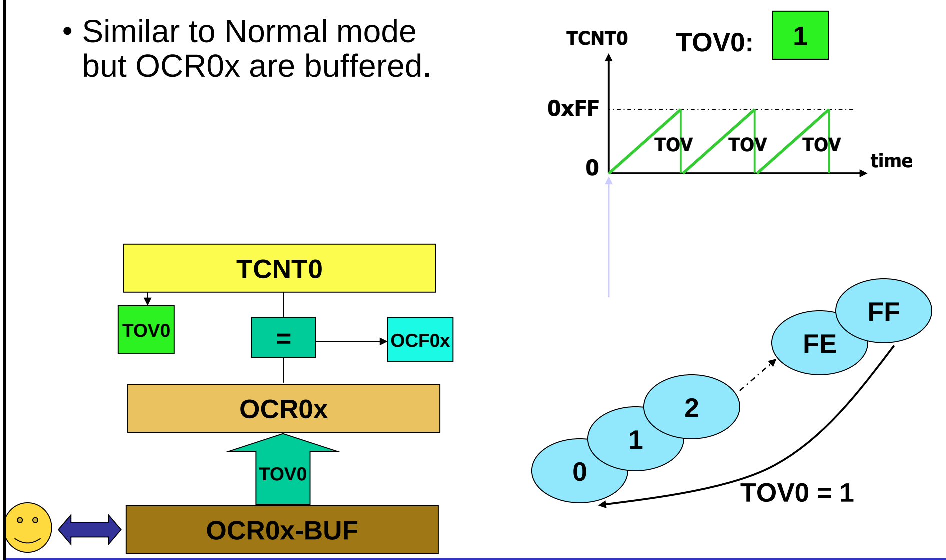
Fast PWM mode

- Similar to Normal mode but OCR0x are buffered.



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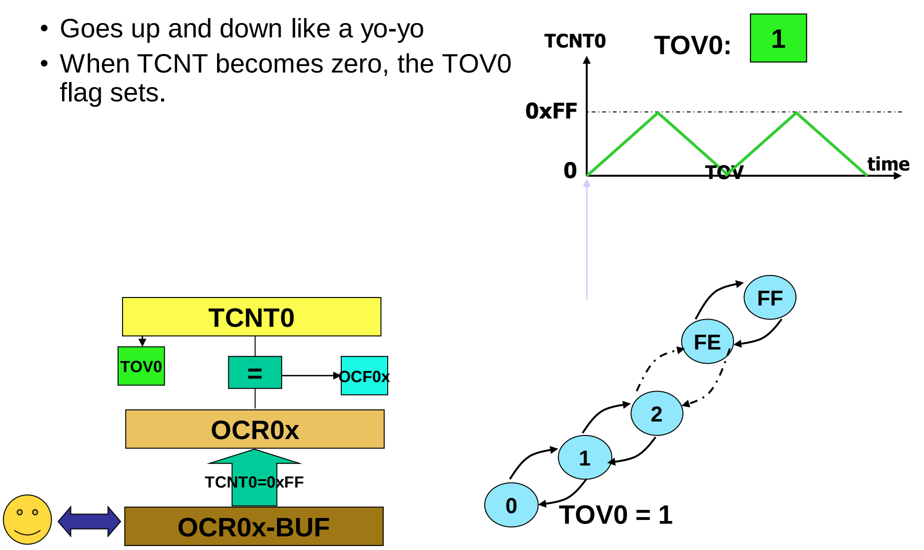
Phase Correct PWM mode

- Goes up and down like a yo-yo
- When TCNT becomes zero, the TOV0 flag sets.



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FOC0A	FOC0B	-	-	WGM02	CS02	CS01	CS00	TCCR0B
COM0A1	COM0A0	COM0B1	COM0B0	-	-	WGM01	WGM00	TCCR0A

Compare Output Mode (COM)

CTC or Normal (Non PWM)

COM0x1	COM0x0	Description
0	0	Normal port operation, OC0 disconnected
0	1	Toggle OC0 on compare match
1	0	Clear OC0 on compare match
1	1	Set OC0 on compare match

Fast PWM

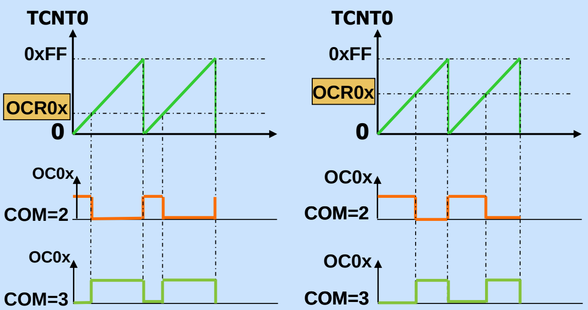
COM0x1	COM0x0	Description
0	0	Normal port operation, OC0 disconnected
0	1	Reserved
1	0	Clear OC0 on compare match, set OC0 at TOP.
1	1	Set OC0 on compare match, clear OC0 at TOP.

Phase Correct PWM

COM0x1	COM0x0	Description
0	0	Normal port operation, OC0 disconnected
0	1	Reserved
1	0	Clear OC0 on compare match when up-counting. Set OC0 on compare match when down-counting.
1	1	Set OC0 on compare match when up-counting. Clear OC0 on compare match when down-counting.

Fast PWM Calculations

Fast PWM
Duty cycle = changeable (0% to 100%)
Frequency = selectable between limited choices



$$\text{Duty Cycle} = \frac{\text{OCR0} + 1}{256} \times 100$$

$$\text{Duty Cycle} = \frac{255 - \text{OCR0}}{256} \times 100$$

$$F_{OC0} = \frac{f_{clk}}{N(256)}$$

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Assuming XTAL = 16 MHz, make the following pulse duty cycle = 75% and frequency = 62.500KHz

$$F_{OC0} = \frac{f_{clk}}{N(256)} \Rightarrow 62.500\text{KHz} = \frac{16\text{MHz}}{N(256)} \Rightarrow N = \frac{16\text{MHz}}{62.500\text{K}*256} = 1$$

75/100 = (OCR0x+1)/256 ➔ OCR0x+1 = 192 ➔ OCR0x = 191

```
DDRD |= (1<<6); //PD6 as output
OCR0A = 191;
TCCR0A = (1<<COM0A1)|(1<<WGM01)|(1<<WGM00);
TCCR0B = 0x01; //N = 1 (no prescaler)
```


FOC0A	FOC0B	-	-	WGM02	CS02	CS01	CS00	TCCR0B
COM0A1	COM0A0	COM0B1	COM0B0	-	-	WGM01	WGM00	TCCR0A

Compare Output Mode (COM)

CTC or Normal (Non PWM)

COM0x1	COM0x0	Description
0	0	Normal port operation, OC0 disconnected
0	1	Toggle OC0 on compare match
1	0	Clear OC0 on compare match
1	1	Set OC0 on compare match

Fast PWM

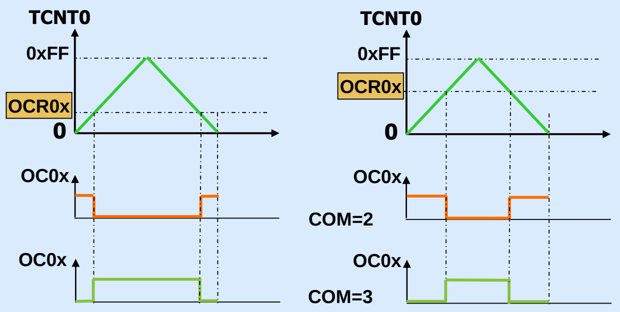
COM0x1	COM0x0	Description
0	0	Normal port operation, OC0 disconnected
0	1	Reserved
1	0	Clear OC0 on compare match, set OC0 at TOP.
1	1	Set OC0 on compare match, clear OC0 at TOP.

Phase Correct PWM

COM0x1	COM0x0	Description
0	0	Normal port operation, OC0 disconnected
0	1	Reserved
1	0	Clear OC0 on compare match when up-counting. Set OC0 on compare match when down-counting.
1	1	Set OC0 on compare match when up-counting. Clear OC0 on compare match when down-counting.

Phase Correct PWM Calculations

Phase Correct PWM
Duty cycle = changeable (0% to 100%)
Frequency = selectable between limited choices



$$\text{Duty Cycle} = \frac{OCRx}{255} \times 100$$

$$\text{Duty Cycle} = \frac{255 - OCR0}{255} \times 100$$

$$F_{OC0} = \frac{f_{clk}}{N(510)}$$

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Assuming XTAL = 16 MHz, make the following wave: duty cycle = 75% and frequency = 31.372KHz

$$F_{OC0} = \frac{f_{clk}}{N(510)} \Rightarrow 31.372\text{KHz} = \frac{16\text{MHz}}{N(510)} \Rightarrow N = \frac{16\text{MHz}}{31.372\text{K}*510} = 1$$

$75/100 = OCR0x / 255 \rightarrow OCR0x = 191$

```
DDRD |= (1<<6); //PD6 as output
OCR0A = 191;
TCCR0A = (1<<COM0A1)|(1<<WGM00);
TCCR0B = 0x01; //N = 1 (no prescaler)
```


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