Review of Silicon Photonics Technology and Platform Development

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***Abstract*— Many breakthroughs in the laboratories often do not bridge the gap between research and commercialization. However, silicon photonics bucked the trend, with industry observers estimating the commercial market to close in on a billion dollars in 2020 [1]. Silicon photonics leverages the billions of dollars and decades of research poured into silicon semiconductor device processing to enable high yield, robust processing, and most of all, low cost. Silicon is also a good optical material, with transparency in the commercially important infrared wavelength bands, and is a suitable platform for large-scale photonic integrated circuits.**

Silicon photonics is therefore slated to address the world's ever-increasing needs for bandwidth. It is part of an emerging ecosystem which includes designers, foundries, and integrators. In this paper, we review most of the foundries that presently enable silicon photonics integrated circuits fabrication. Some of these are pilot lines of major research institutes, and others are fully commercial pure-play foundries. Since silicon photonics has been commercially active for some years, foundries have released process design kits (PDK) that contain a standard device library. These libraries represent optimized and well-tested photonic elements, whose performance reflects the stability and maturity of the integration platforms.

We will document the early works in silicon photonics, as well as its commercial status. We will provide a comprehensive review of the development of silicon photonics and the foundry services which enable the productization, including various efforts to develop and release PDK devices. In this context, we will report the long-standing efforts and contributions that previously IME/A*STAR and now AMF has dedicated to accelerating this journey.

***Index Terms*— Silicon Photonics, Foundries, Optical Device Fabrication, Photonic integrated circuits**

I. INTRODUCTION

Silicon is the foundation on which the multi-billion-dollar electronics industry has been built. Billions of dollars and decades of research have been invested in to study every aspect of silicon semiconductor device processing, leading to a very mature, low-cost, high-yield, and robust process. Silicon photonics is the attempt to leverage the maturity and know-how of silicon complementary metal-oxide semiconductor (CMOS) processing techniques to apply it to the realm of photonics and opto-electronics. In doing so, researchers hoped to achieve an order-of-magnitude improvement in yield, and cost and time-to-market with less additional investment [1], [2]. To put it succinctly, silicon photonics deals with the manipulation of light in the silicon. This involves the generation, routing, modulation, processing and detection of light [3], as shown in Fig. 1. Together, these functions form the optical analogue to electronics integrated circuits (IC), so called the photonic integrated circuit (PIC).

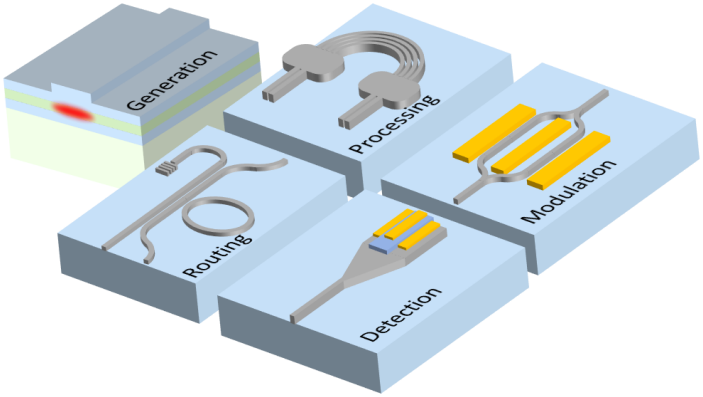

Fig. 1. Typical library components of a complete photonic integrated circuit platform: generation, routing, processing, detection, and modulation.

Silicon photonics began with the seminal paper by Soref and Bennett in 1987 [4]. This paper described the free carrier dispersion effect in silicon: how by injecting (or depleting) carriers in silicon, the material properties (refractive index n and k) can be changed. Thus, integrating a PN junction into a waveguide structure enabled the first building block of a photonic integrated circuit: a phase modulator [5], [6]. Subsequently, work began in many universities and research institutes to start to create more and more types of devices necessary for a full silicon PIC solution.

The first target was high quality waveguides. An enabling technology, the development of silicon-on-insulator wafers by Bruel [7], allowed for the confinement of light in the vertical direction, allowing lithography to define a waveguide in the plane. The original SOI waveguides were comparatively large, with several microns in width and thickness [8]. But eventually a 220 nm de-facto standard was adopted by the research community [9], [10] achieving low losses [11] and tight

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bending radii [12] along with splitters [13], crossings [14], and many other types of passive devices [15]–[17] . Still, there are ongoing arguments for thicker silicon (in the range of 300 to 500 nm) which comes with the benefit of lower waveguiding loss, relaxed tolerances for phase sensitive devices and better vertical light coupling [18]. Subsequently, silicon photonics became a hot research area, and many more components started to appear, such as directional couplers [19], multiplexer/de-multiplexer [20] and active components such as tunable micro-ring resonators [21]. Around the same time was the development of Mach-Zehnder modulators [6], [22], with the first "high speed" demonstration of 1 GHz bandwidth based on the plasma-dispersion effect [23]. A parallel development is the detection of electroluminescence from MBE-grown strained SiGe on silicon [24] and its subsequent integration into a waveguide photodetector [25]. Wafer-level high quality germanium can now be epitaxially grown on silicon [26]. The silicon photonic chip is almost complete with one key exception: a silicon laser. This is a significant hurdle as pure crystalline silicon lacks a direct bandgap precluding the possibility of monolithic silicon laser. There are two main thrusts to table this: laser integration into silicon via packaging [27], and the more ambition silicon-based lasers [28]. While the former can be and is commercially applied [29], the latter approach still struggles. A good silicon-based laser is still an active area of research after many decades [30], [31].

As the technology inched toward the market, work has begun on the next stage: packaging for silicon photonics. There are issues with packaging silicon photonic chips with fiber. The high refractive index of silicon means that there is potentially a large mode and refractive index mismatch with optical fibers, which will create large reflections and result in low coupling efficiencies. Works include high efficiency grating couplers [32], [33] and edge couplers [34], [35] have shown that reasonable coupling losses can be achieved. This trend of packaging should accelerate, which many expecting that 2.5 dimensional (2.5D) or 3 dimensional (3D) integrated photonics will be commercially deployed in the next couple of year [36], [37]. In this, 2.5D refers to where chips are interconnected through an interposer or substrate, whereas 3D refers to the stacking of optical and electrical dies.

Finally, commercially viable transceivers were being developed: in 2007, Luxtera, one of the pioneers, debuted silicon photonics transceivers for datacom market with the world's first 40G active optical cable (AOC) with a reach of up to 300 meters [38]. In 2014, Acacia debuted their silicon photonics solutions with the first 100G coherent transceiver, which could be used for metro reach applications [39]. Others soon joined the fray, debuting their own silicon photonics transceivers solutions. In 2020, the sales of silicon photonic transceivers is expected to cross 1 billion dollars, with industry observers predicting that silicon photonics will be pervasive in the coming years [40], [41].

In this paper, we will review the development efforts that enabled silicon photonics commercialization, with a focus on the development of foundry platforms and the associated device libraries. The paper is organized into four sections. Section II reviews the silicon photonics foundry platform, which will explore some of the players and some of the technologies of an open-access silicon photonics fab; Section III reviews the standard library devices offered by various foundries, and the discussion has been grouped into 4 sub-sections: (a) silicon passive devices, (b) silicon nitride passive devices, (c) modulators and (d) photodetectors, which together form a standard process design kit (PDK) device library. Finally, Section VI concludes the paper.

II. Foundry Platform Development And Foundry Services

A. Silicon photonics platforms development

Although silicon photonics is currently at its nascent commercial stage, it already has a healthy ecosystem [42], which is supported by traditional silicon industries. Already the big players in the datacom and telecom space have their own internal silicon photonics program, and this includes integrated device manufacturers [43]. There is also a healthy space for silicon photonics startups which include many different fields,

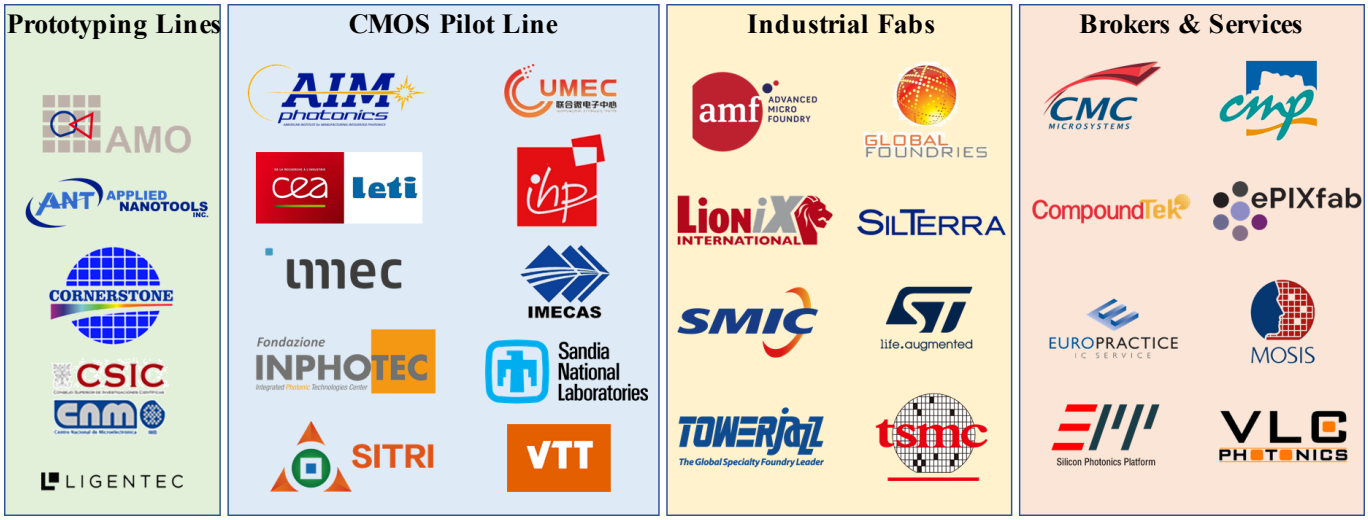

Fig. 2. Silicon photonics foundries that providing open access fabrication services. (Revised from Yole report [36])

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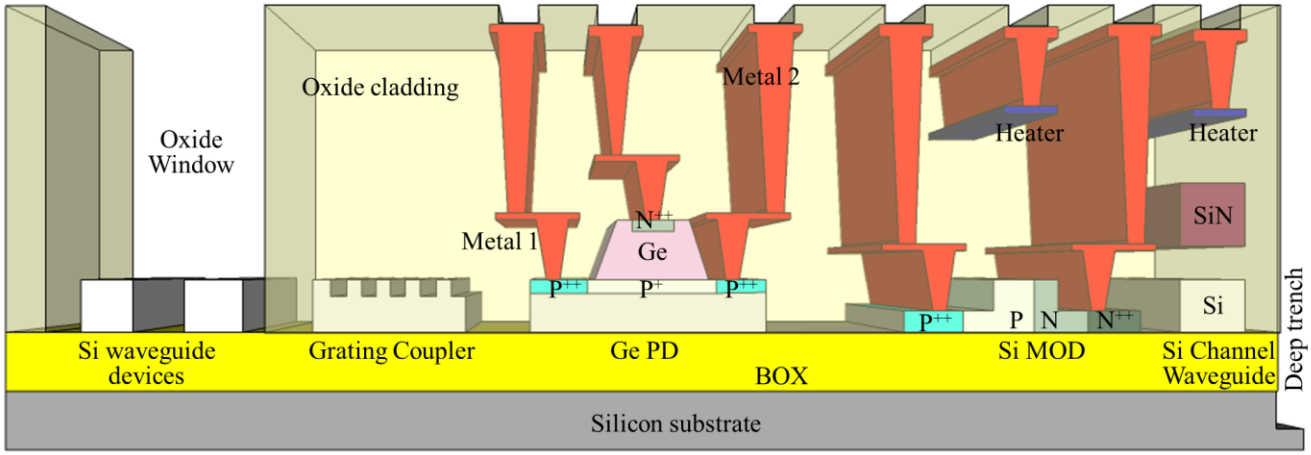

Fig. 3. Cross-sectional view of AMF's standard MPW flow. Some common elements are shown, such as phase shifters, photodiodes, and gratings.

such as design houses [44], Quantum Computing, Artificial Intelligence, etc. Additionally, there is a healthy infrastructure of supporting software. These include aspects such as computer aided design (CAD), and optical simulations. Some of the software are dedicated for optics and photonics. Others such as Cadence and Silvaco have been adapted from silicon electronics to photonics.

With such an ecosystem, it becomes viable for a silicon photonics companies or start-ups without an inordinate investment to design silicon photonic devices with purpose-built software, fab them out in a commercial foundry, package the singulated dies, and finally launch their silicon photonic product. Fig. 2 shows the silicon photonics foundries and the brokers that can provide silicon photonics fabrication services [45]. These range from prototyping lines, to pilot lines, and industrial fabs. There are also brokers who may add their own value towards industrial fabs.

For a long time, silicon photonics is based on SOI as the primary integration platform. Various silicon photonics passive and active devices can be implemented using this platform. However, for some passive devices, such as WDM, it faces the process control issue as well as the relatively large phase error due to the high index contrast of the silicon material and thus the smaller fabrication tolerance. Therefore, SiN platform starting with silicon test wafer is proposed. Although SiN platform has some unique advantages, such as extremely low propagation loss, the large fabrication tolerance; SiN itself has no active effect (except thermal tuning). In view of this, SiN-on-SOI platform is developed, leveraging on both advantages of Si and SiN platforms [46].

Fig. 3 shows the cross-sectional schematic of a typical silicon photonics integration platform that is fabricated at AMF, which include both SiN and SOI devices. The SiN waveguide layer is used for such as large-scale light routing, while all other functional passive and active devices can be formed in silicon waveguide layers. In association with it, a library of photonic elements has been released as part of a PDK. This PDK which is associated with the standard integration flow, allows external designers to reduce their own development work required. Thus, it allows customers to obtain their final designs with considerably less required runs. Similarly, AIM also published the similar work with multiple SiN waveguide layers integrated on SOI platform, showing the benefit of the extended functionalities [47].

B. Silicon photonics foundry services

In general, there are three different types of fabrication services that most foundries provide, namely multi-project wafer (MPW) service, customized service, and volume production [1]. MPW is the service that many designers can share the same mask and fabrication process. Thus, the fabrication cost is also shared among designers. Normally, MPW integration process is the most mature process in a foundry, which includes the integration modules that fulfills most of the application requirements, such as silicon waveguide, high-speed modulator, Ge photodetector, thermal heater, etc. Thus, designers can design their required integration circuits based on these provided modules. Due to the nature of having multiple projects per wafer, every step should be agreed upon. Therefore, process customization is normally either not allowed, or limited in scope as to not affect other designs. MPW services provides chips instead of wafers to designers. The chips size varies from different foundries, and thus the price.

Table I has been compiled from publicly available sources, and it compares the variable available MPW services. The table is not exhaustive; some organizations have announced the launches of their respective PDKs, yet they are not accessible publicly at the moment. We list the MPW design areas for different foundries. The chip sizes vary from very small in 10 mm^2 to over 50 mm^2. The cost tends to be around $1,000 per mm^2 for most standard active offerings. MPW runs are cost effective for prototyping, as the costs of masks and fabrication is shared amongst many projects. When these projects move towards production and require their own wafers, the cost per area will be orders of magnitude cheaper.

As shown in Table 1, most foundries adopt thin SOI, with the waveguiding silicon layer not exceeding 400 nm in thickness. This therefore will support mode sizes in the sub-micron range, which is ideal for compact and high-speed devices. However, some organizations such as VTT uses 3-micron SOI, allowing for ultra-low propagation loss at the cost of footprint and speed.

TABLE I
COMPARISON OF FOUNDRY INTEGRATION PLATFORMS

Foundries (Platform)	MPW Platform	Wafer size (mm)	Film thickness (nm)	Process Line	Minimum CD (nm)	Typical MPW area (mm^2)	Reference
AMF (MPW)	SOI passive with heater	200	220nm Si	193nm	120	44.8	[48]
	PSIN-on-SOI passive with heater	200	220nm Si	248nm for SiN/ 193nm for Si	300 (SiN) / 120 (Si)	44.8	[48]
	SOI active	200	220nm Si	193nm	120	44.8	[48]
	PSIN-on-SOI active	200	400nm SiN 220nm Si	248nm for SiN/ 193nm for Si	300 (SiN) / 120 (Si)	44.8	[48]
AIM (MPW)	SOI	300	220	193nm (Immersion)	100	50	[47], [49]
CEA-Leti (Si310-PHMP2M)	SOI	200	310	193nm	80	-	[50]
Cornerstone (MPW)	SOI	200	220/340/500	248 nm	200	56.2	[51]
GF (90WG)	SOI	300	170	193nm (Immersion)	90	25	[52]
IHP (SG25H5-ePIC)	SOI	200	220	248nm	-	10	[53]
IMEC (iSiPP50)	SOI	200	220	193nm	130	26.5	[54]
VTT (MPW)	SOI	150	3000	UV	-	50	[55]

MPW is an ideal platform for proof-of-concept or research-based projects. However, for most silicon photonics projects, especially for advanced applications, various additional process modules or process variations are required to reach the specific design performance. These additional process changes may break compatibility with the MPW process flow. In such cases, customized fabrication services are available. For customized service, it is feasible that both the designers and the foundry can discuss and finalize the integration process flow, including variations experiments. Such process variations may include but not limited to:

- customized implantation conditions in order to achieve specific concentrations or different PN junction profiles such as L-shaped or U-shaped PN junctions.
- customized Si/Ge thickness for performance enhancement or different Ge stack layers for such as Avalanche Photodiode (APD).
- additional waveguide layers, such as the integration with LPCVD SiN waveguide layer, or even two or three PECVD SiN waveguide layers.
- additional metal routing layers if the interconnect circuits are extremely large.
- enhanced functionalities using additional process capability, such as oxide trench with under bump metallization (UBM) and solder bump for laser diode packaging, or V-groove for fiber assembly.

With enhanced functionalities provided by these additional processes, the fabricated silicon PIC can fulfill specific requirements imposed by various applications.

III. SILICON PHOTONICS PDK DEVELOPMENT

Many open-access foundries develop and provide silicon photonic building blocks in the form of a process design kit (PDK). This PDK serves as a starting point for silicon photonics designers to design circuits for their applications, without investing the monumental work of individual device research. The performance of these PDK devices tend to be high, as each foundry will maximize the performance of each individual device within the library over many runs. However, these typically are not the true limit of each platform, and many foundry customers engage in their own research and development work to create their specifically required components with optimized performance.

Table II shows the PDK building blocks that are offered by some of the foundries with corresponding performances. Here we only list some of the key devices (modulators, detector, passive devices, and coupling devices), which will form the backbone of most silicon photonics integrated circuits. Modulators and detectors are important for encoding and decoding information from the optical to the electrical domain and vice versa. Passive devices are required to perform optical functions (filtering, delay, phase control) and coupling devices are required to couple in and out light from external lasers and fibers. For the modulators and detectors, we have chosen MZM and Ge PDs as baselines for comparison. These are the primary options for modulations and detector. We have used the passive propagation loss and the excess loss of the 1×2 MMI as proxies for the passive device performance. Additionally, we report the performance of both grating and edge couplers where available.

Conventionally, to ensure the performance of such library devices to be successfully implemented, the end-users need a stable integrated photonic production line as well as several rounds of trail runs prior the actual production. To simply the developing routine for all the users, typical foundries including AMF provide PDK devices library, which developed under the design of experiment (DOE) approach, and optimal design was presented. In the following section, we will discuss various PDK elements available to designers with 4 main categories: (a) SOI passive devices, (b) SiN devices, (c) modulators, and (d) photodiodes. Together, these 4 types of components can be built to allow many different types of functions in a photonic integrated circuit.

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TABLE II
LIST OF PDK DEVICE AND THE PERFORMANCE FROM DIFFERENT FOUNDRIES

Institution (Platform)	Mach-Zehnder Modulators	SiGe Detector	Passive Devices	Edge Coupling	Ref.
AMF (MPW)	BW: > 40 GHz @ -2V IL: 4 dB Vπ: 6.29V Length: 4 mm	BW: 35 GHz @ -2V R: 0.85 A/W ID: 30 nA Bias: -2V	Loss: 1.4 dB/cm (500 nm × 220 nm Rib) 1×2 MMI: 0.3 dB	1.2 dB SMF	[48]
AIM (MPW)	Speed: 50 Gbps IL: 2.7 dB VπL: 0.8 V-cm @ -1V Length: 1 mm	BW: 50 GHz R: 1 A/W ID: 40 nA Bias: 1V	Loss: 0.9 dB/cm (Low Loss Rib)	1.5 dB SMF	[47], [49]
CEA-Leti (Si310-PHMP2M)	BW: 40GHz @ -2V IL: 2.4 dB VπL: 2 V-cm Length: 3 mm	BW: 35 GHz R: 0.75 A/W ID: 50 nA Bias: -1V	Loss: 2dB/cm (Rib) 1×2MMI: 0.5 dB	-	[50]
GF (90WG)	BW: 27 BHz @ -2V IL: 3.5 dB VπL: 1.54 V-cm Length: 3 mm	BW: 39 GHz R: 1 A/W ID: 70 nA Bias: -1V	Loss: 2.2 dB/cm (170 nm × 350 nm Rib) Multimode Rib	0.7 dB Metamaterial waveguide SMF	[52]
IHP (SG25H5-ePIC)	BW: - IL: - VπL: 3.0 V-cm Length: 7 mm	BW: 60 GHz R: 0.8 A/W ID: 200 nA Bias: -2V	Loss: 2.5 dB/cm (500 nm × 220 nm Rib)	-	[53]
IMEC (iSiPP50)	BW: 37 GHz @ -2V IL: 2.5 dB Vπ: 12V Length: 1.5 mm	BW: 50 GHz R: 0.9 A/W ID: 50 nA Bias: -1V	Loss: 1.4 dB/cm (450 nm × 220 nm Rib)	2 dB Lensed fiber	[54]
VTT (MPW)	BW: Up to 2.5 MHz	BW: 35 GHz R: 0.8 A/W ID: 1 uA Bias: -1V	Loss: 0.1 dB/cm (3 um × 3 um Strip) 1×2 MMI: 0.2 dB	1 – 1.4 dB SMF	[55]

A. SOI Passive Devices

SOI passive devices refer to a set of devices that does not require supplying an electrical signal (particularly a high-speed RF signal). Passive devices are fundamental building blocks with many devices included. Functionality-wise, it covers optical coupling, routing, and processing for integrated photonic circuits. Among these devices, waveguides are the most fundamental building block in all the open access foundry's PDK elements. Based on a foundry's standard process technology, most of them provide three consecutive etching steps to serve different purposes. For example, in AMF's case: starting from 220 nm silicon, we first etch 70 nm Si to form the grating couplers, followed with another 60 nm etch to form a 90 nm slab region. Finally, this 90 nm Si will be fully removed in some of the region to form channel waveguide. As part of process control and monitoring, the remaining silicon thickness is tracked after every etching step.

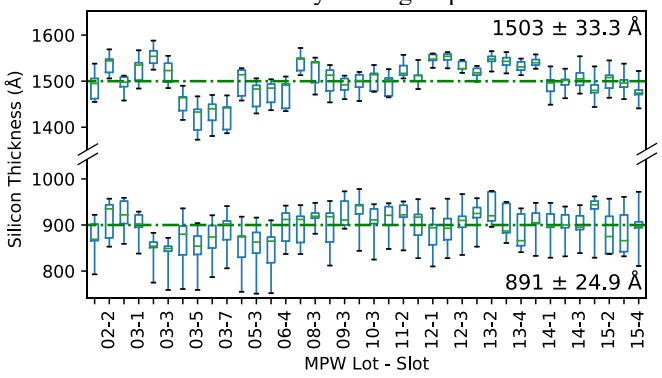

Fig. 4. The statistical data of the remaining silicon thickness corresponding to grating coupler and slab waveguide, measured from multiple MPW wafers. The dotted green line represents the target thicknesses of 1500Å and 900Å.

Fig. 4 shows an example of the remaining silicon thickness corresponding to the targets of 1500 Å and 900 Å, which is compiled from MPW wafers running in AMF in 2019 and 2020. The target thicknesses of 1500 Å and 900 Å, the average thickness is 1503±33.3 Å and 891±24.9 Å respectively.

For most of the foundries with 8-inch wafer capability, silicon waveguides are patterned using 248 nm (KrF) photolithography, with the minimum structure critical dimension of around 180 nm. With dry 193 nm (ArF) tool, AMF has enabled higher resolution photolithography. The benefit of this is the better control of structure critical dimension (CD), with enhanced wafer level uniformity as well as wafer to wafer repeatability. Fig. 5 shows the CD control data from multiple MPW wafers for the waveguide with 500 nm in width, with the average of 499±6.4 nm.

Silicon waveguide loss is dominated by sidewall scattering, which is associated with the optical lithography and further aggravated in the dry-etching process.

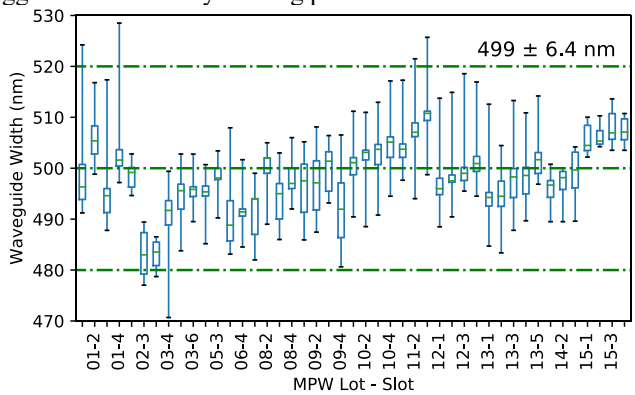

Fig. 5. The statistics of the waveguide width measured from multiple MPW wafers.

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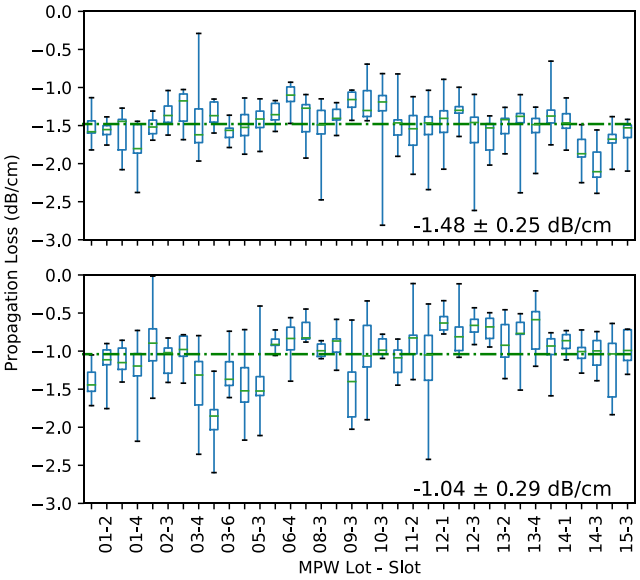

Fig. 6. Statistical propagation losses of the (top) channel waveguide and (bottom) slab waveguide from multiple MPW wafers.

While literature has reported ultra-low losses for SOI waveguides, most of the work focused on improving the line edge roughness (LER). As shown in Table I, silicon photonics foundries typically employ commercially available 193 nm / 248 nm lithography, which then typically produce losses remains in the range of 1-2 dB/cm (shown in Table II). To improve the sidewall roughness, which will achieve better waveguide propagation loss and lower random phase error, post-processing methods such as oxidation and H_2-annealing [56] are adopted.

TABLE III
Typical Performance of AMF SI PDK Library Devices

Device	Wavelength	Performance
Edge Coupler	C band	Loss TE: <1.30dB/facet Loss TM: <1.25dB/facet
Grating coupler	C band	Loss<4dB/facet 1dB bandwidth~40 nm
1-by-2 MMI	C band	Loss <0.1 dB Imbalance<0.1 dB
2-by-2 MMI	C band	Loss <0.3 dB Imbalance<0.15 dB
Crossing	C band	Loss<0.15 dB Crosstalk < -40 dB
PBS	C band	Loss TE: 0.3dB Loss TM: 0.3 dB PER: ~17dB
PBRS/PBRC	C band	Loss TE: 0.1dB Loss TM: 0.3 dB PER: ~20dB
Edge Coupler	O band	Loss TE: <1.64dB/facet Loss TM: <1.25dB/facet
Grating coupler	O band	Loss<4dB/facet 1dB bandwidth~40 nm
1-by-2 MMI	O band	Loss <0.2 dB Imbalance<0.1 dB
2-by-2 MMI	O band	Loss <0.4 dB Imbalance<0.1 dB
Crossing	O band	Loss <0.15 dB Crosstalk < -40dB

However, these post-process methods affect the geometry and width of patterned elements, and therefore bring unexpected variation (such as CD variation, phase error, etc.) for the other photonic devices. As a result, usage on these methods may not be recommended in foundry process. Another method to reduce sidewall roughness is to use advanced lithography technology such as immersion 193nm lithography, and/or implement the phase-shift mask (PSM) to further reduce the process variability [57].

To ensure the stable integration process by tracking the waveguide loss performance, wafer-level testing is required in order to perform in-line optical loss characterization at any stage of the wafer processing. Normally, waveguide cutback structures with grating couplers are used as process control monitor (PCM). Fig. 6(a) shows the statistics of the propagation loss from AMF's MPW wafers. It shows that the channel waveguide propagation loss is 1.48 ± 0.25 dB/cm, while the slab waveguide propagation loss is 1.04±0.29 dB/cm.

Giving such silicon waveguide, we develop various silicon passive PDK devices. Without detailing in each individual device, Table III lists the typical performance of AMF Si passive PDK library devices.

B. SiN Passive Devices

Silicon Nitride (SiN) is a CMOS-compatible material for the photonic integrated circuits (PICs) [58], and can provide complementary functions in a silicon photonics chip. While the transparency range of silicon is only between 1.1 μm to 4 μm [59], [60],[44], SiN covers a broad operation range from visible (~400 nm) to the mid-infrared wavelength (~4 μm), expanding the PIC to various applications, such as biochemical sensors at visible light [61], [62], LiDAR application [63], telecom and datacom [64], and optical gas sensing in mid-infrared range [65]. The index-contrast between SiN and oxide cladding layer is only 38% [66],[45],[46], leading to a wider waveguide and therefore the larger radius for bend waveguide. For non-linearity characteristic, Si suffers from two-photon absorption when wavelength is below 2.2 μm, causing insufficient efficiency for nonlinear processes. In contrast, the two-photon absorption is zero for SiN. Furthermore, the weak two-photon absorption and low waveguide loss make SiN material to be suitable for non-linearity applications requiring high optical power, especially in resonant structures with high quality factors like frequency comb generation, supercontinuum generation [47]–[50]. The thermo-optic coefficient for Si and SiN are 1.86×10^{-4} K^{-1} and 2.45×10^{-5} K^{-1} at 1.55 μm, respectively. Hence, SiN is suitable for temperature insensitive application [66].

SiN can be prepared by either low-pressure chemical vapor deposition (LPCVD) or plasma-enhanced chemical vapor deposition (PECVD), enabling multiple SiN waveguide layers and be flexible for photonic integrated circuits with enhanced circuit performance and expanded functionality. The LPCVD SiN deposition process is at high temperature (>700 °C), while PECVD SiN is deposited at low temperatures. Such different thermal budget results in different integration process [70].

LPCVD SiN provides the homogeneity of material index, which suggests the deposited SiN is close to stoichiometric Si_3N_4.

TABLE IV
SUMMARY FOR SIN PROCESSES AT DIFFERENT FOUNDRIES

Platform (Foundry)	Material	Thickness (nm)	λ(nm)	Loss (dB/cm)
TriPlex (LioniX)	LPCVD	300/350/300 (double layer)	504-1000	<0.1 [71], [72]
		170/500/170 (double layer)	1550	<0.1 [73]
		800-1200 (Buried)	1550	<0.01 [63], [74]
LGT-AN800 (LigenTec)	LPCVD	800	1550	0.067 [75], [76]
LGT-AN150 (LigenTec)		150	405-1000	0.1
BIOPIX300 (IMEC)	PECVD	300	650-1000	0.45 [77]
BIOPIX150 (IMEC)		150	650-1000	0.6-2.1

On the other hand, PECVD could reach different SiN film with different compositions, such as silicon-rich (higher index than Si_3N_4) and nitrogen-rich (lower index than Si_3N_4) SiN films. For both LPCVD and PECVD SiN, there is an absorption window around 1520 nm due to the N-H and Si-H bonding [78]. In order to eliminate such absorption loss, high temperature annealing is normally adopted in order to remove the hydrogen bond. As a result, LPCVD SiN typically has lower losses at 1520 nm wavelength range compared to PECVD SiN.

Moreover, due to the high temperature process, LPCVD SiN films may crack due to high film stress. Thus, it is challenging to deposit thick LPCVD SiN film. In order to overcome this issue, the damascene process, similar to the dense filler pattern surrounding the waveguides [75], and mechanical trenches process [79] were developed.

With regarding to the standard fabrication services, there are multiple foundries offering different kinds of SiN integration process aiming for different applications, including LioniX [80], LigenTec [81], IMEC [82], etc. Table IV summarizes some of the typical SiN technologies from these foundries.

TABLE V
SUMMARY FOR AMF SIN PLATFORMS OVER VARIOUS WAVELENGTHS

Wavelength (nm)	Mode	SiN Thickness (nm)	LPCVD SiN (dB/cm)	PECVD SiN (dB/cm)
430-464 [83]	TE/TM	200	<9.0	< 5.5
466-500 [83]	TE/TM	200	<5.4	<4.0
502-550 [83]	TE/TM	200	<3.5	<2.9
552-600 [83]	TE/TM	200	<2.5	<2.5
552-648 [83]	TE/TM	200	<1.7	<2.4
1310 [84]	TE	400	<0.30	<0.2
1550	TE	400	<0.42	<3.01
1580	TE	400	<0.22	<1.25
2000	TE	600	--	2.5

AMF provides the complete solution with different SiN integration platforms at different thicknesses. It offers both pure SiN only platform for passive application, as well as SiN integrated on SOI wafer with enhanced functionalities. With regarding to operation wavelengths, we develop the integration platforms, which could be applied for life-science application in visible light range, LiDAR application from 600 nm to 1550 nm, telecommunication and optical transceiver at 1310 nm and 1550 nm, and optical gas sensing in mid-infrared range. Table V summarizes the details of the SiN processes with single-mode operation from visible to traditional telecommunication wavelength and infrared wavelength regions. As an example, Fig. 7(a) and (b) show the wafer-level loss distribution of the LPCVD and PECVD SiN waveguides at 1550nm. The loss is respectively 0.37 ± 0.157 dB/cm and 3.00 ± 0.181 dB/cm.

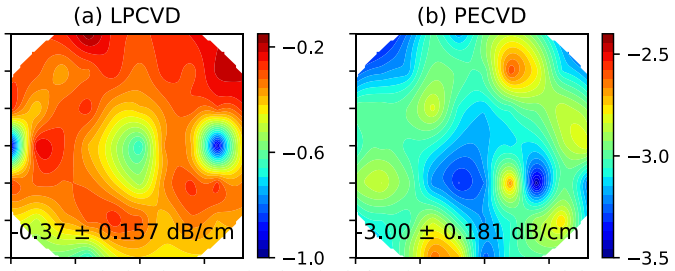

Fig. 7. Wafer level propagation loss in dB/cm for (a) PECVD and (b) LPCVD SiN waveguide at 1550nm.

With the most sophisticated silicon photonics integration platform aiming for telecommunication application operating at 1310nm and 1550nm wavelength ranges, we developed various SiN PDK devices using both LPCVD and PECVD SiN, including such as grating coupler, MMI splitter, crossing, directional coupler, etc. Table VI lists the typical performance of AMF SiN PDK library devices.

TABLE VI
TYPICAL PERFORMANCE OF AMF SIN PDK LIBRARY DEVICES

Device	Wavelength	Performance
Grating coupler	C band	Loss<5dB/facet 1dB bandwidth~50 nm
1-by-2 MMI	C band	Loss <0.3 dB Imbalance<0.2 dB (0.3)
2-by-2 MMI	C band	Loss <0.7 dB (0.3) Imbalance<0.3 dB
Crossing	C band	Loss<0.35 dB Crosstalk < -30 dB
Grating coupler	O band	Loss<5dB/facet 1dB bandwidth~40 nm
1-by-2 MMI	O band	Loss <0.2 dB (0.3) Imbalance<0.1 dB (0.3)
2-by-2 MMI	O band	Loss <0.7 dB (0.3) Imbalance<0.3 dB
Crossing	O band	Loss <0.2 dB (0.16) Crosstalk < -30dB

In order to leverage the advantages for both SOI and SiN functionalities, we develop SiN-on-SOI integration platform using both LPCVD and PECVD SiN, forming multiple waveguide system. This can be seen in the cross-sectional diagram (Fig. 3). In such integration platform, all the Si and SiN PDK devices can be integrated, while the light transition between different waveguide layers is through spot-size converters with low-loss vertical coupling. As for the inter-layer oxide thickness between SiN and Si waveguides, it is set to be 150 nm for LPCVD SIN-on-SOI platform, while it is 250 nm for PECVD SiN-on-SOI platform.

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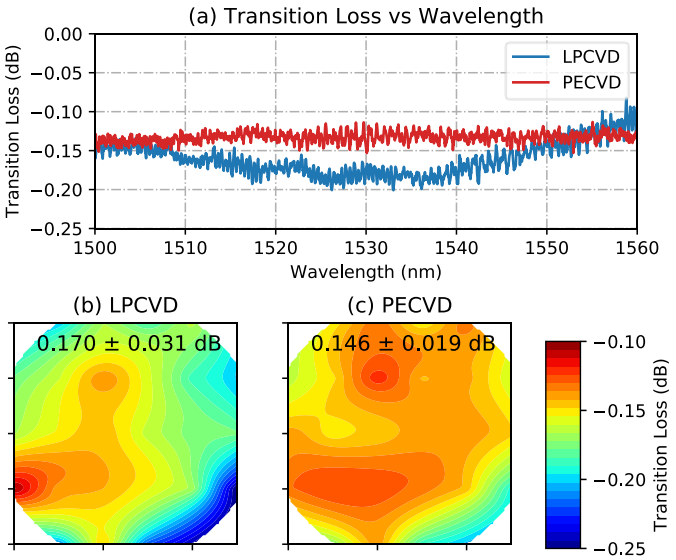

Fig. 8. SiN-to-Si vertical coupling transition loss for TE mode for both LPCVD and PECVD SiN waveguide. (a) Over whole C band. Wafer-level uniformity plots for (b) LPCVD and (c) PECVD SiN platforms.

Fig. 8 shows the vertical transition loss of TE mode for both LPCVD and PECVD SiN integrated platforms. Over the whole C band, the transition loss is less than 0.2 dB. From the wafer-level contour plot for both LPCVD and PECVD SiN integrated platform, the loss distribution is uniform over whole 8-inch wafer, with respectively the transition loss of 0.17±0.03 dB and 0.15±0.02 dB.

C. High-Performance Silicon Modulators

An optical phase shifter is an important element in photonics integrated circuit, as phase and intensity are two key methods for transmitting data optically. Phase shifters in silicon photonics typically utilize one of two effects: thermal effect and plasma dispersion effect [85]. While thermal effect is a rather slow modulation effect limited by heat dissipation, the high-speed modulation in silicon is mainly from plasma dispersion effect.

The plasma dispersion effect is particularly important in silicon photonics, as it can operate well into the tens of GHz. To make a useful device from plasma dispersion, we integrate a PN junction into a waveguide, and supply it with voltage across the junction, injecting or depleting carriers. Such a device is shown in Fig. 9(a).

A phase shifter can be structured into a Mach-Zehnder Interferometer (MZI) configuration to form an intensity modulator. The input beam splits into two arms, respectively a reference beam and a modulated beam. The phase difference between the two beams produces either constructive or destructive interference at the output port, thus creating an intensity modulator. In practice, both arms are modulated albeit in opposite phase directions, in principle halving the required voltage per arm to obtain the same voltage-intensity relation. This is shown in Fig. 9(b), which is the transmission spectrum of a Mach-Zehnder modulator with imbalanced arms, upon different applied voltages. A micro-ring modulator (MRM) is a variant of this idea, as shown in Fig. 9(c). By modulating the effective length of the cavity, for a fixed wavelength the transmission can be tuned towards or away from a resonant condition. This results in some nonlinearity, but the footprint and modulation efficiency can be better than MZM configuration. As can be seen by the zoomed-in graph, the modulation tends not to be large, but due to the steepness of the resonance point, a good modulation efficiency can be obtained.

Lateral PN junctions are considered more or less a 'solved' issue; balance of efficiency and loss versus doping is well known and not much additional performance can be squeezed from it. However, there are ways of designing around the limitations of a uniform PN junction. Some approaches use vertical junctions, such as SISCAP (silicon-insulator-silicon capacitors) junctions, with the idea of increasing the junction depletion region that overlaps with the optical mode, albeit at the cost of higher fabrication complexity. Various shapes of

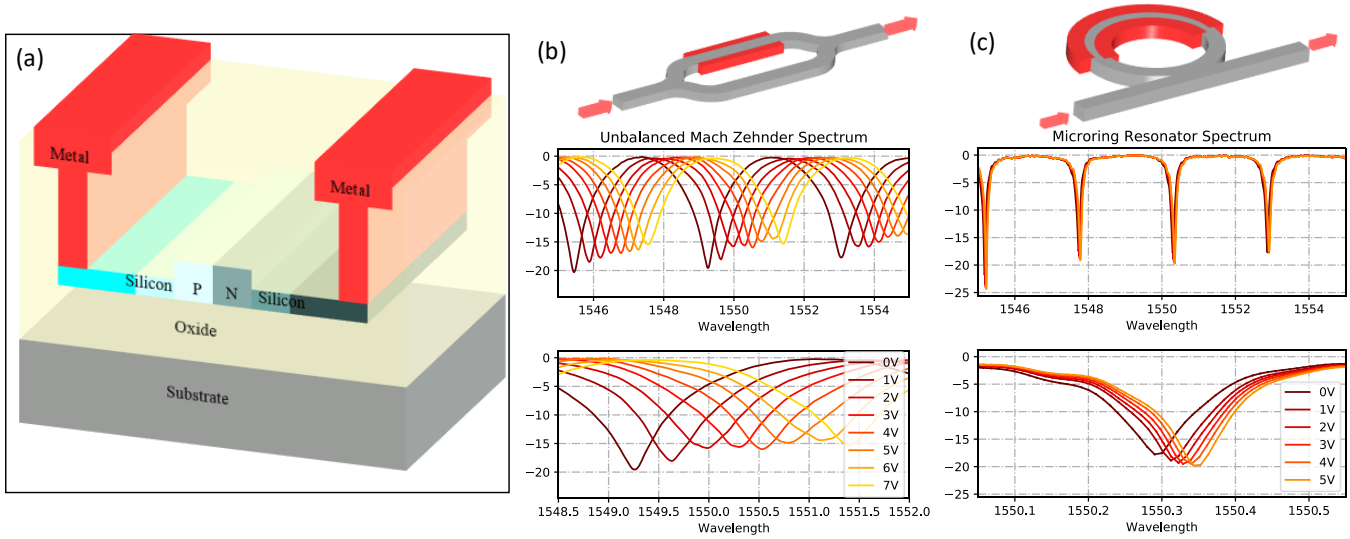

Fig. 9. (a) Cross section of a silicon waveguide integrated PN junction, utilizing the plasma dispersion effect in the PN junction to modulate the refractive index. (b) Mach-Zehnder configuration to form an intensity modulator from a phase modulator. Voltage vs Wavelength shown for an unbalanced arm Mach-Zehnder. A zoomed-in graph is provided. (c) Micro-ring resonator applies the same principle to the tuning of the resonance point of a cavity. Voltage vs resonance point tuning is shown, again with a zoomed-in graph.

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junctions (such as L-shaped [86] and U-shaped [87]) also increase the modulation efficiency by increasing junction area without much increase in complexity, just needing additional doping layers. Some styles (such as self-aligned doping [88]) are also chosen to improve misalignment tolerance. The cross-section for these methods of forming the PN junction are shown in Fig. 10. The junction can also be varied along the direction of propagation, by interleaving the PN junctions [89]. It is important to note that in modulator design, it is a matter of trade-offs: such schemes that increase the region of index change also correspondingly increase the capacitance. In travelling wave electrode designs, RF losses are strongly influenced by the junction capacitance. Therefore, it is not a simple upgrade to change from, for example, a simple PN junction to a U-shaped junction (Fig. 10(a) to (d)), and such choices need to depend upon whether bandwidth or efficiency is more important.

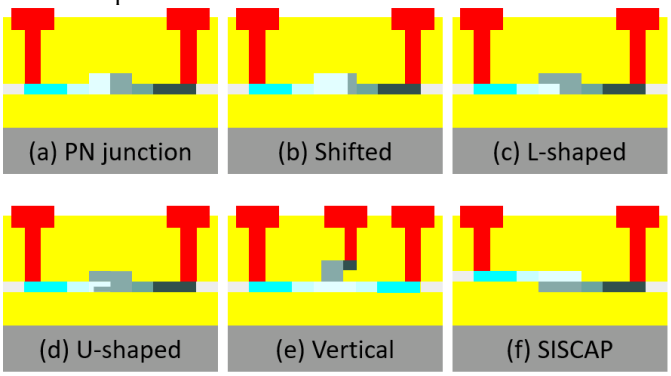

Fig. 10. Various designs of PN junction. Various methods that increase the modulation efficiency also increases the capacitance. (a) to (d) can be fabricated with modifying the doping, whereas (e) and (f) may require process change.

Si-Ge electro-absorption modulators are another type of modulator that instead utilize the Franz-Keldysh effect, which describes the change in absorption due to an applied electrical field. The physical reason is due to the change of the bandgap, which therefore moves the optical absorption edge. The waveguide integrated geometry of these FK devices negates the traditionally large voltages needed as the electrical field is enhanced due to the small distances, and as a result can be modulated at typically lower voltages than Mach-Zehnder devices. However, this does mean that it is generally only capable of electro-absorptive modulation in the C + L band. EAMs do cost additional fabrication complexity but have very good performances. As the name suggests, EAMs modulate absorption and not phase. As a result, phase modulation methods are not so straightforward to implement in EAMs. Nevertheless, there have been implementations of QAM in EAMs utilizing interferometric effects [90], [91].

Ultimately, the design of silicon photonic modulators is typically a trade-off between several parameters. A modulator can be generally described with the following figures of merits:

Bandwidth: refers to the frequency at which the electro-optical response (S21) decays to -3dB from the DC point (sometimes the 1 GHz point). In many designs, this bandwidth is related to the R and C characteristics of the modulator. There are other bandwidth limitations, for example photon lifetime in micro-ring modulators or metal conductivity and dielectric loss in travelling-wave modulators.

Modulation efficiency: typically specified in Vπ, the voltage required to achieve π phase shift, or Vπ×L, multiplied by the phase shifter length. For some devices (such as MRM, EAM), the concept of Vπ may not exactly exist, and instead the peak-to-peak voltage (Vpp) may be used.

Insertion loss: refers to the optical power loss after passing through the modulator. This can either be specified in dB or dB/mm. An important parameter to consider along with the optical power budget.

Footprint: can be an important consideration for photonic integrated circuits, especially as photonic circuits become more complex.

Fabrication complexity and process robustness: higher fabrication complexity may reduce yield and increase costs, and can sometimes be the defining characteristic that makes designers chose one device type over another. Process robustness is also a concern: performance devices need high yield to be commercially viable. This can be particularly important for SiGe devices, as the epitaxial growth of germanium on silicon is a fairly complex process.

Spectral Tolerance: spectral tolerance refers to the capability of the device to work across a large wavelength range without many drawbacks. While this is an issue for all modulators, it is particularly disadvantageous to micro-ring resonators (which are very sensitive to the wavelength and the cavity can heat up significantly during operation) and EAMs (which typically cannot operate in lower wavelengths, such as O-band). To compensate this effect, typically modulators employ feedback mechanisms (for example by monitoring the drop port of a micro-ring modulator) [92].

Fig. 11 summarizes these figure-of-merits, with references from literature that demonstrate the strengths and weaknesses of each device type. There are, of course, many ways to overcome weaknesses of any one device, so this should only serve as a general guide to understanding. In each device type, each parameter can be improved specifically, though usually at the cost of others. From Fig. 11, although on paper Mach-Zehnder modulators do not stand out, the careful balance of parameters means that it is widely commercially deployed.

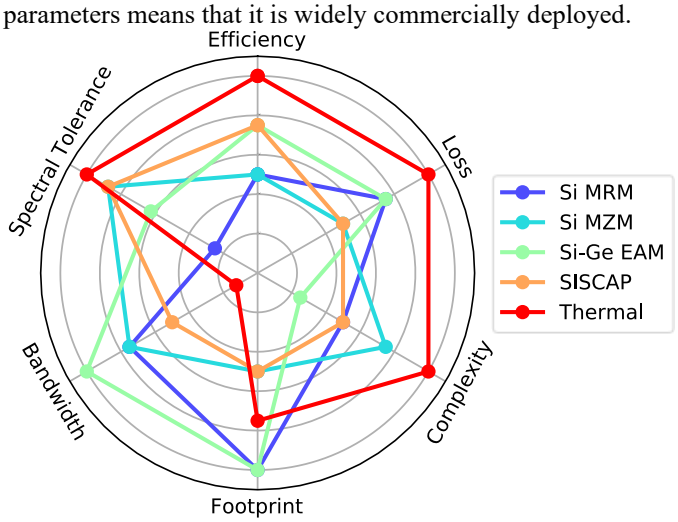

Fig. 11. Modulator dilemma of silicon-based modulators, balancing the figure of merits, and the relative performance of various modulators (higher is better). Other figures of merit include process complexity and footprint. These are just for reference, individual designs within each sub-group can obtain vastly different metrics. References: Si MRM [93], [94]; Si MZM [95], [96]; SiGe EAM [97], [98]; SISCAP [99], [100]; Thermal [101], [102].

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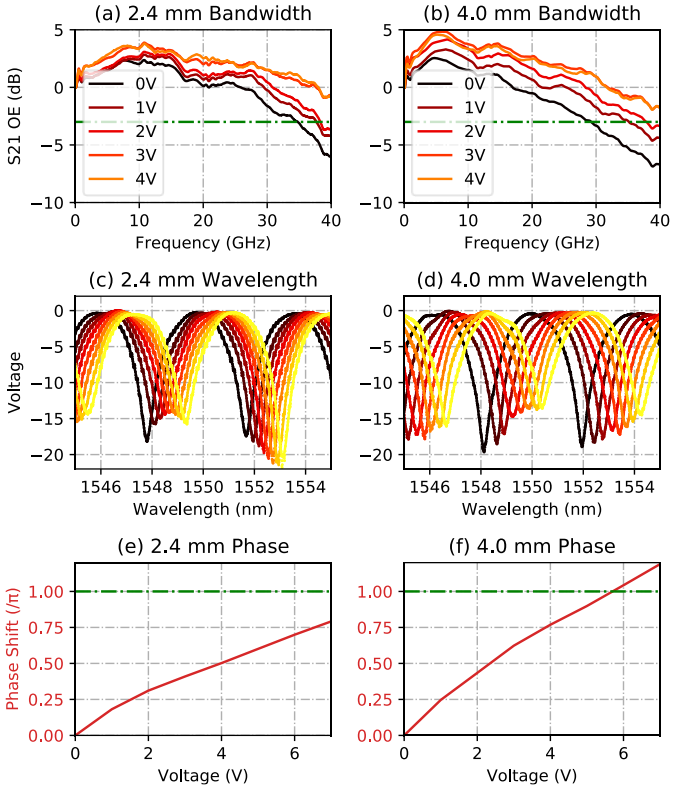

Fig. 12. Typical figures of Merit of AMF's PDK C-band modulator. The PDK modulator is characterized in 2 lengths, 2.4 mm (left column) and 4.0 mm (right column), from which customers may choose a custom length according to their application. (a, b) The S21 electro-optic bandwidth normalized to 100 MHz (the lowest measured frequency). (c, d) The voltage applied vs wavelength spectrum, showing the effect of applying a reverse bias voltage. Each line is in 1 V increments from 0V to 7V. (e, f) The cumulative phase shift against voltage. A value of 1 represents Vπ. For the 4.0 mm modulator, Vπ is 5.9V, whereas the 2.4 mm modulator achieved 0.8 Vπ at 7V

AMF (and previously IME) has devoted great efforts to develop high speed modulators [103], [104]. The current iteration of PDK modulator is based upon the series push-pull Mach-Zehnder structure, and is characterized at two lengths, 2.4 mm and 4.0 mm. The modulator FOM is shown in Fig. 12, which shows the bandwidth, transmission spectrum versus applied voltage, and the phase shift versus applied voltage. For the 4.0 mm modulator, Vπ is 5.9 V, whereas the 2.4 mm modulator achieved 0.8 Vπ at 7 V. The actual doping levels are around the 3.5E17 cm^{-1} range with corresponding sheet resistances of 4100 and 1640 Ω/□ for the P-doped and N-doped, respectively. The idea is that this provides circuit designers with flexibility to range between and even beyond these lengths with some extrapolation. This may be important for each designer to balance the metrics depending upon their own application.

As shown in Fig. 12(a), the bandwidth of a 4.0 mm modulator is 29 GHz at 0 V, which quickly ramps to over 40 GHz at -3V. The 2.4 mm modulator hovers around the -3 dB line from 38 – 40 GHz at 0 V, and quickly goes to above 40 GHz for any applied reverse bias. 40 GHz represent the limit of the measurement equipment, and the setup is calibrated up to the end of the microwave cable (excluding the 67-GHz probe tip). The probe tip has a slight electrical attenuation (<0.5 dB) at 40 GHz.

These represent the state-of-the-art bandwidth achievable while maintaining reasonable Vπ and are fully compatible with the MPW platform offered. The high speeds are obtained by iterative optimization of the modulator using the standard MPW platform. The PDK modulator is designed at 50-Ω impedance, and while driving at 50-ohm the reflection S11 tends to be under -13 dB across the range. The standard modulators utilize an on-chip termination of around 40 Ω. This can of course be tuned to improve bandwidth at the cost of increased power consumption. The modulator is also characterized with an eye diagram (Fig. 13), which simulated the actual configuration of a transceiver. The modulators are driven by a bit-pattern generator (BPG), then amplified to 3Vpp, and then the signal is received by a digital communication analyzer (DCA), which includes some signal processing.

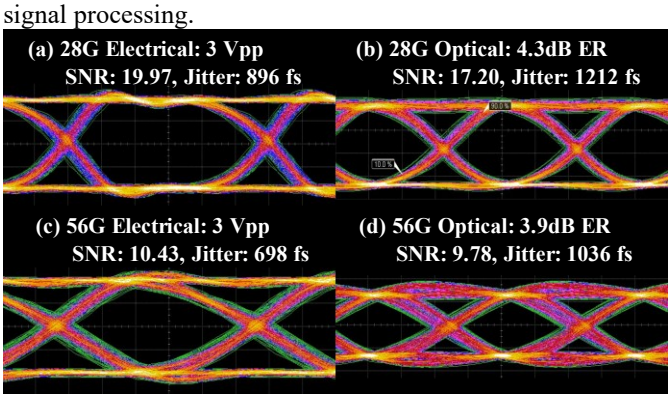

Fig. 13. Eye diagram testing for the C-band PDK modulator with 2.4mm in length. (a) Electrical Eye Diagram of the driving signal at 28 Gb/s and the corresponding (b) optical eye diagram. Likewise, (c) is the electrical 56 Gb/s NRZ OOK, and the resultant optical eye is shown in (d). The extinction ratio ranges from 3.9 to 4.3 dB ER with 3Vpp driving signal, depending upon the driving speed. The signal is generated by a bit pattern generator and amplified by a driver, and subsequently attenuated to the 3V level using passive RF attenuators. The corresponding electrical signals to drive the optical eye are also shown for comparison.

For example, driving at quadrature (to maximize the linearity and response), it may only be necessary to drive at half of less of Vπ to obtain the required extinction ratio. The choice of length then depends on the required extinction ratio and/or voltage. The 2.4 mm modulator obtains an extinction ratio of 3.947 dB at 56 Gb/s. If additional extinction ratio is required, it is simply a matter of either increasing the voltage or changing the operating point closer to the null point. The rise and fall times shown are not deconvoluted and are 10%-90% and can be affected by some filtering in the receiver end (to remove noise).

We summarize the state-of-the-art demonstrations of the high-speed silicon modulators in Table VII. To standardize the results, if multiple bandwidths are taken at several bias points, the bias point closest to -3V is shown. Likewise, the phase shifter loss is standardized to the unbiased case. Some of the data is extracted from the graphs from some of the reference. The modulation efficiency is taken at DC. As a result, in an ideal RC network, a modulator with 34.9 GHz bandwidth will have a 10%-90% rise time equal to 10 ps, half the time per symbol of a 50 Gbaud modulation. As the modulation speed increases, this bandwidth-imposed limitation will ultimately close the eye as the baud rate increases. This eye closure can eventually dictate the achievable baud rate for the modulator.

TABLE VII
C-BAND SILICON PHOTONICS MODULATOR FROM LITERATURE

BW(GHz) (Bias)	Vπ (V)	VπL (V·cm)	Length (mm)	PS Loss (dB/mm)	Reference
>40 (-3V)	5.9	2.36	4	1.15	[48]
>40 (-3V)	8.8	2.11	2.4	1.15	[48]
42.3 (-2V)	7	1.40	2	2.2	[105]
35 (-4V)	4.5	1.35	3	2	[106]
30 (-5V)	7.5	2.25	3	0.9	[107]
35 (-5V)	7.3	3.29	4.5	6.8*	[108]
30.4 (-3V)	3	1.20	4	2.95	[109]
29.9 (-3V)	4	1.60	4	1.75	[109]
27 (-1V)	7.8	2.73	3.5	1.03	[110]
38 (-2V)	8	3.20	4	0.95	[96]
20 (-2V)	4.5	2.25	5	1.5	[111]
24 (-5V)	3	2.20	5.5	0.94	[112]
20 (-2V)	3.1	1.86	6	1.2	[113]

* 6.8 dB total IL

There are many precedents in literature showing that a 30+ GHz BW modulator is required to support 56 Gbaud, but this is by no means the limit. Some performance penalty is acceptable from an OSNR/BER point-of-view, and transmission-side techniques such as pulse-shaping/pre-emphasis and receiver-side equalization and filtering can allow much higher baud rates while maintaining the target OSNR/BER. For example, [109] demonstrated over 100 Gbaud modulation with ~30 GHz modulators, with one key point being that the 6 dB EO Bandwidth were over 50 GHz and does not steeply roll off after 50 GHz.

D.High Performance Germanium Photodetectors

A photodiode is a semiconductor device that converts an optical signal to an electrical signal such as a voltage or current pulse. This conversion is achieved by the creation of free electron-hole pairs through absorption of photons.

Normally, PIN structure includes a sandwiched intrinsic region between the p-type and n-type region is adopted for photodetector. When it is illuminated with photon energy greater than or equal to the bandgap of the semiconductor material, the photons are absorbed, and electron-hole pairs are generated. By applying an external reverse bias, a depleted region is formed. This results in the entire voltage drop on the depleted region and thus a high electric field, facilitating the collection of the photo-generated electron-hole pairs. Due to this high electric field, the photo-generated carriers travel at their saturation velocity.

This PIN structure is particularly important in designing photodetectors for silicon photonics as it can easily meet the high-speed demand in the range of tens of GHz. To integrate such PIN photodetectors into the silicon photonics platform, the hetero-epitaxial germanium (Ge) is generally considered to be the ideal intrinsic region material as it has strong absorption in the near-infrared regime and the advantage of a fully CMOS compatible, high throughput, and low-cost integration.

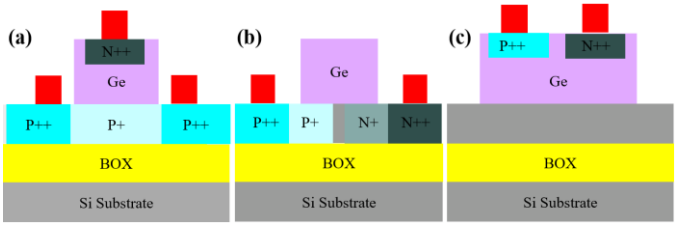

Fig. 14. (a) Vertical Ge PIN photodetector. (b) Lateral Ge PIN photodetector. (c) Variant of lateral PIN photodetector.

In silicon photonics, the vertical Ge photodetector [114]–[116] is the most straightforward design as shown in Fig. 14(a), which is widely used and shows promising device performance. Another widely studied Ge PIN photodetector design [117], [118] is based on a lateral PIN configuration with both anode and cathode metal contacts on Si, as shown in Fig. 14(b). Although metal contacts can be made on Ge to form anther type of lateral PIN configuration [116], [119], as shown in Fig. 14(c), it will introduce a large responsivity loss and increases the process flow complexity as well.

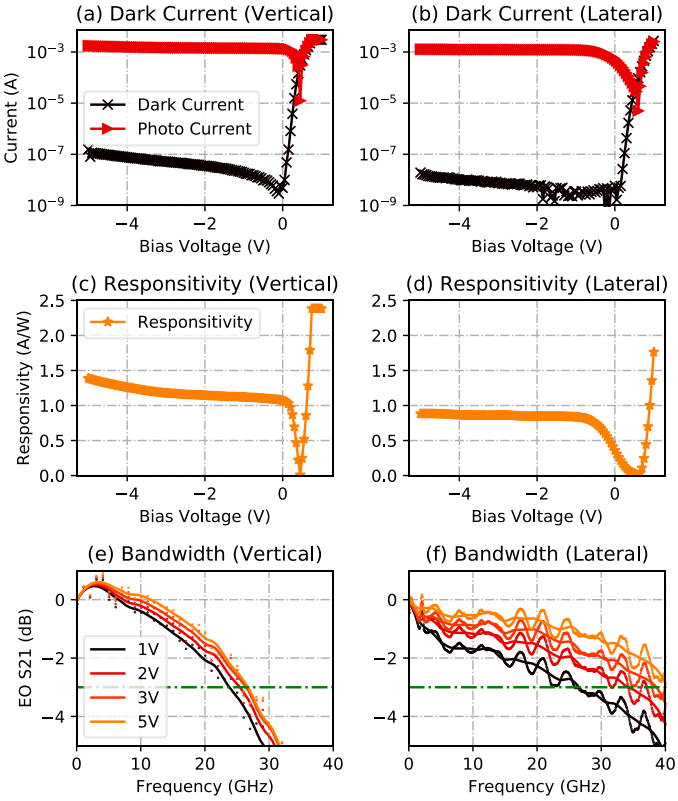

Fig. 15. Testing results of AMF vertical and lateral Ge photodetectors: (a)-(b) dark current and photocurrent, (c)-(d) responsivity, (e)-(f) bandwidth.

In general, a Ge Photodetector can be characterized with the following FOMs: 1) dark current, 2) responsivity, 3) 3-dB bandwidth and 4) operation voltage. Responsivity is defined as the ratio of the generated photocurrent and the incident optical power in A/W. The 3-dB bandwidth (denoted $S21_{OE}$) represents the capability to respond to a quickly modulated optical signal and is defined as the frequency at which the responsivity drops to half. The dark current is the reverse-biased current of a photodetector without illumination. Ideally, a Ge PIN photodetector can respond to a fast-modulated optical signal

with a low operation voltage. Typically, the trade-off between the responsivity and the bandwidth of a Ge PIN photodetector can be partly addressed by using the waveguide structure to decouple the light absorption from the carrier transport. The bandwidth of a Ge PIN photodetector depends on the photo-carrier transit time and the RC time constant. As the capacitance is inversely proportional to while the transit time is proportional to the width of the intrinsic region, photo-carrier transit time and junction capacitance are inter-dependent, and thus the design of a Ge PIN photodiode involves a performance trade-off. In general, for the vertical Ge PIN photodetectors with the Ge thickness of 500 nm which is adopted by most of the foundries, the intrinsic Ge region is narrow and thus the capacitance dominates over the transit time. Therefore, the bandwidth of a vertical Ge PIN photodetector is RC constant limited. Whilst, for lateral Ge PIN photodetector, the electrical field in Ge is relatively weak, resulting in a low drift velocity to sweep out the photo carrier, thus the bandwidth is generally the transit time limited.

Fig. 15 shows the typical performance of respectively the vertical (left column) and lateral (right column) Ge photodetectors. For the vertical Ge photodetector, the responsivity has already reached 1.12 A/W at -1 V while the bandwidth can reach 25 GHz at -1 V and ramps up to 28 GHz at -3 V. As to the lateral Ge photodetector, the responsivity is about 0.83 A/W at -1 V while the bandwidth can easily reach 31 GHz at -1V, which then quickly ramps up to over 40 GHz at -5 V. This indicates a notable increase in the response speed with a higher reverse bias. The dark current is well controlled for both vertical and lateral Ge photodetectors. Particularly, the dark current is only 7 nA at -3 V for lateral Ge photodetector.

TABLE VIII
GE PIN PHOTODETECTORS AND THE TYPICAL PERFORMANCES (AT WAVELENGTH OF 1550NM WITH -2V BIASED VOLTAGE)

Type	Dark Current	Res. (A/W)	BW (GHz)	Ref.
Lateral	<10 nA	0.83	37	[48]
Lateral	<120 nA	<1.14	~7	[120]
Lateral	10 nA	0.95	9	[121]
Lateral	~500 nA	1.06	>70	[122]
Lateral	8 nA	>1.0	27	[117]
Lateral	~200 nA	1.16	32.8	[123]
Lateral	~50 nA	0.5	~40	[124]
Lateral	3.6 nA	0.74 @ -1V	>67	[118]
Vertical	50 nA	>1	25	[48]
Vertical	120 nA	0.88	28	[116]
Vertical	10 nA	0.95	36	[125]
Vertical	2 nA	0.65 @ -1V	40 @ -1V	[126]
Vertical	3.5 μA	1.09	42.5	[127]
Vertical	<15 nA	1	>45	[128]

Table VIII shows the performance comparison of various demonstrations for both vertical and lateral Ge photodetectors at 1550 nm. Most of the dark current, responsivity, and bandwidth are taken at the same bias point of -2 V otherwise specified. Considering all FOMs, AMF PDK photodetectors show a good balanced performance.

IV. OUTLOOK AND CONCLUSIONS

Silicon photonic, initially primarily developed by universities and research institutes, is poised to undergo rapid expansion, leveraging upon the decades of work in silicon electronics. Silicon photonics already has commercial products, albeit at a low volume stage. The ecosystem of design houses, production lines and packaging houses allow both traditional large corporations as well as start-ups to quickly integrate silicon photonics into their platform.

Currently, silicon photonics is expected to revolutionize the transceiver datacom and telecom market. The main draw being that silicon photonics will be significantly cheaper than the other options, particularly InP-based transceivers (whose wafers are only commercially mature on the 2 inches to 4 inches level, and are much more expensive comparing to silicon wafers). Silicon photonics also has significantly lower upfront costs, which many companies being able to tap into the silicon photonics fabrication ecosystem that has already been described here. However, silicon photonics does not have the full function required for a full photonics integrated circuit, the key component being the lack of a laser. As a result, a typical silicon transceiver experiences additional coupling loss from the laser to the silicon photonics chip. This coupling loss is not prohibitive, as many packaging works have managed to reduce this loss to 1 dB or less [129].

TABLE IX
DATACOM VS TELECOM

	Datacom	Telecom
Distances	• Short reach • Private companies	• Metro, regional, long haul • Telecom, ISPs
Operating Environment	• Highly controlled datacenter	• Could be anywhere: subsea
Costs	• Short device lifespan (3-5 years) • Frequency upgrading • Cost Sensitive	• Long device lifespan (10+ years) • Infrequent upgrading • Cost in-sensitive
Volume	• High volume, low margin • High Y-O-Y growth	• Low volume, high margin • Low Y-O-Y growth
Implications to Silicon Photonics	• Extremely cost sensitive • Target $1/Gbps • Low voltage operation to save power costs	• Less sensitive to costs • High robustness needed • Performance guarantees

The open access nature of silicon photonics fabs and reduced overall costs, makes silicon photonics a highly attractive proposition at the datacom-level, where price is king. The jury is still out for the high-performance coherent transceiver market (especially at the long-haul level), where

performance and robustness start to take priority over cost, and each system manufacturer may weigh differently the cost-benefit analysis of InP, SiP and LN. Datacom is expected to have a lot more demand than telecom in terms of wafers, and this high-volume pressure may eventually push the telecom markets towards silicon photonics as well. Table IX briefly summarizes these differences.

Moreover, as an enabling technology, silicon photonics is not limited to optical communication. Applications such as optical sensing [130], [131], LIDAR [132], [133] , are being commercialized using silicon photonics. Sensing and LIDAR applications have a large market in self-driving cars, as silicon photonics-based LIDAR represents an order-of-magnitude cost decrease compared to electro-mechanical scanning systems. Solid state silicon photonics LIDAR can be cheaper, smaller, more robust, and can allow some of the processing to be done in the optical domain. Advanced applications in quantum photonics and photonic computation are also being actively explored, with SiP-based QKD networks [134], [135], artificial neural network and optical computing [136], [137] already being demonstrated. More and more, the encryption of data is taking precedence, and exploiting quantum phenomenon to encrypt information is a natural evolutionary step. Silicon photonics computation is another field gaining traction in literature, especially as a candidate for neuromorphic computing. Many industry observers believe that silicon photonics has reached its inflection point, and, at least in the world of photonics, the future is still silicon.

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