25 Gbit/s silicon microring modulator based on misalignment-tolerant interleaved PN junctions

Xi Xiao,* Hao Xu, Xianyao Li, Yingtao Hu, Kang Xiong, Zhiyong Li, Tao Chu, Yude Yu, and Jinzhong Yu

Optoelectronic System Laboratory, Institute of Semiconductors, Chinese Academy of Sciences, P.O. Box 912, Beijing 100083, China
*xixiao@semi.ac.cn

Abstract: A high-speed depletion-mode silicon-based microring modulator with interleaved PN junctions optimized for high modulation efficiency and large alignment tolerance is demonstrated. It is fabricated using standard 0.18 μm complementary metal–oxide–semiconductor processes and provides low $V_\pi L_\pi s$ of 0.68 V·cm to 1.64 V·cm with a moderate doping concentration of 2×10^{17} cm^{-3}. The measured modulation efficiency decreases by only 12.4% under ± 150 nm alignment errors. 25 Gbit/s non-return-zero modulation with a 4.5 dB extinction ratio is experimentally realized at a peak-to-peak driving voltage of 2 V, demonstrating the excellent performance of the novel doping profile.

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OCIS codes: (130.0130) Integrated optics; (130.0250) Optoelectronics; (130.4110) Modulators.

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1. Introduction

Inspired by the excellent optical properties of the silicon-on-insulator (SOI) platform and the high quality fabrications provided by complementary metal–oxide–semiconductor (CMOS) technologies, silicon photonics has made significant progress in the past few years [1, 2]. Large-scale monolithic optoelectronic integration on silicon wafers has been widely recognized as an essential step for the realization of on-chip optical interconnects which is

expected to enable low-power and high performance computing systems [3–6]. Terabit-per-second on- and off-chip optical communication require compact silicon-based modulators with high modulation speed and low power consumption to transfer high-speed electrical signals into optical intensity signals [7–9]. Among the various kinds of silicon-based modulators, the microring modulator based on carrier depletion in reverse PN junction is considered as a promising candidate for on-chip application silicon photonics which is recently demonstrated with > 10 Gbit/s modulation speed [10–13], micron-size footprint [14–16], wavelength tuning capacity [17, 18], and femtojoule-per-bit-scale power consumption [19, 20].

However, a tradeoff between modulation speed and extinction ratio exists because of the speed limitation induced by the large optical lifetime of the high quality factor (Q factor) microring resonators. Low Q factor microrings can be employed to produce a high modulation bandwidth [20]. However, without special designs on the junction doping profiles, the modulation efficiency of the traditional vertical or horizontal PN junction cannot produce sufficient resonance shifts and hence result in small extinction ratios [20, 21]. Therefore, the key solution to break the speed-extinction limitation of the microring modulator is to increase the electro-optical (EO) efficiency of the reverse PN junctions, that is, to reduce the voltage-length product $V_\pi L_\pi$. On the other hand, the high requirement on the accurate overlay of doping masks is another drawback of typical depletion-mode modulators because the EO efficiency directly depends on the location of the PN junction within the waveguide [22]. The poor overlap of the submicron waveguide mode and the ~100 nm space charge region results in a rather weak effective index change if the PN junction is not precisely aligned [23]. So during the fabrications of depletion-mode modulators, expensive 0.13 μm CMOS processes are normally used to ensure small junction alignment errors and hence realize desirable performance [24, 25]. Recently, a kind of self-aligned doping process has been developed to solve the junction alignment problem and demonstrated the modulations up to 40 Gbit/s [26, 27]. But it more or less put on the requirement on the implantation equipments when embedding PN junctions to the microrings without fixed waveguide sidewall rotation. In order to realize high speed microring modulators in a standard CMOS foundry with minimal cost, we need to explore a kind of PN junction providing both low $V_\pi L_\pi$ and large tolerance to the junction misalignment.

Interleaved PN junction could provide high EO efficiency due to enhanced carrier-light overlap [28]. Recent research has realized 10 Gbit/s modulation based on the similar structure [29], while the performance improvements on the misalignment tolerance and the modulation efficiency have not been achieved yet. In this paper, a high speed silicon microring modulator based on interleaved PN junctions is presented without precise junction alignment. With the optimizations on our previous design and device [30], the current modulator demonstrates the low $V_\pi L_\pi$, the large misalignment tolerance and the high modulation speed, simultaneously. Experiments confirm that the effective index changes are tolerant with ± 150 nm alignment errors and hence fully compatible with standard 0.18 μm CMOS fabrications. An effective $V_\pi L_\pi$ of 1.24 V·cm and a low doping loss of 12.6 dB/cm are demonstrated with moderate doping density. Consequently, high-speed modulations of 14, 20, and 25 Gbit/s are respectively demonstrated with low driving power.

2. Device description and fabrications

In order to achieve high modulation efficiency, the overlap of the ~100 nm wide free charge region and the submicron optical mode should be improved. We designed the interleaved PN junctions with which interface vertical to the optical propagation direction, as shown in Fig. 1. When the modulator is reversely biased, the light propagating inside the waveguide would vertically pass through each junction interface, leading to a thorough interaction with carriers. Based on the former simulations, a doping density of 1×10^{18} cm^{-3} brings to a rather high efficiency with a theoretical $V_\pi L_\pi$ of only 0.24 V·cm. However, in current work, a lower

doping level of 2×10^{17} cm^{-3} was chosen for an acceptable doping-induced absorption loss. The lengths of the P and N regions are optimized as both 300 nm, indicating a 600 nm long doping period. The interleaved width of the cascade PN junctions is carefully designed to be 700 nm to ensure both low capacitance and large misalignment tolerance. The proposed doping profile is predicted to have a 35 GHz bandwidth and ~9 dB/cm doping loss.
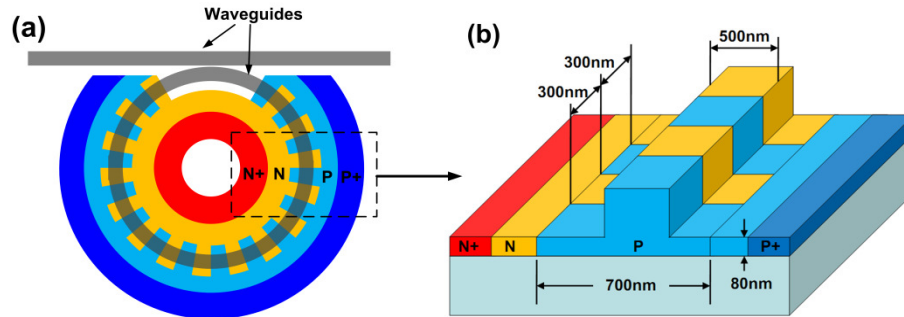

Fig. 1. (a) Schematic layout of microring modulator embedded with periodic interleaved PN junctions. The gray regions indicate silicon waveguides. The light blue and yellow regions in the waveguide represent P- and N-doped silicons, respectively. (b) Schematic 3-D view and dimensions of the waveguide with the interleaved PN junctions. The doping period is 600 nm with a P and N duty cycle of 1:1. The waveguide is 500 nm wide and has an 80-nm-thick slab for electrical contact. The interleaved region is 200 nm wider than the waveguide, ensuring large misalignment tolerance.

The 30 μm-radii microring modulator embedded with the optimized interleaved PN junctions was fabricated using a commercial 0.18 μm CMOS process from the Semiconductor Manufacturing International Corporation (SMIC) in China [31]. We firstly defined and etched the waveguides on the SOI wafer from SOITEC with a 340-nm-thick top silicon layer and a 2-μm-thick buried oxide layer. All waveguide and doping dimensions are designed to be over 180 nm for the CMOS compatibility. The 500 nm wide microring waveguide is single coupled to a straight waveguide, see Fig. 2(a). The fiber-to-waveguide coupling is implemented by grating couplers. The slab thickness was optimized to 80 nm for a tradeoff between the diode resistance and optical confinement. Then, the interleaved PN junctions were realized using deep-UV lithography and boron and phosphorus implantations. The waveguide was firstly P-type doped to a background concentration of 2×10^{17} cm^{-3} by multiple implantation processes to approach to a uniform doping distribution. The multi-step N-type implantations were followed with a higher density of 4×10^{17} cm^{-3} to form the abrupt PN junctions. Highly doped P + and N + regions were both defined 500 nm away from each side wall of the ring waveguide, respectively, followed by 10 second rapid thermal anneal at 1000°C. Finally, aluminum was deposited, patterned, and etched down to form the ground–signal–ground electrodes. The optical microscope view of the fabricated device is shown in Fig. 2(b).
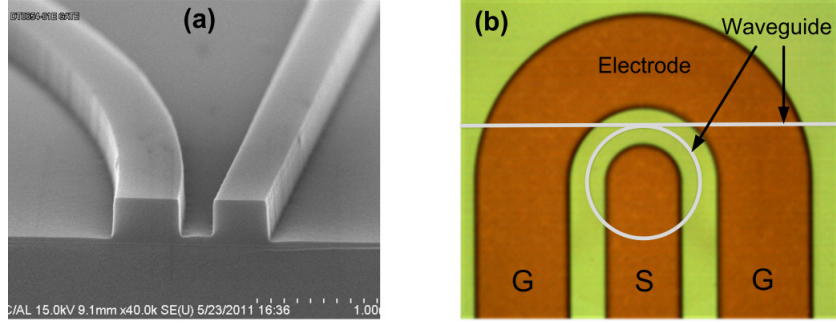
Fig. 2. (a) SEM image showing the coupling region of the microring and bus waveguides. (b) Optical microscope view of fabricated 30 μm radius microring modulator with aluminum ground–signal–ground pads.

3. Results and discussions

3.1 DC performance

The transmission spectra of the microring were obtained when the biased voltages vary from forward 0.5 V to reverse 5 V, see Fig. 3(a). Considering that the depletion region width of a PN junction is proportional to the square root of the applied voltage, the changes in the depletion region width are more efficient when the applied voltage gets close to the built-in voltage of the PN junction. Hence, a smaller bias voltage was observed to result in a higher resonance shift efficiency, which is approximately 40 pm/V at 0 V bias and decreases to 17 pm/V at −5 V bias. The $V_\pi L_\pi$ of the microring modulator can be calculated by the following:

$$V_\pi L_\pi = V \cdot \frac{FSR \times \pi R}{\Delta \lambda} \tag{1}$$

where V is the applied voltage, FSR is 3.2 nm, indicating the wavelength difference between two adjacent resonances, R is the radius of the microring, and $\Delta\lambda$ is the resonance wavelength shift. Figure 2(b) shows the $V_\pi L_\pi$ ranging from 0.68 V·cm to 1.64 V·cm as a function of the applied voltages. Based on the measured spectral curves, a driving voltage of 0 V to −2 V is enough to drive the modulator, which enables a 20 dB excess in DC extinction ratio. Therefore, the effective $V_\pi L_\pi$ can be calculated as 1.24 V·cm when this driving voltage is used.
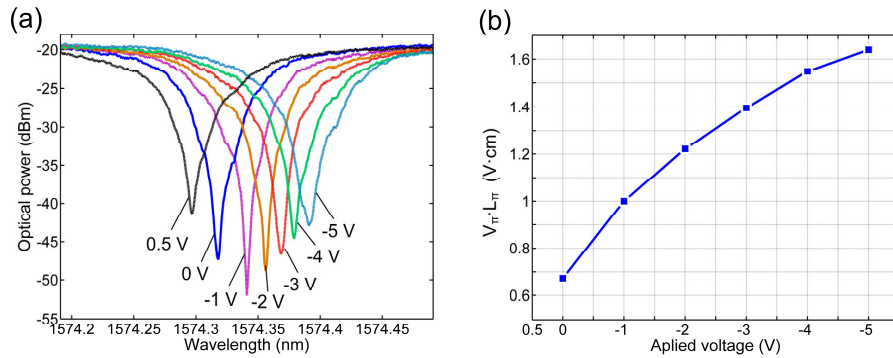

Fig. 3. DC performance of the reverse-biased ring modulator. (a) Transmission spectra of the ring resonator at −5 V to 0.5 V bias voltages. (b) $V_\pi L_\pi$ with different bias voltages calculated from the measured resonance shifts. The maximal $V_\pi L_\pi$ of 1.64 V·cm was obtained at a −5 V bias voltage. However, the effective $V_\pi L_\pi$ for a driving voltage below −2 V is 1.24 V·cm.

We analyzed the doping induced optical loss by curve fitting the resonances of the microring modulator and a passive microring, respectively, as shown in Fig. 4. Compared with the traditional cut-back method or Fabry-Pérot method, this method is independent to the fiber-to-waveguide coupling or cleaved waveguide facets and hence induces less experimental error [32]. The passive microring with the same waveguide dimensions as the microring modulator was fabricated together with the modulator. In order to obtain accurate loss abstraction, the ring-waveguide coupling strength of the passive ring was weakened for over 10 dB resonant extinction. For the passive waveguide without doping, the intrinsic Q factor is calculated as 1.31×10^5 which shows a 4.1 dB/cm waveguide loss. While for the active ring waveguide after doping and activation, the intrinsic Q factor decrease to 2.94×10^4 corresponding to a total optical loss of 16.7 dB/cm. Therefore, a 12.6 dB/cm doping induced loss can be calculated, which is smaller than the loss of the modulators with comparable $V_\pi L_\pi$ values [33, 34]. Compared with the reported devices at the similar doping level [35], this modulator provides much higher modulation efficiency and lower absorption loss. These results indicate that the same volume of carriers contribute to a larger refractive index change due to the enhanced carrier-light overlap by using the interleaved cascade junctions. As the theoretical predicted doping loss is 9 dB/cm, we attribute the additional loss to the diffusion of N-type region during anneal and the fabrication imperfections.
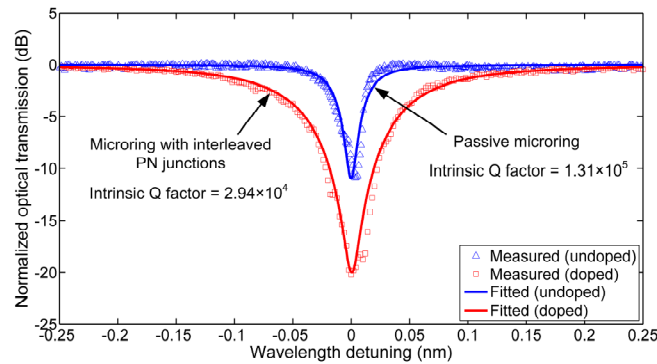

Fig. 4. Spectral responses of the non-biased microring modulator (red) and a passive microring resonator (blue) with identical waveguide dimensions as the ring modulator, respectively. The discrete dots represent the measured results, while the solid lines show the fitted resonances.

To demonstrate the large misalignment tolerance of the device, we compared the effective index change against the horizontal alignment error of the interleaved and normal vertical PN junctions. The measured results under an applied voltage of −5 V are presented in Fig. 5. For the vertical PN junction, the maximum effective index change significantly depends on the position of the PN junction in the waveguide. The modulation efficiency decreases by 65.5% when the junction is dislocated for ± 150 nm. However, under the same misalignment and applied voltage, the maximum index change of the interleaved PN junction is 2.2×10^{-4} and has only 12.4% degradation which shows an over fivefold improvement on the misalignment tolerance. In particular, the efficiency is almost independent with an alignment error of less than 60 nm, making the proposed novel PN junction fully compatible with standard 0.18 μm CMOS fabrications.
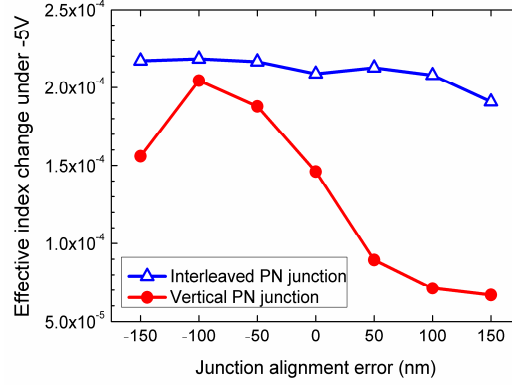
Fig. 5. Measured effective index change against junction alignment error of interleaved (blue) and vertical (red) PN junctions under −5 V bias, respectively.

3.2 Dynamic performance

The modulator's frequency response can be characterized by measuring its S11 parameter [36]. The S11 magnitude and phase response was measured from DC to 25 GHz by a signal integrity network analyzer (SPARQ, Lecroy). Figure 6(b) shows the measured S11 data and curve fitting results from the equivalent circuit model shown in Fig. 6(a). C_p represents the capacitance between the electrodes through the top dielectrics and the air, and C_j and C_{ox} are the capacitances in the reverse-biased diode junction and through the buried oxide layer, respectively. R_s and R_{si} are the diode series resistance and the resistance of the substrate silicon layer, respectively. Using the extracted parameter presented in Fig. 6(a), the junction capacitance is calculated to be 0.34 fF/μm which benefits from the low doping concentration.

The electrical bandwidth of the device under test (DUT) was calculated when it was loaded with a 50 Ω source. Assume that V_g is the sinusoidal output voltage and Z_g and Z_0 are the source resistance and the characteristic impedance of the cables and probe, respectively, which both equal to 50 Ω in the current paper. Γ_L is the load reflection coefficient between the probe and DUT. Therefore, the magnitude of the voltage across the reverse-biased PN junction V_j can be given by

$$\left|V_j(\omega)\right| = \left|\frac{V_g}{2} \cdot (1 + \Gamma_L) \cdot \frac{1/(j\omega C_j)}{1/(j\omega C_j) + R_s}\right| \tag{2}$$

where

$$\Gamma_L = \frac{Z_{DUT} - Z_0}{Z_{DUT} + Z_0} \tag{3}$$

and

$$Z_{DUT} = \frac{1}{j\omega c_p} \| (\frac{1}{j\omega c_j} + R_S) \| (\frac{1}{j\omega c_{ox}} + R_{Si}). \tag{4}$$

During the small-signal test, the resonance wavelength shift increases almost linearly to the applied voltage. Therefore, the output optical power is approximately proportional to V_j, and the electrical bandwidth corresponds to the −3 dB roll-off frequency of the V_j magnitude response, which was obtained as 41 GHz from Eq. (2).
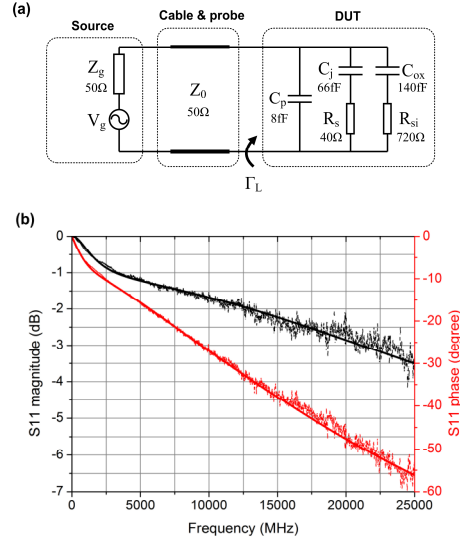
Fig. 6. (a) Equivalent circuit model and fitting data for the S11 parameter measurement at zero bias. (b) Measured S11 magnitude (black) and phase (red) responses with corresponding fitting curves simulated from the equivalent circuit model.

However, for a resonator-based modulator, the modulation bandwidth is also limited by the optical cavity lifetime. The Q factor of our microring is 1.45×10^4 at −1 V reverse bias, indicating an optical bandwidth of 13.6 GHz. The small-signal EO response of the modulator was measured within the frequency range of 200 MHz to 20 GHz, and a bias voltage of −1 V and the wavelength at half maximum of the resonance were chosen. The optical signal output from the microring was amplified, filtered, and converted to an electrical signal using a 50 GHz photodetector. As shown in Fig. 7, the −3 dB bandwidth (f_{-3dB}) of the proposed modulator is 11.8 GHz. The EO response was simulated by combining both the impacts of the optical lifetime and the intrinsic electrical bandwidth. The theoretical bandwidth of 12 GHz agrees well with the measurement. The 10%-to-90% rise time could therefore be predicted as $0.35/f_{-3dB} \approx 30$ ps [37], which can theoretically support a modulation bit rate up to 25 Gb/s.
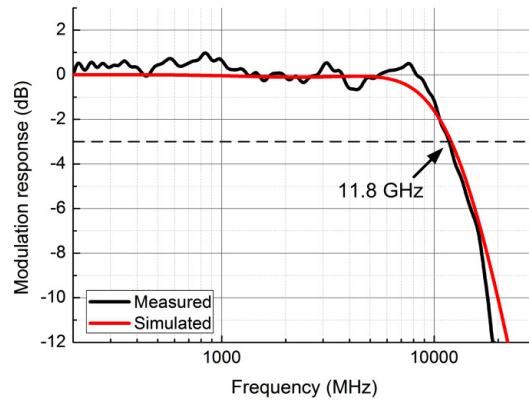

Fig. 7. Measured (black) and simulated (red) EO responses of the modulator. The EO response was measured in the frequency range of 0.2 GHz to 20 GHz with a −5 dBm small-signal drive and −1 V DC bias. The measured EO bandwidth is represented by black curve with −3 dB bandwidth of 11.8 GHz. The red curve denotes the simulated response at ~12 GHz, which agrees well with the measurements.

Optical eye diagrams were measured at high bit rates to demonstrate the high-speed performance of the device. A continuous-wave light was modulated by applying non-return-zero pseudorandom binary sequence (PRBS) $2^{15}-1$ signals with a V_{pp} of 2 V and DC bias of −1 V. The device insertion loss is around 10 dB including 5.4 dB coupling loss for two grating couplers and ~4 dB modulation penalty. The output light from the modulator was amplified using an Erbium-doped fiber amplifier and transmitted through a band-pass filter. Finally, the optical signal was measured by a 65 GHz optical head of a Tektronix digital scope DSA8200, see Fig. 8. The eye diagram at 14 Gbit/s obtained with ~6 dB extinction ratio is shown in Fig. 8(a). For the 20 Gbit/s eye diagram in Fig. 8(b), the difference in the modulation extinction is negligible, indicating the capability of a higher modulation speed. Finally, an eye diagram with 25 Gbit/s modulation speed was achieved under the same driving condition, as shown in Fig. 8(c). The extinction ratio decreased to 4.5 dB because of the optical-lifetime-induced bandwidth limitation.
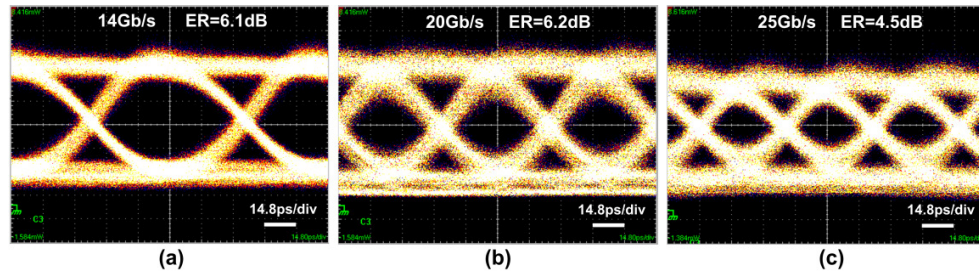

Fig. 8. Measured eye diagrams under bit rates of (a) 14, (b) 20, and (c) 25 Gbit/s, respectively, with driving voltage amplitude of 2 V.

4. Conclusions

We demonstrate a high speed silicon microring modulator based on the interleaved PN junctions providing both high modulation efficiency and large tolerance to the misalignment. The doping profile and optical structure were specially designed to be compatible with the standard 0.18 μm CMOS process. The fabricated device has a large tolerance with ± 150 nm junction alignment errors and shows only 12.4% degradation on the modulation efficiency. Due to the enhanced carrier-light overlap induced by the cascade interleaved PN junctions, an effective $V_{\pi}L_{\pi}$ of 1.24 V·cm and a doping-induced loss of 12.6 dB/cm were both achieved with a light doping concentration of 2×10^{17} cm^{-3}. The −3 dB cutoff bandwidth was measured as 11.8 GHz which agrees well with the simulations. Finally, when driven using PRBS data with a V_{pp} of 2 V, 20 and 25 Gbit/s, high-speed modulations with the extinction ratio of 6.2 and 4.5 dB were achieved, respectively. High speed modulation in excess of 40 Gbit/s can be expected by employing the interleaved PN junction in a Mach–Zehnder or cascade ring modulator.