A Two-Segment Optical DAC 40 Gb/s PAM4 Silicon Microring Resonator Modulator Transmitter in 65nm CMOS

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Abstract: A two-segment silicon photonic microring modulator implements an optical DAC for PAM4 modulation. Independent level and edge-rate control is achieved using segmented MSB/LSB pulsed-cascode drivers. The 65nm CMOS transmitter achieves 40Gb/s operation at 4.38mW/Gb/s while driving each microring modulator segment with 4.4V_{ppd} swing.

1. Introduction

Growing bandwidth demands in data-centers and high performance computing motivates the investigation of advanced optical interconnect techniques for these systems. A combination of four-level pulse-amplitude modulation (PAM4) and wavelength division multiplexing (WDM) allows for realization of high bandwidth-density interconnects. Microring resonator devices are promising candidates for this application due to their compact size and inherent WDM mux/demux capabilities. Previously, PAM4 modulation has been demonstrated by driving two identical ring modulators coupled to a common bus waveguide with external pattern generators [1]. However, generating uniform PAM4 level spacing is difficult with this two ring configuration. PAM4 modulation with a single ring has been realized utilizing a CMOS voltage DAC driver with the flexibility to adjust the levels to compensate for the modulator's nonlinearities [2]. Lower complexity driver circuitry is possible with an optical DAC implementation, with a 16-segment monolithically integrated microring device driven by simple non-return-to-zero (NRZ) output stages demonstrated recently [3]. However, this monolithic integration approach comes at the cost of active area-overhead in advanced CMOS processes and additional post-processing steps. This work presents a 40Gb/s transmitter designed in 65nm CMOS utilizing a two-segment optical DAC silicon photonic microring device driven by segmented pulsed-cascode drivers with flexible NRZ voltage level and edge-rate control to achieve PAM4 modulation.

2. Two-Segment Ring Modulator

As shown in Fig. 1(a), a two-segment carrier-depletion microring modulator with a radius of 12µm is utilized in this work with longer MSB and shorter LSB segments to allow for PAM4 level generation using two NRZ drivers. Two distinct p-n junctions are formed with outer p+ and inner n+ and highly doped p++ and n++ regions to provide ohmic contacts. The device displays an 18GHz bandwidth and 7500 *Q* factor, as shown in the measured transmission curves of Fig. 1(b). A high-swing (>4V) driver is required due to the relative small tunability of the ring modulator (~20pm/V). An optimal 1.9:1 MSB:LSB ratio is selected to compensate for the total device non-linearity including voltage-to-index and index-to-intensity nonlinearities to provide nominally uniform level spacing with equal drivers' swing with the input laser wavelength slightly offset from the resonant frequency, as illustrated in the linear-scale transmission curves of Fig. 1(c). Further compensation of fabrication tolerances is possible by utilizing high-speed NRZ drivers with independently adjustable output voltages swings to finely set the PAM4 levels.

3. Circuit Implementation

The proposed half-rate two-segment microring modulator transmitter block diagram is shown in Fig. 2(a). Odd and even bits from a 16-bit PRBS pattern generator are separately serialized to serve as inputs to independent MSB/LSB output drivers. Level shifters and buffers provide the required voltage levels for driving the differential high-swing pulsed-cascode drivers [4], with each driver connected to the corresponding microring segment through AC-coupling capacitors (Fig. 2(b)). Biasing resistors provide the necessary DC voltages to ensure proper reverse-bias operation of the depletion-mode modulator. Considering the AC-coupling loss, the differential high swing pulsed-cascode drivers provide up to 4.4V_{ppd} swing to each microring segment. The output driver prevents CMOS device

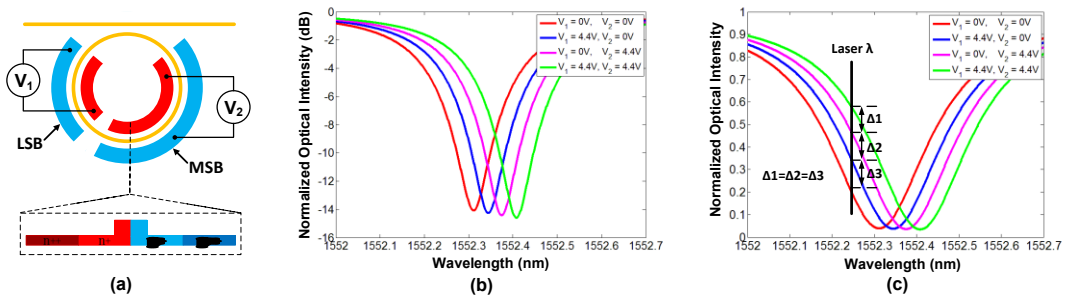

Fig. 1. (a) Top and cross-section views of the two-segment carrier-depletion microring modulator. Measured normalized transmission curves with different reverse bias voltages: (b) dB scale and (c) linear scale.

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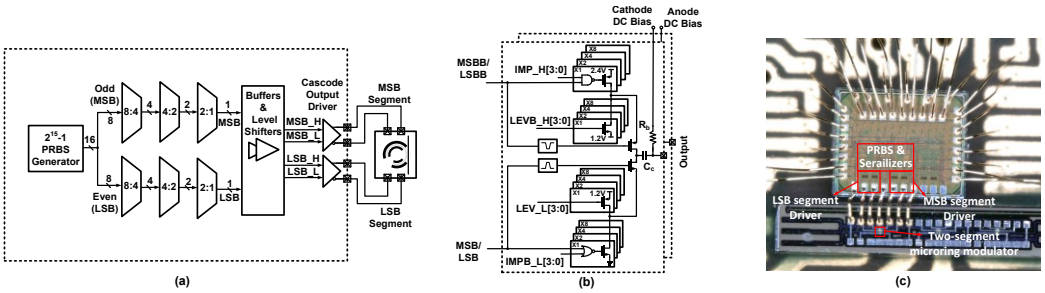

Fig 2. (a) PAM4 microring transmitter block diagram. (b) Segmented high-swing pulsed-cascode output driver. (c) Hybrid-integrated PAM4 transmitter prototype.

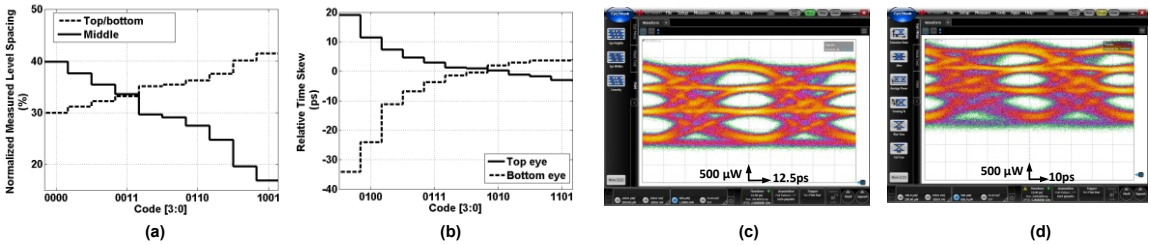

Fig 3. (a) Measured height of the three PAM4 optical eyes versus LEV code. (a) Measured time skew of the three PAM4 optical eyes versus IMP code. Measured optical eye diagrams at (c) 32Gb/s and (d) 40Gb/s.

overstress by pulsing the cascode transistors during the individual MSB/LSB output 2-level transitions. As all output transitions have the cascode transistors pulsed, this allows for sharper multi-level rise/fall times relative to a voltage DAC implementation [2]. Timing skew tuning of the three PAM4 eyes is achieved with each of the MSB/LSB output drivers segmented with the IMP control bits determining the number of driver segments connected to the microring segments to enable independent control over MSB/LSB rise and fall times. Independent control over PAM4 voltage levels in order to compensate for microring modulator nonlinearities caused by fabrication imperfections is achieved with the LEV control signals changing the number of segments connected to nominal 1.2V supply at each pull-up/down side of the driver. This effectively forms a voltage divider between the level-shifted 2.4V and nominal supply at the pull-up side and between the nominal supply and ground at the pull-down side.

3. Experimental Results

Fabricated in a GP 65nm CMOS process, the majority of the microring modulator transmitter circuitry utilizes the nominal 1.2V supply except for the pulsed-cascode output drivers and level shifting predrivers which use a 2.4V supply. The silicon photonics IC with the two-segment microring modulators was fabricated in a 130nm SOI process. A hybrid chip-on-board integration approach is utilized in this prototype (Fig. 2(c)), with the two chips placed in close proximity to minimize wirebond length. The measured PAM4 level spacing versus LEV settings are shown in Fig. 3(a) with fixed IMP control bits. While turning off all LEV segments (code 0000) provides a maximum $4.4V_{ppd}$ at the output of both drivers, this yields a relatively larger middle eye-height. Utilizing a LEV code of 0011 for the MSB driver (code=LEV_H=~LEV_L) results in close to equally spaced PAM4 optical eyes. Fig. 3(b) shows how the IMP settings can minimize timing skew of the three PAM4 eyes. With the MSB driver having maximum pull-up setting and the LSB driver having maximum pull-down setting, the MSB pull-down setting (code=IMP_L) and LSB pull-up setting (code=IMP_H) are swept. Close to zero skew is achieved with the 1001 code for both settings. The 32Gb/s and 40Gb/s PAM4 optical measurement results are depicted in the eye-diagrams of Fig. 3(c) and Fig. 3(d), respectively. The proposed CMOS driver consumes 143.5mW (4.48mW/Gb/s) and 175.2mW (4.38 mW/Gb/s) at 32Gb/s and 40Gb/s data-rates, respectively.

4. Conclusion

This work demonstrates a CMOS microring modulator transmitter which achieves high-speed PAM4 modulation using a two-segment optical DAC microring device. The AC-coupled high-swing output driver provides $4.4V_{ppd}$ swing without causing device overstress. Output driver level and edge-rate control in the segmented output stage compensates for fabrication imperfection and asymmetric dynamics of the carrier-depletion ring to provide equal PAM4 level spacing with minimal timing skew and enhanced edge-rates to achieve 40Gb/s PAM4 operation.

Acknowledgment

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