

## Chapter - 5

### Binary Parallel Adder:

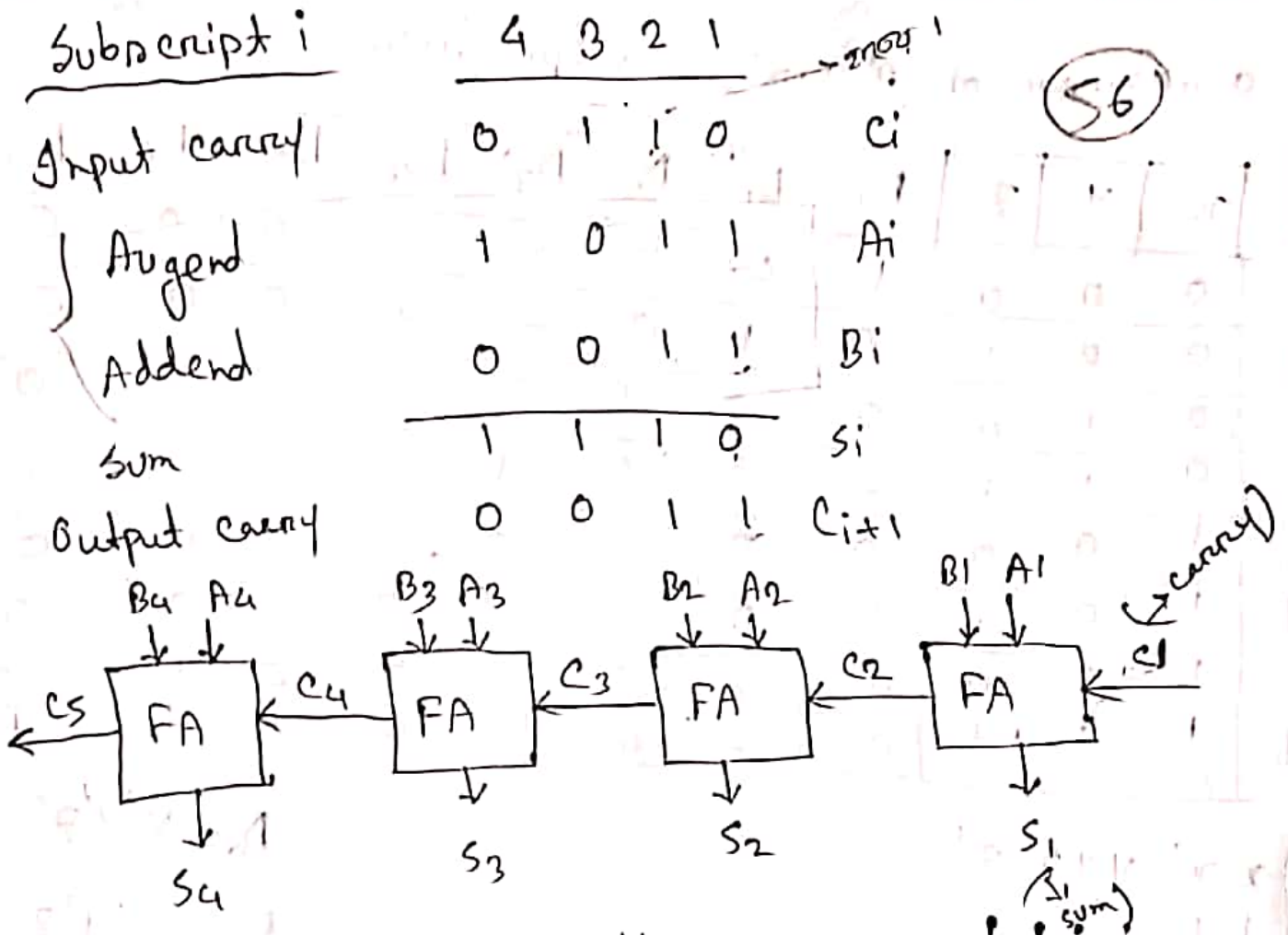
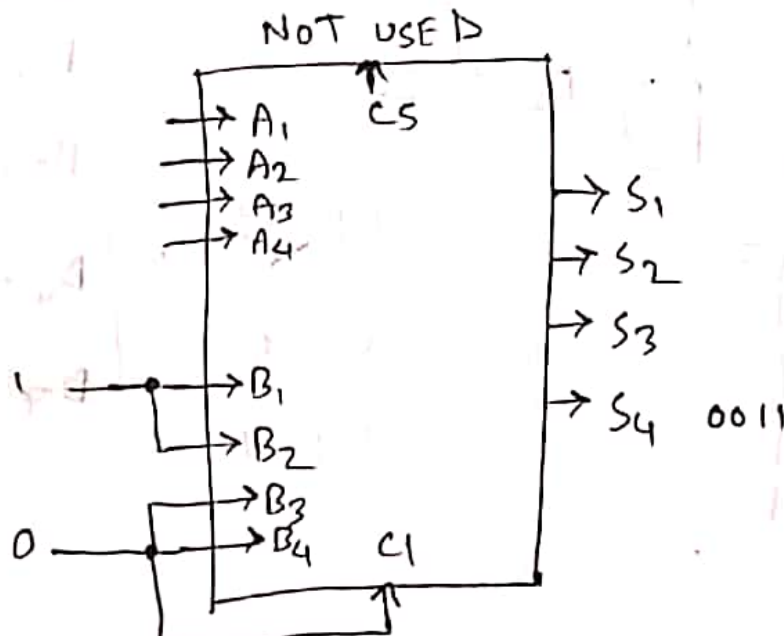


Figure : 4-bit full Adder.

Design a BCD-to-excess-3 code converter.



Decoder: A decoder is a combinational circuit that converts binary information from  $n$  input lines to a maximum of  $2^n$  unique output lines.

X	Y	Z	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

X X' Y Y' Z Z'

(57)

$$D_0 = X'Y'Z'$$

$$D_1 = X'Y'Z$$

$$D_2 = X'Y'Z'$$

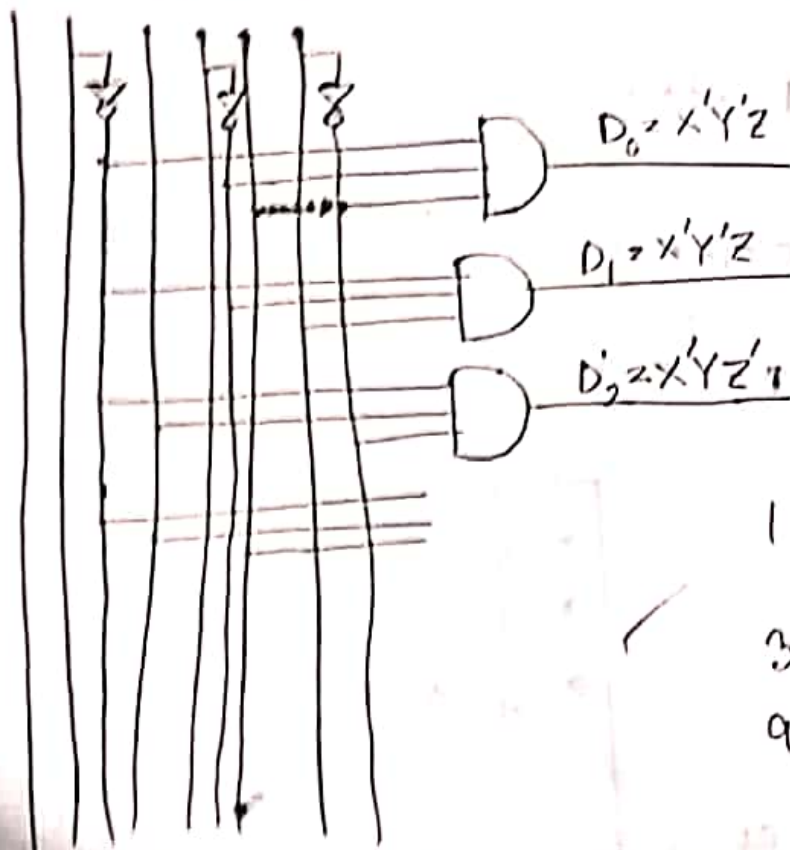
$$D_3 = X'Y'Z$$

$$D_4 = XY'Z'$$

$$D_5 = XY'Z$$

$$D_6 = XYZ'$$

$$D_7 = XYZ$$

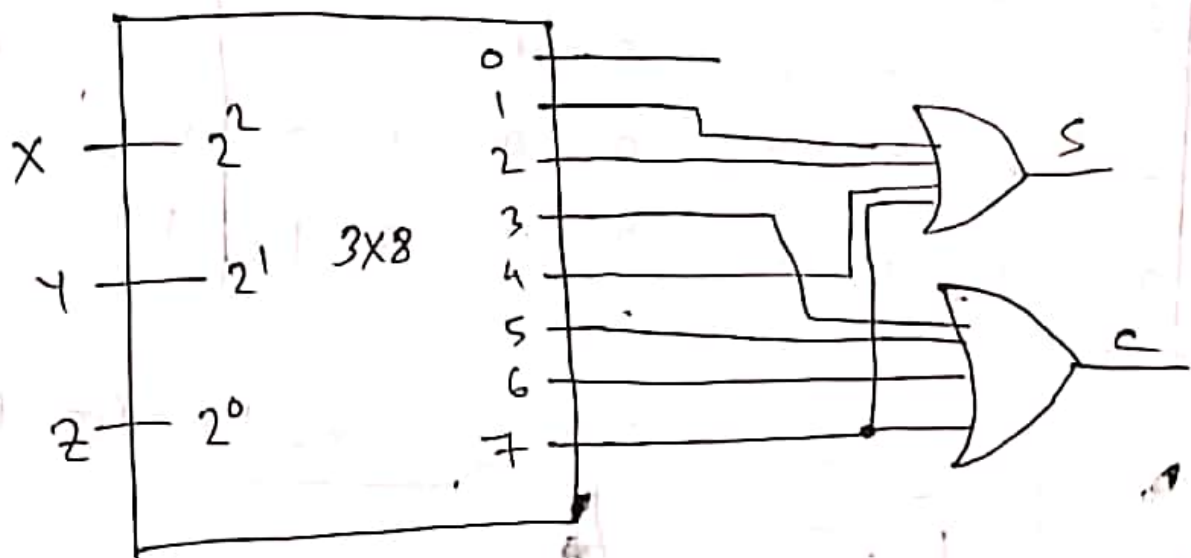


1 2 13 12  
in ou  
3 4 5 6  
9 10 11 8

Example: Implement a full-Adder circuit with a decoder & two OR Gate.

$$S(x, y, z) = \sum (1, 2, 4, 7) \quad (58)$$

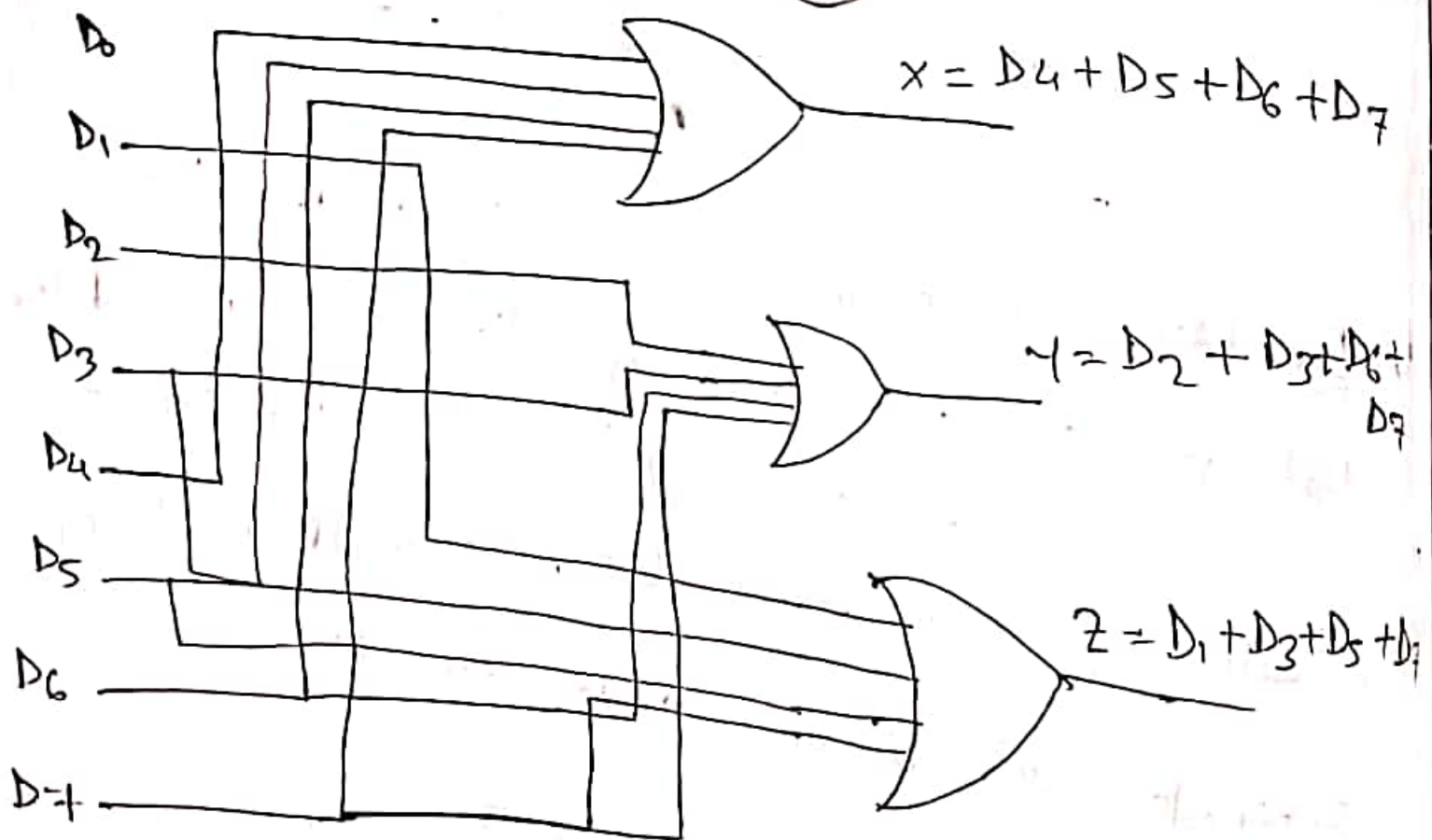
$$C(x, y, z) = \sum (3, 5, 6, 7)$$



Encoder: An encoder is a digital function that produces a reverse operation from a decoder. An encoder has  $2^n$  (or less) input and  $n$  ~~selection~~ <sup>output</sup> lines ~~whose~~ bit. The output lines generate the binary code for the  $2^n$  input variables.

D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	x	y	z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1	1
0	0	0	1	0	0	0	0	0	1	0
0	0	0	0	1	0	0	0	1	0	1
0	0	0	0	0	1	0	0	1	0	0
0	0	0	0	0	0	1	0	1	1	1
0	0	0	0	0	0	0	1	1	1	0
0	0	0	0	0	0	0	0	1	1	1

(59)



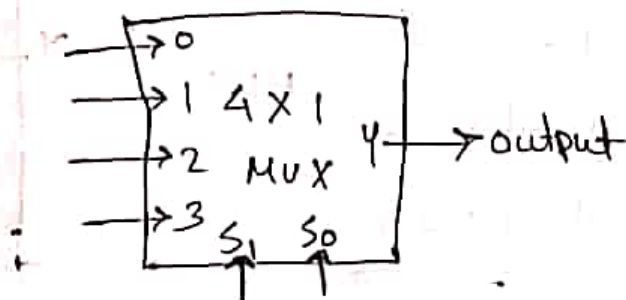


## Multiplexers:

28/04/19

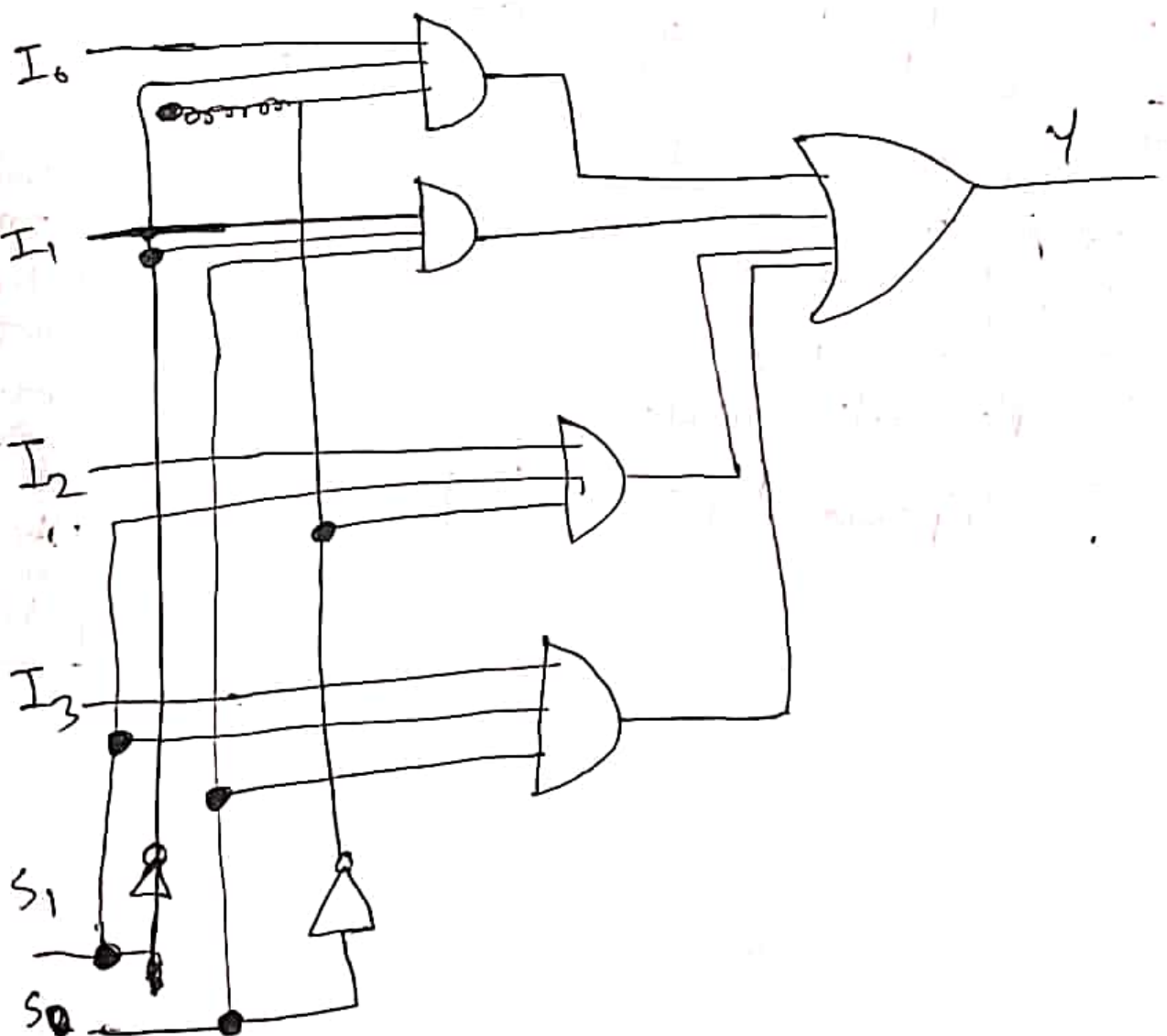
A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line.

(60)



$S_1$	$S_0$	$Y$
0	0	$I_0$
0	1	$I_1$
1	0	$I_2$
1	1	$I_3$

Selection lines.



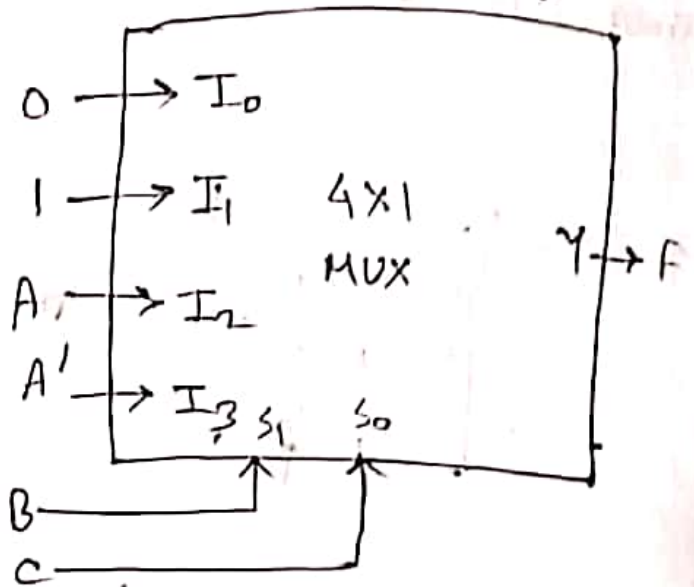
# Multiplexers

$$F(A, B, C) = \Sigma (1, 3, 5, 6)$$

Truth table:

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

(6)



Now,

	$I_0$	$I_1$	$I_2$	$I_3$
(0) $A'$	0	①	2	③
(1) A	4	⑤	⑥	7
	0	1	A	$A'$

Implementation table

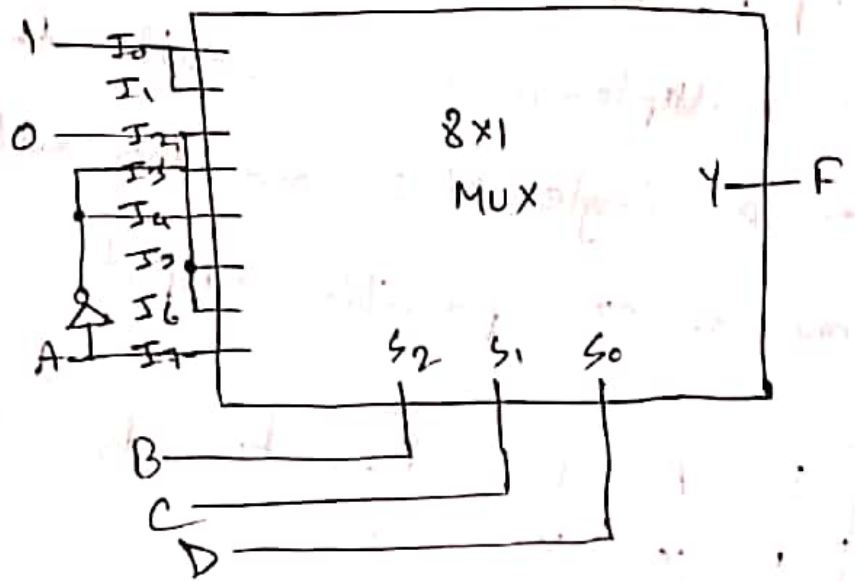
Multiplexers Implementation

Circle ના  
 અંક 0,  
 2 ને circle  
 અંક 1,  
 3 ને circle ના  
 તમે circle  
 શરૂ થઈ તુ  
 line 5 નાકર  
 બાકે અંક  
 like  $\rightarrow A$  or

$F(A, B, C, D) = \Sigma (0, 1, 3, 4, 8, 9, 15)$

(62)

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1



multiplexer implementation

	$I_0$	$I_1$	$I_2$	$I_3$	$I_4$	$I_5$	$I_6$	$I_7$
$A'$	(6)	(1)	2	(3)	(4)	5	6	7
$A$	(8)	(9)	10	11	12	13	14	(15)
	1	1	0	$A'$	$A'$	0	0	$A$

B. Demultiplexer: A decoder with an enable

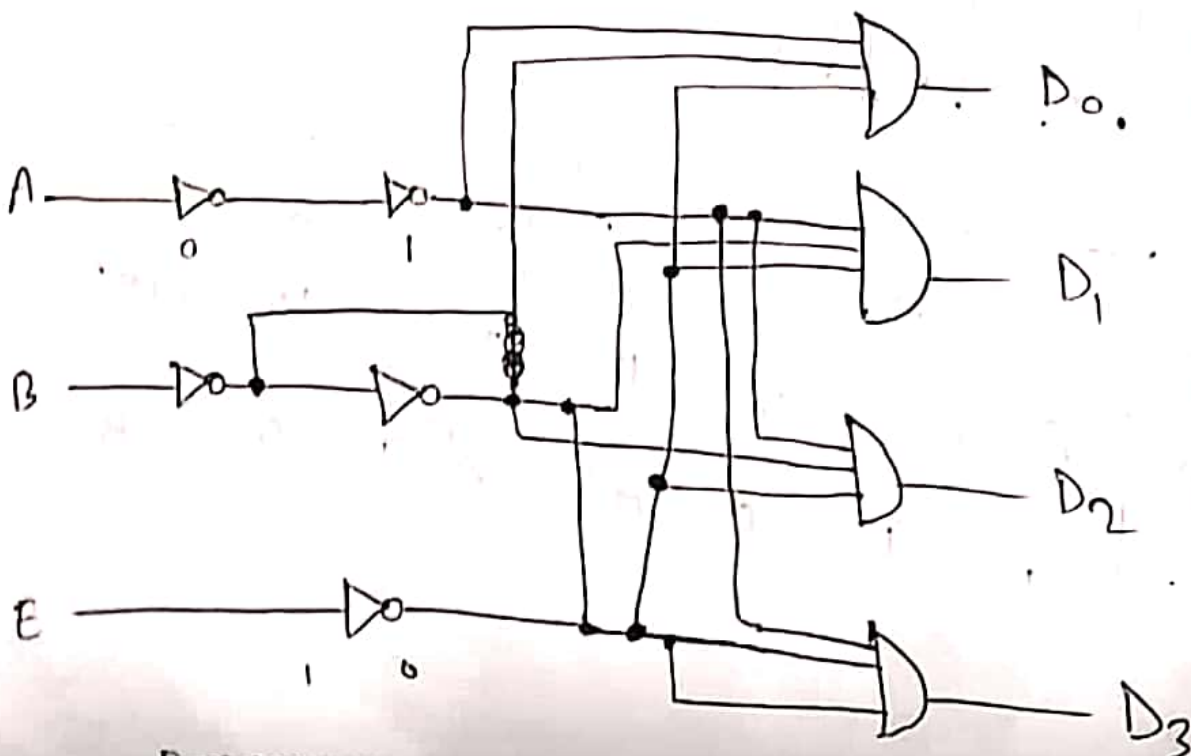
input - can function as a demultiplexer.

A multiplexer is a circuit that receive information on a single line and transmit this information on one of  $2^n$  possible output lines. (63)

E	A	B	$D_0$	$D_1$	$D_2$	$D_3$
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

ଅନୁମୋଦିତ  
ପାଠ  
ପ୍ରକାଶ  
ଓଆ  
ସାହିତ୍ୟ  
1976

E = 1 Enable  
E = 0 Disable

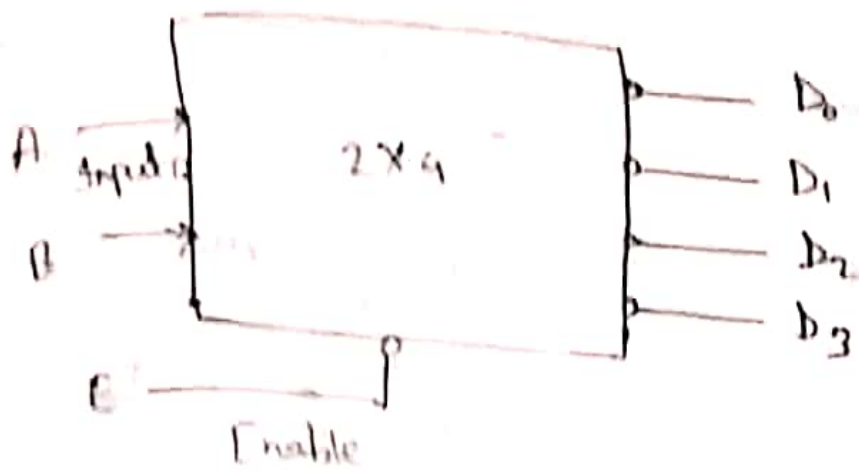


E = 0 Disable

0 1

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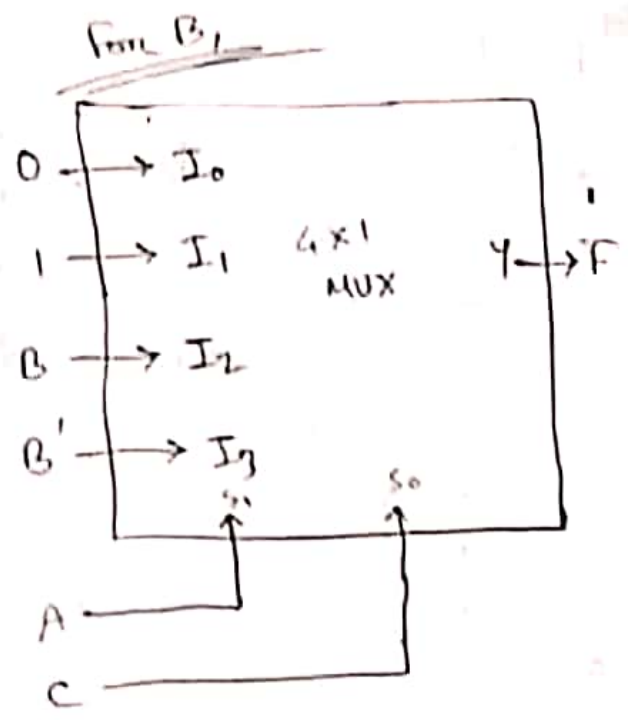


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$F(A, B, C) = \sum (1, 3, 5, 6)$

05/05/19

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

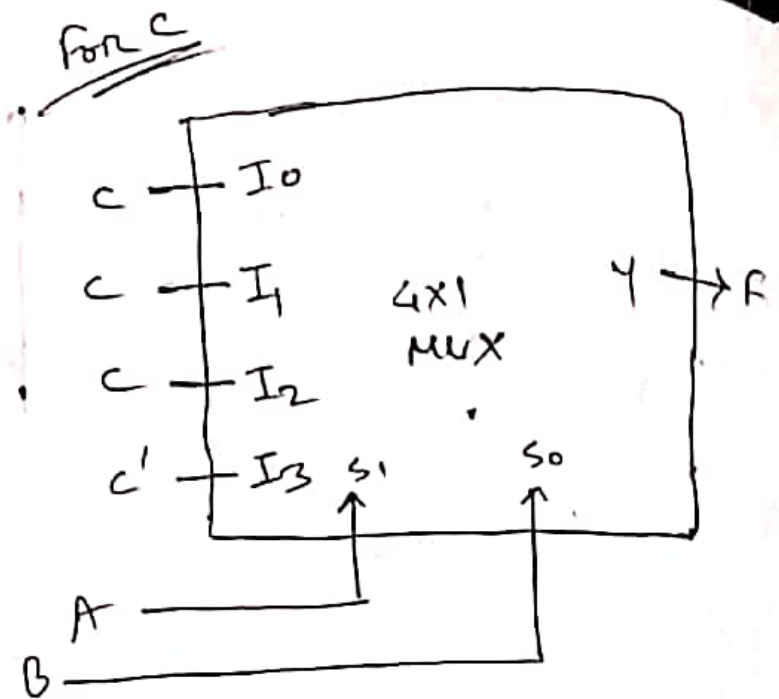


Implementation table

	$I_0$	$I_1$	$I_2$	$I_3$
$B'$	0	①	4	⑤
$B$	2	③	⑥	7
	0	1	B	$B'$

↑  
multiplexers

	$I_0$	$I_1$	$I_2$	$I_3$
$c'$	0	2	4	⑥
$c$	①	③	⑤	7
	$c$	$c$	$c$	$c'$



$$F(A, B, C, D) = \sum (0, 1, 3, 4, 8, 9, 15)$$

[A, B, C, D] Table + implementation

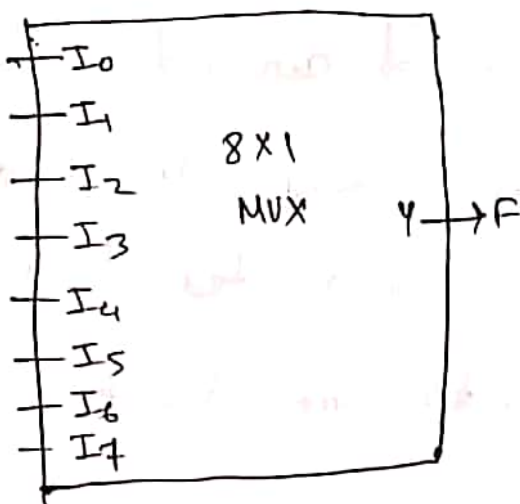
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

	$I_0$	$I_1$	$I_2$	$I_3$	$I_4$	$I_5$	$I_6$	$I_7$
$A'$	(0)	(1)	2	(3)	(4)	5	6	7
$A$	(8)	(9)	10	11	12	13	14	(15)
	1	1	0	$A'$	$A'$	0	0	$A$

	$I_0$	$I_1$	$I_2$	$I_3$	$I_4$	$I_5$	$I_6$	$I_7$
$C'$	(0)	(1)	(4)	5	(8)	(9)	12	13
$C$	2	(3)	6	7	10	11	14	(15)
	$C'$	1	$C'$	0	$C'$	$C'$	0	$C$

	$I_0$	$I_1$	$I_2$	$I_3$	$I_4$	$I_5$	$I_6$	$I_7$
$D'$	(0)	2	(4)	6	(8)	10	12	14
$D$	(1)	(3)	5	7	(9)	11	13	(15)
	1	$D$	$D'$	0	1	0	0	$D$

	$I_0$	$I_1$	$I_2$	$I_3$	$I_4$	$I_5$	$I_6$	$I_7$
$B'$	(0)	(1)	2	(3)	(8)	(9)	10	11
$B$	(4)	5	6	7	12	13	14	(15)
	$B$	$B'$	0	$B'$	$B'$	$B'$	0	$B$



# State Reduction & Assignment

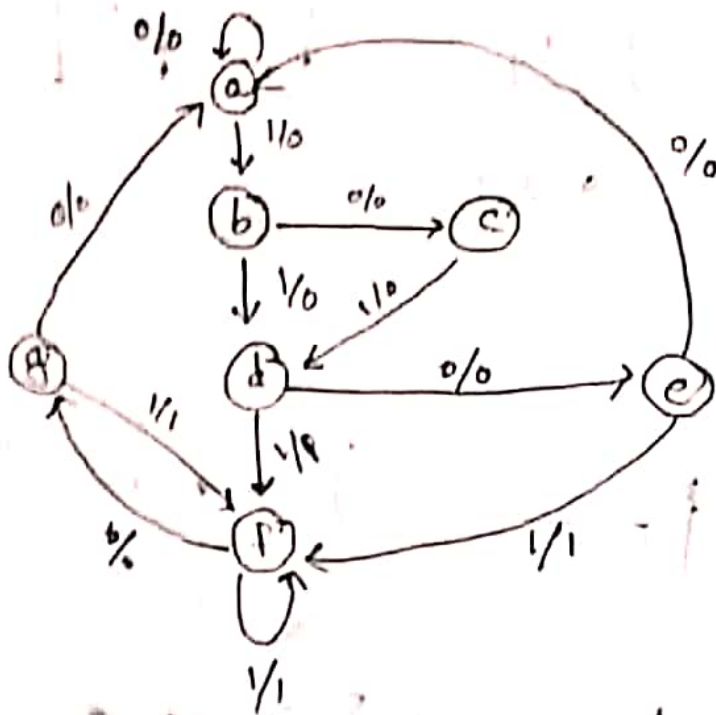
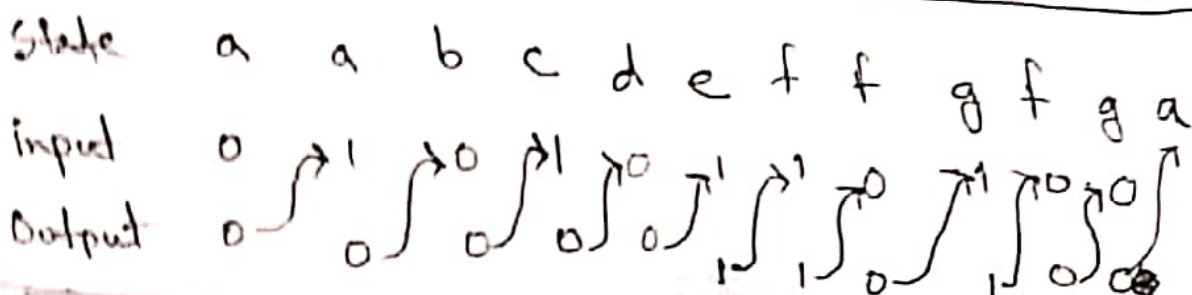


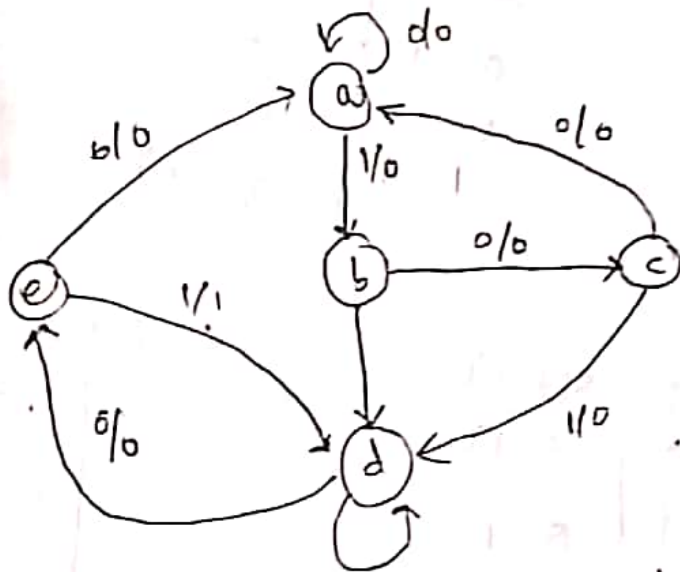
Fig: state diagram

Present state	Next State		Output	
	x=0	x=1	x=0	x=1
a	a	b		
b	c	d	0	0
c	a	d	0	0
d	e	f	0	0
e	a	f	0	1
f	b	f	0	1
g	a	f	0	1





Present state	$x=0$	$x=1$	$x=0$	$x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	<del>f</del> d	0	0
e	a	<del>f</del> d	0	1
<del>f</del>	<del>g</del> e	f	0	1
<del>g</del>	a	f	0	1



Reduced state diagram

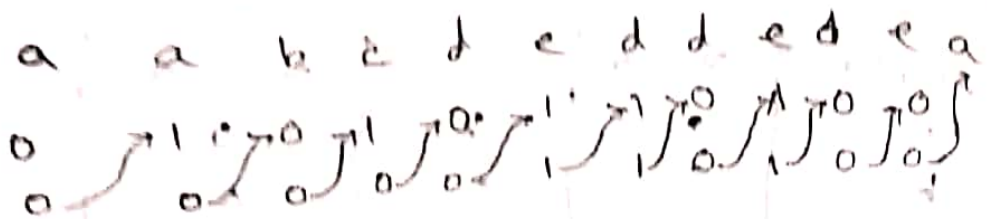
2're output  
 g a f  
 e c f  
 for g to state  
 a state for  
 f state output  
 d state output as  
 state for  
 state for  
 f state output  
 state for

Present state	$x=0$	$x=1$	$x=0$	$x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

State

input

output



10/10/10