

Lecture-1

Wednesday

9/8/23

Overview

CSE 2203: Microprocessors and Microcontrollers

Introduction + course profile

Lecture-2

Microcomputer History

Monday

14/8/23

Different microprocessor with features:

What is n-bit microprocessor?

microprocessor size = ALU size

Intel 4004:

→ 1971

→ 4-bit microprocessor

→ 4-bit data bus, 12-bit address bus

⇒ we use 4 wire lines for data computation.

⇒ n-bit address = 2^n address can be define.

→ 4-KB of memory (outside)

→ 45 instructions.

→ Problems:

(1) Speed

(2) Word width

Intel 8008 → Intel 8080 → Intel 8085 → 8086/8088

⇒ First modern ⇒ last 8-bit

8-bit processor μ processor

*** Particular generation difference.

Microprocessor (***)

→ microprocessor and cpu are used interchangeably.

→ A μ processor is a multipurpose, programmable, clock-driven, register based electronic device that reads binary instructions from a storage device called memory, accepts binary data as input and process data according to those instructions and provides results as output.

Lecture-3

wednesday

23/8/23

Introduction to

Microprocessor

Assignment: Lecture-3 Topics

→ Submission: Next class

why we need to learn microprocessor?

General purpose, no special purpose, we use it in any device.

Difference between microprocessor & microcontroller:

Microprocessor	Microcontroller
1. CPU stand alone, RAM, ROM, i/o separate.	1. CPU, RAM, ROM, memory integrated in one single chip.
2. Designer can decide on the amount of ROM, RAM & i/o ports.	2. Fixed amount of on-chip ROM, RAM, i/o ports.
3. Expensive	3. For application in which cost, power are critical.
4. General purpose.	4. Single purpose.
5. High processing power.	5. Low
6. High power consumption	6. Low
7. Customizable	7. Not customizable.

8086 Architecture

1. Clock Speed:

→ Per second 10^9 (1000M) clock cycle produce
clock speed.

→ Faster the clock speed, faster the processing speed.

$$* 800 \text{ MHz} = 800 \times 10^6 \text{ clock cycles}$$

2. Uses of transistors in computer:

→ Building Block of computers

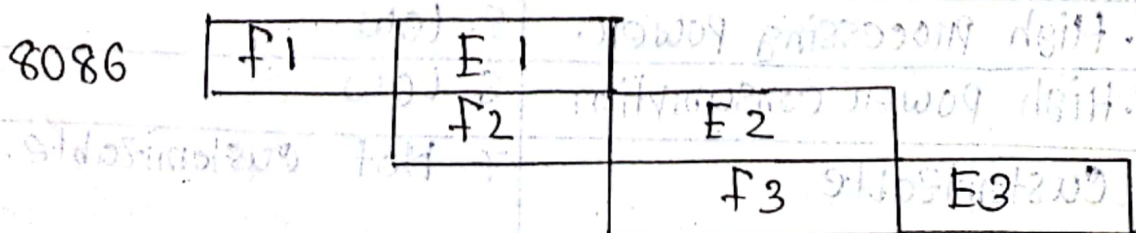
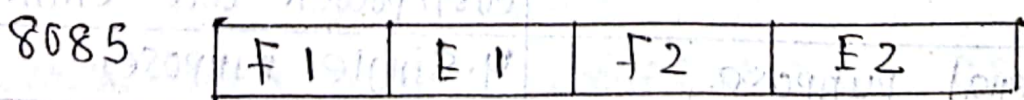
→ memory location = pair of transistors.

3. Moore's law:

→ integrated circuits double every two years.

4. 8088/86 pipelining:

8085 not pipelined processor.



8086 microprocessor:

Features:

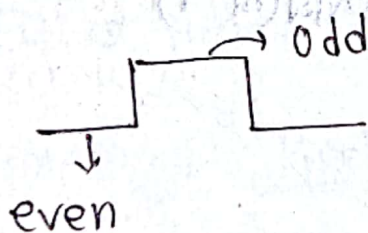
1. 20 bit address bus, 16 bit data bus.
2. multiplexed address and data bus.

৬ একই bus but অনেক কাজ করতে পারে।

3. +5V needed

4. 40 pin dual in package

* NMI → Non Maskable
interrupt.



address bus } Same bus
data bus } দিয়ে
কাজ করতে।

8086 internal Architecture: Draw + explain (***)

↓
Block Diagram

Main Unit:

- ① BIU
- ② EU

Registers:

*** Flag Register

#	0101	0100	0011	1001
	0100	0101	0110	1010
	1001	1001	1010	0011

Sign flag, $SF = 1$ (MSB = 1)

Parity flag, $PF = 1$ (even no 1)

Carry flag, $CF = 0$

Auxiliary flag, $AF = 1$ (first nibble & carry)

Zero flag, $ZF = 0$

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8086 Microprocessor

Bus Interface Unit (BIU):

- Contains 6 byte instruction queue
- Segment Register (CS, DS, ES, SS) → Special Purpose Register
- Summation Block, $\Sigma = \text{offset} +$
- Instruction point \Rightarrow current instruction location address.
- * Prefetched bytes in a FIFO called Queue.
- * EU is ready then call instruction from queue.

Pipelining

- * pipelining is a kind of parallel processing.

Memory Segmentation

→ 20 bit address bus \rightarrow can address 2^{20}

* OFFSET size 16 bit

*** Instruction \rightarrow physical address \rightarrow
 Calculate \rightarrow ?

Starting address 10000 / code segment
 offset 0029 / IP
 $\hline 10029$

Example:

If $DS = 7FA2H$ and the offset is $438EH$

(a) physical address

$7FA200$
 $438E$
 $\hline 83DAE$

(b) Lower Range: \rightarrow starting

$7FA20 + 0000 = 7FA20$

(c) Upper Range of DS: \rightarrow Ending

$7FA20 + FFFF = 8FA1F$

(d) Show the logical address:

$7FA2:438E$

Lecture-5

wednesday

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Programming languages

* Machine language \rightarrow Binary (0,1)

* Assembly "

* High-level "

Machine language:

\Rightarrow Deals with machine directly \Rightarrow No need for translation

\Rightarrow Fast

\Rightarrow No extra space needed.

Assembly language:

\Rightarrow Uses Mnemonics (MUL, ADD, MOV, DIV)

\Rightarrow Faster than high level language.

4 Parts:

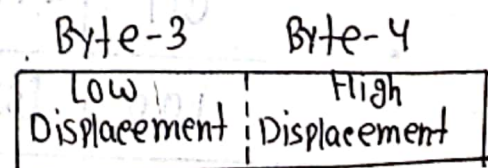
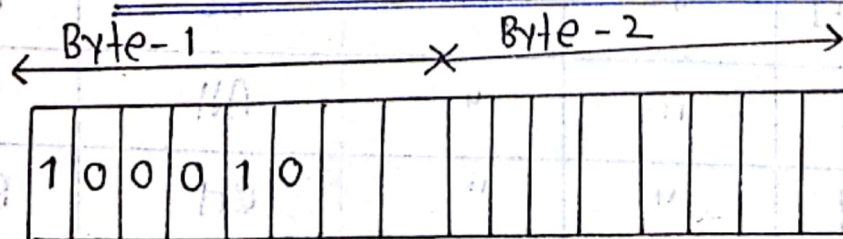
① Label ② Opcode ③ Operand ④ Comments

\downarrow
tells the
Processor what to
do.

\downarrow
data for
operation
data

High-level language: More closer to human.

MOVE Instruction Coding Format and Examples



← op code D | W | MOD | REG | R/M

W=0 \rightarrow Byte
W=1 \rightarrow Word

D=0 From Register
D=1 To Register

OR
Direct Address Low Byte Direct Address High Byte

Register		CODE
W=0	W=1	
AL	AX	000
BL	BX	011
CL	CX	001
DL	DX	010
AH	SP	100
BH	DI	111
CH	BP	101
DH	SI	110

Register Transfer

Memory Transfer

MOD R/M	00	01	10	11	
				W=0	W=1
000	$[Bx] + [SI]$	$--- + d8$	$--- + d16$	AL	AX
001	$" + [DI]$	"	"	CL	CX
010	$[BP] + [SI]$	"	"	DL	DX
011	$" + [DI]$	"	"	BL	BX
100	$[SI]$	"	"	AH	SP
101	$[DI]$	"	"	CH	BP
110	$d16$ Direct Address	$[BP] + d8$	$[BP] + d16$	DH	SI
111	$[Bx]$	"	"	BH	DI

MOV SP, BX

OPCODE = 100010

D = 0, W = 1

MOD = 11

REG = 011

R/M = 100

MOV SP, BX

OPCODE = 100010

D = 1, W = 1

MOD = 11

REG = 100

R/M = 011

MOV CL, [BX]

OPCODE = 100010

D = 1, W = 0

MOD = 0100

REG = 001

R/M = 111

MOV 43H[SI], DH

OPCODE = 100010

D = 10, W = 0

MOD = 01, REG = 110

R/M = 100

*** Assignment → Move instruction all exercise + example.

18/9/23 →

Submission.

→ Language

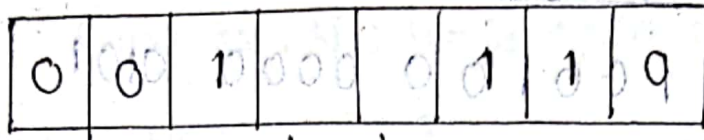
Lecture-6

18/9/23

Monday

MOV CS:[BX], DL

SEGMENT OVERRIDE PREFIX

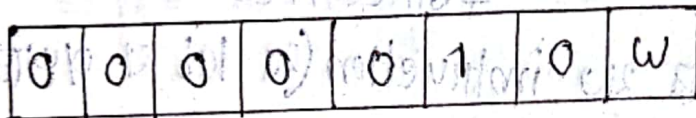


Segment Register

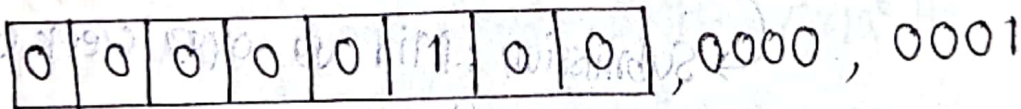
ADD AL, 01H

Segreg	code
CS	01
DS	11
ES	00
SS	10

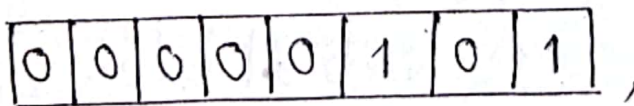
The Format is-



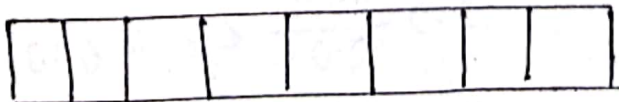
data byte, data byte



ADD AX, 3201H



ADD AL, 05H



IN AL, 05H

→ Appendix A to 8086 instruction
is format 7H41

*** MOV, ADD, IN

Format for IN -

1 1 1 0 0 1 0 0

, data byte, data byte

1 1 1 0 0 1 0 0 0 0 0 0 1 0 1 0

IN AX, 3205H

1 1 1 0 0 1 0 1

E5H, 05H, 32H

+ directives

*** Chapter-6 এর ২০ instruction (২৭ lab ও প্রশ্নের

২(৭২) Syntax, Explanation, example Assignment.

Submission : Mid এর পরের week এর
বুঝার ।

1 0 1 0 0 0 0 0

1 1 1 0 0 1 0 0

অন্যান্য প্রশ্নের ওপর

IN AX, 3205H

*** MON, 05.11.2020

Lecture-7

Wednesday

4/10/23

Instruction Timing and Delay loops

clock cycles

MOV cx, N ; 4 = C_0 → clock cycle overhead

KILL TIME : NOP ; 3
NOP ; 3

LOOP KILL TIME : 17 or 5 → Jump না করে
পরের line এ আসে

$$\therefore C_T = C_0 + N(C_L) - 12$$

$$\Rightarrow N = \frac{C_T - C_0 + 12}{C_L} = \frac{5000 - 4 + 12}{23} = 218 = 0DAH$$

□ 1ms delay = 1000 μ s delay

□ 8086 μ p, clock speed = 5MHz = 5×10^6 Hz

$$n = \frac{1}{T}$$

$$\Rightarrow T = \frac{1}{n} = \frac{1}{5 \times 10^6} = 0.2 \mu s$$

→ 0.2 μ s → 1 c.c

$$\therefore 1 \text{ " } \rightarrow \frac{1}{0.2} \text{ "}$$

$$\therefore 1000 \text{ " } \rightarrow \frac{1000}{0.2} \text{ c.c} \\ = 5000 \text{ c.c}$$

□ 2.5 ms Delay

$$2.5 \text{ ms delay} = 2.5 \times 10^3 \mu\text{s}$$

$$0.2 \mu\text{s} \rightarrow 1 \text{ cc}$$

$$\therefore 1 \mu\text{s} \rightarrow \frac{1}{0.2} \text{ cc}$$

$$\therefore 2.5 \times 10^3 \rightarrow \frac{2.5 \times 10^3}{0.2} = 12,500$$

$$\therefore N = \frac{12,500 - 4 + 12}{1} = 12,508 \approx 12,500$$

□ Nested LOOP: → অনেক বড় time দরকার হলে

MOV BX, COUNT1 ; 4

ENTD1: MOV CX, COUNT2 ; 4 (COUNT1)

ENTD2: LOOP ENTDN2 ; ((17 x COUNT2) - 12) COUNT1

DEC BX ; 2 (COUNT1)

JNZ ENTDN1 ; 16 (COUNT1) - 12

□ 30 s delay

Lecture-8

5/10/23

Thursday

8086 Addressing Modes

→ slide

Some important topics:

① Editor

④ Locator

② Assembler

⑤ Debugger

③ Linker

⑥ Emulator

→ Assignment

CT Syllabus: Lecture 1-8

Lecture-9

9/10/23

Monday

Instruction detail with example.

Directives " " " " " "

⇒ DB, DW, DD,

⇒ CMP instruction: क्या रीति की ?

CMP Destination, Source

CMP Bx, cx