

CSE 2203

[part - manik sir]

Exam - 2016

Section-A

a) The advantage of using a CPU register

for temporary data storage over using a memory location is about speed.

By using the CPU register, the information

is kept local to the CPU. By storing a value in a memory location, a lookup has to be performed to retrieve it.

A register is merely a very fast piece of storage that exists directly on the microprocessor and can be accessed synchronously without any waiting. It is conceivable to make a processor where we have no registers but only memory.

would be probably very slow.

(a) ~~divide - don't~~

~~base 102~~

(b)

~~base 1000~~

Segmentation: A segment is a logical unit of memory that may be up to 64kb long.

Segmentation is the process in which the main memory of the computer is logically divided into different segments, and each segment has its own base address.

The advantage of segmentation in 8086 is that it is used to enhance the speed of execution of the computer system, so that the processor is able to

fetch and execute the data from the memory easily and fast.

It provides a powerful memory management mechanism.

Data related or stack related operations can be performed in different segments. Code related operations can be done in separate code segments. It allows to process to easily share data. Segmentation allows to extend the addressability of the processor.

It is possible to enhance the memory size of code, data or stack segments beyond 64 KB by allotting more than one segment for each area.

High level language programs are machine independent. They are easy to learn, easy to use, and convenient for managing complex tasks.

Assembly language programs are machine specific. It is the language that the

processor to directly understand.

Trade-offs are actually the trade-off that exchange something of value, especially as part of a compromise.

So there are many trade-offs of choosing between assembly language and HLL.

Assembly language was created as an exact shorthand for machine level coding, so that we wouldn't have to count 1's and 0's. High level language is readable to users but assembly language is readable to processors. Assembly language is nearly compared up to HLL. It has a fixed program set and it is easier for a processor to read assembly code. On the other hand, high level language is much more easy to the users who code and user friendly.

SS contains 5000H, SP contains FFE0H

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SP contains FFE0H

i) Physical address: ~~means~~ physical address

physical address is the actual position of code and data bytes in physical memory.

ii) The mentioned segment is "stack segment"

SS contains 5000H

so, lower range = base of the segment

Physical address, $DS * 10H + 5000H$

Segment register has 16 bit address line

but memory has 20 bit address line.

so we have to convert it into 20 bit

by padding a zero

lower range = 5000H

Upper range (top of the stack)

$$= \text{Base address} + \text{offset} = 5000H + FFE0H$$

$$= 5FFEOH$$

iii) The upper range of the stack

segment. is 5FFEOH
. 10000000000000000000000000000000

The lower range off the segment is 5000m

\therefore the maximum size of ~~is 5FFEOH - 50000H~~

mission, lecture 20f of repeating code, ~~FFF~~¹¹¹ FF E0H

That is around 64KB, so this is

—

as a result of trapping *bombyx* and *(ii)*

(e)

HOTDOGS California 200

i) 32 bit microprocessor is feeding with 3 GHz clock generator.

~~2. each~~ the time for each clock cycle

$$\text{is } 1/(3 \text{ GHz}) = 0.3 \text{ ns}$$

To complete an instruction, 20 cycles are needed. So $0.3\text{ ns} \times 20 = 6\text{ ns}$

$$\text{needed. So } 0.3 \text{ ns} \times 20 = 6 \text{ ns}$$

Q. The processor speed is $\frac{1}{6\text{ns}}$ ins/sec.

177

ii) The executing code size is 64KB
 average instruction size is $32\text{bit} = 4\text{B}$
 \therefore the code has around $\frac{64\text{K}}{4} = 16000$ instruction

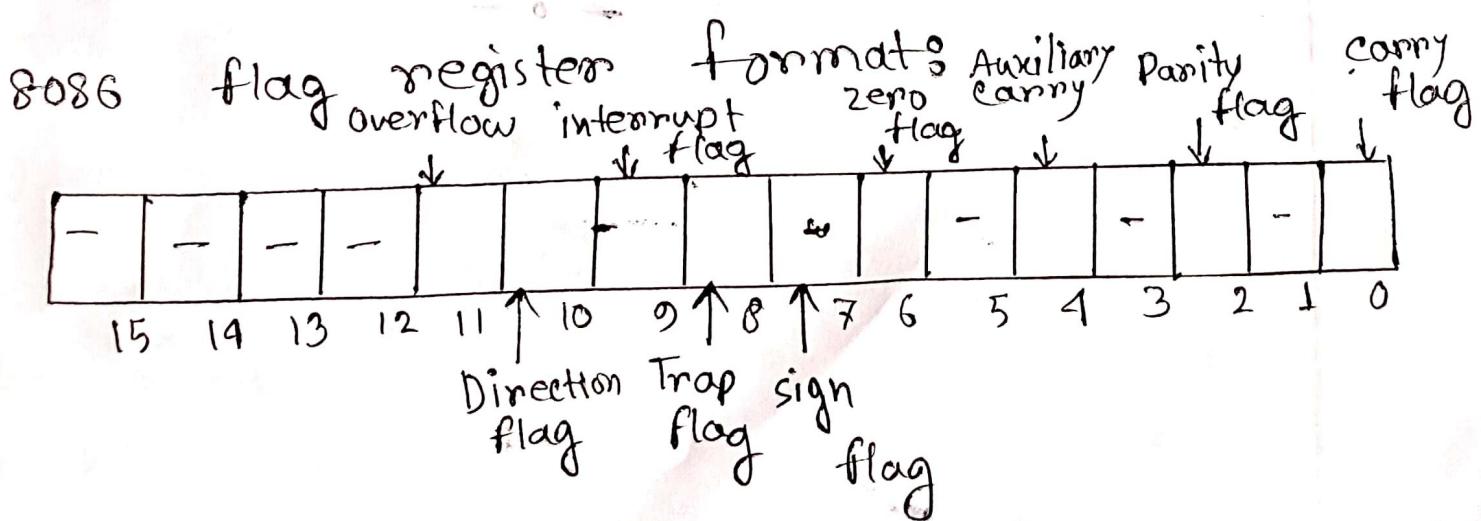
each instruction needs 6ns.

\therefore It would take around $(16000 \times 6\text{ns})$

$$= 96 \times 10^{-6} = 9.6\mu\text{s}$$

(Ans)

Flag register is one of the special purpose registers. The flag bits are exchanged to 0 or 1 depending upon the value of result after arithmetic or logical operations.



In 16bit status word, nine individual bits of the flag register are used as control flag (3 of them) and status flag (6 of them). The remaining 7 are not used.

code : mov, AL, OFFH
ADD AL, 01H
after the execution
for this code, the status flags will be

CF \rightarrow 1 (Carry flag is set because of unsigned overflow)

PF \rightarrow 1 (Parity flag is set because even number of 1's)

AF \rightarrow 1 (Overflow in lower nibble)

ZF \rightarrow 1 (result is zero)

SF \rightarrow 0 (result is unsigned)

OF \rightarrow 0 (it was not a signed overflow)

- o -

(b)

Addressing modes are the different ways in which a processor can access data are called addressing modes.

i) mov AX, [BX]

This mode is a register based indirect addressing mode. In this mode, the effective address of the memory may be taken directly from one of the base registers or index register by instruction.

This instruction moves a word from the data segment in AL and AH respectively. The address pointed by BX and BX+1 is

ii) mov AX, [BX+8]

This mode is register relative addressing mode. The operand address is calculated using one of the base registers and a displacement of 8 or 16 bits.

iii) $\text{MOV} [BX + SI], BP$

This mode is ~~is~~ base indexed addressing mode because here the operand address is calculated as base register plus an index register.

~~[BX + SI]~~ MOV

iv) MOV AX, OFFFEH

This mode is ~~is~~ immediate addressing mode.

Hence the operand is ~~is~~ specified in the instruction itself.

In the above instruction, $OFFFEH$ is directly moved to AX register.

~~[BX + SI]~~ MOV

(c)

(d)

H₂O + IA → G

no effect on water. H₂O + IA → G
IA at H₂O does not affect G

IA does not affect G

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|

H₂O + IA

Draft step 3 o.w. shot 90

11/8 NT not

diff resistance

H₂O + IA + DNA G

No effect on water. DNA does not affect G

Effect of DNA on water is not consistent with

now bus. source of H₂O + IA + DNA

Effect of DNA on water is not consistent with

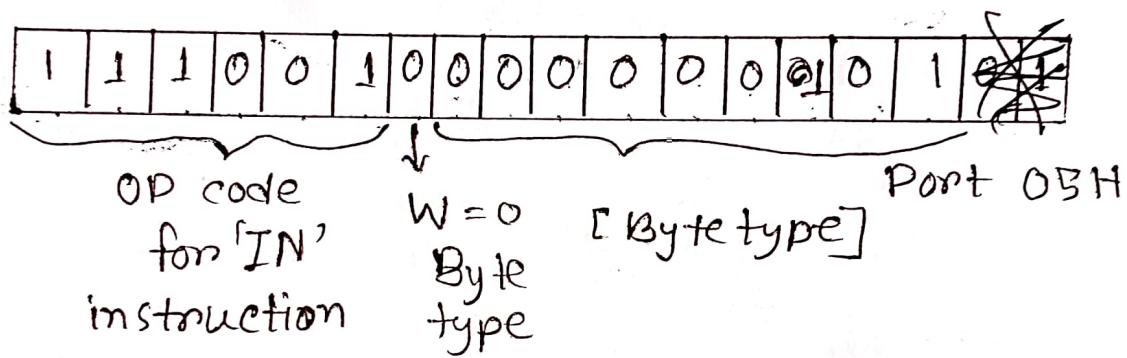
Effect of DNA on water is not consistent with

(d)

i) IN AL, 05H

This means, the IN instruction will copy a byte from port 05H to AL.

binary code:



ii) AND AL, 0FH

The 'AND' instruction means, the will do AND operation for the operand bits.

For 0FH, it'll mask out upper 4 bits of AL.

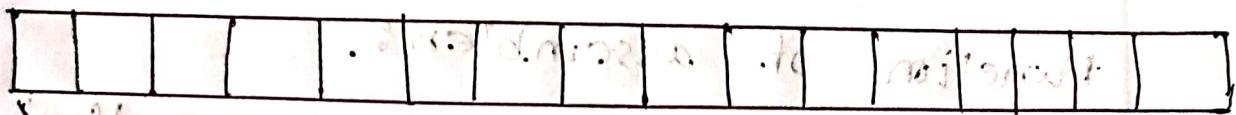
Let, $AL = 0011101$ | $0FH = 00001111$

Then,
AND

AL, OFH

: now, $AL = 00001101$

binary code:



for 'AND' instruction

iii) ~~MOV [BX], CX~~ move [BX], CX to say

This instruction will copy a word from CX register to a memory location from [BX] register.

binary codes ad nos derived solutions for

1000010010000111
OP code [BX]

from register

move word

CX reg [BX]

memory, sh

no displacement

processor

3(a)

Function of assembler.

An assembler is a program that converts assembly language into machine code. It takes the basic commands and operations from assembly code and converts them into binary code that can be recognized by a specific type of processor. Assemblers are similar to compilers in that they produce executable code.

Function of emulators

An emulator device can be used to test how an app would function on different devices. Emulating various devices informs app developers of any necessary changes to the functionality of their app, as well as improving UX and highlight other areas for improvement.

(b)

MOV SP, 0050H

PUSH AX

CALL STRING₂

POP AX

STRING₂ PROC NEAR

~~STRING₂~~

DUSHF

PUSH AX

PUSH CX

POP CX

POPAX

POPE

RET

STRING₂ ENP

Before Push, AX
SP → 0050H
AX → 0050H

SP → 004E
after push
AX →

SP after

call STRING₂
→ 004C

SP after

DUSHF → 004A

SP after

PUSH AX →

SP after

push CX →

SP, after

push CX →

SP after

POPE → 0046

SP after

RET → 0048

SP after

POPE → 0048

SP after

RET → 0048

SP after
POP AX

SP after

RET
004E

SP after

POPF
004C

SP after

POPAX
004A

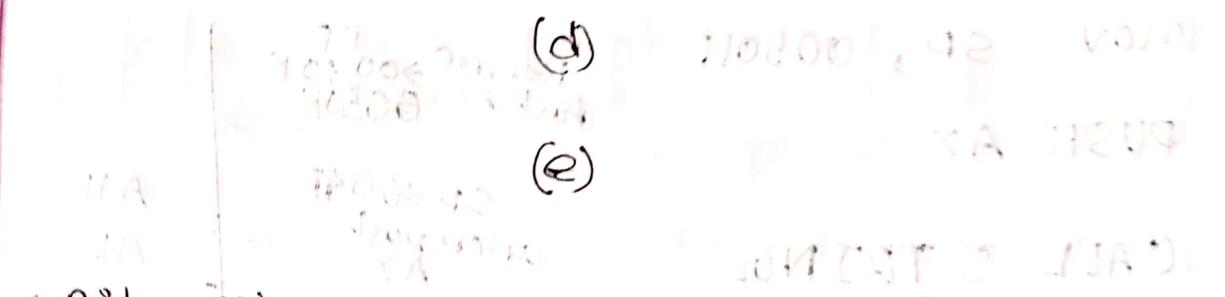
SP after

POP CX
0048

SP after

POPEX
0048

decrement of 2 and for POP
For push, SP decrement by 2
instruction, SP increment by 2



Bit - slice microprocessor

A ~~bit~~ ^{bit} - Slice microprocessor (Bsm) is a ~~micro~~ ^{mini} processor designed as a module with the primary purpose of being able to assemble multiple identical such microprocessors to form a larger processor of some desired word size.

Bit slice microprocessors can be cascaded to produce any conventional as well as unconventional word sizes.

Q (a, b, c, d)