Hafsah Shahzad

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OBJECTIVE

Recent PhD graduate specializing in **Deep Learning**, **Performance Engineering** and **Hardware Validation**. Experienced in accelerating **Machine Learning algorithms** for data-centric applications and optimizing design flow for **CPU, FPGA and GPU architectures**. Skilled in **post-silicon system testing and validatio**n, with expertise in **Reinforcement Learning** and **Bayesian Optimization** to enhance system efficiency.

EDUCATION

BOSTON UNIVERSITY, *Boston, USA, 2021- 2025*
PhD in COMPUTER ENGINEERING, May 2025

TECHNICAL UNIVERSITY MUNICH, *Munich, Germany, 2013-2015*
MSc in POWER ENGINEERING, Oct 2015

LAHORE UNIVERSITY OF MANAGEMENT SCIENCES (LUMS), *Lahore, Pakistan, 2009-2013*
BS in ELECTRICAL ENGINEERING, June 2013
See below for synergistic and leadership activities.

Relevant Courses: Computer Architecture, Programming Multicore and GPU, Digital System Design, Power Electronics, High Voltage Technology, Electrical Machines, Digital Signal Processing, Devices and Semiconductors, Advanced Control, Energy Storage, Nanotechnology, Computer networks, Data Acquisition and Interfacing, Computer Organization and Assembly Language, Introduction to Matlab

SKILLS

Programming Languages:
Python(Scikit-Learn,Tensorflow,Pytorch,Keras), SQL, C/C++, Matlab/ Simulink, VHDL/Verilog, Latex,CUDA
Software & Tools:
Vivado, Vitis, gem5, Linux perf, TestStand, LabView, Quartus II, Proteus 7(Ares, ISIS), Altium, Spice Simulators
Hardware Design and Testing:
Digital/Analog Circuit Design, Power Management, Control Loop Design, PCB Design, Soldering, Device Validation, Data Evaluation, Data Acquisition
Deep Learning:
CNN, RNN, LSTM, Large Language Models (LLM), Fine-tuning, , RAG, Raylib, Transformers, Attention

RESEARCH AND PROJECTS

BOSTON UNIVERSITY ***Computer Architecture and Automated Design Lab, ECE Department***

Reinforcement Learning of Compiler Heuristics ***Feb 23 to May 25***
Developed infrastructure to train deep reinforcement learning models that can predict compiler heuristics resulting in up to 80% reduction in binary size. Improved algorithm accuracy by exploring code embeddings, heuristics choices, reward shaping and classifier based predictions.

CodeXplorer - Framework for Feature Extraction from GCC's Gimple ***June 23 to May 25***
Designed an automated framework for extracting over 100 function-level features from GCC's intermediate representation, enhancing feature selection and comparison for optimization tasks.

Neural Network based Cost Model for GCC Binary Size Prediction ***June 24 to May 25***
Designed and implemented a neural net model to predict GCC binary size based on code features and flag transformations, improving compilation efficiency with reasonable accuracy.

Source To Source Compilation For Performance ***Sept 22 to May 25***
Developed framework for automatically annotating high level language programs to improve the quality of code generated by modern compilers, such as GCC, LLVM, Vitis HLS, Intel HLS

Reinforcement Learning Based Compiler Tuning for Custom Hardware Generation ***Jan to Aug 22***
Designed a machine learning based framework to determine the optimal sequence of compiler passes for high level synthesis compilations. Explored new learning strategies for compiler tuning and metrics to evaluate

their impact, hence enabling developers to choose best possible reinforcement learning training options based on their target goals.

Evaluation of High Level Synthesis Tools ***Sept to Dec 21***

Testing High Level Synthesis microbenchmarks and design patterns on tools such as LegUp and Vitis. Explore limitations and performance when synthesizing C benchmarks for FPGA specific backends.

Survey and Taxonomy of FPGA Cloud Architectures ***Jan to Mar 21***

Exploration and analysis of existing and novel cloud architectures for FPGA workloads. Classified these into taxonomic categories to analyze relationship between design choices and system constraints and to better describe and contrast different cloud FPGA architectures.

UNIVERSITY OF COLORADO, BOULDER
CoPEC - Colorado Power Electronics Center

Rectifiers and Inverters for Single Phase UPS Applications ***Jun to Aug 17***

Evaluated trending topologies. Designed the control loop, simulated the UPS system on PLECS and determined the loss model.

TECHNICAL UNIVERSITY MUNICH* and *TEXAS INSTRUMENTS, Freising Germany

Master's Thesis ***Feb to Sept 15***

Maximum Power Point Tracking Solutions for Low Power DC-DC Converters
Simulated and designed ultra-low power PCB circuits that enable the system to sense and monitor maximum power from solar cells under varying light and temperatures, efficiently powering wireless sensor nodes.

Analyze Electrical Behavior of Lithium Battery Types for Metering Applications ***Sept to Nov 14***

Texas Instruments, Freising Germany
Battery characterization- designed and developed measurement setup, executed and analyzed the results.

Lithium Ion Capacitor for Hybrid and Battery Electric Vehicles ***Sept 14 to Jan 15***

Lehrstuhl für Elektrische Energiespeichertechnik- EES (TUM)
Research into Lithium Ion Capacitor technology, market survey for HEV, field of applications, future prospects

Hardware And Software Design For Resolver Demodulation ***Mar to Jun 14***

Lehrstuhl für Elektrische Antriebssysteme und Leistungselektronik (TUM)
Simulated and designed PCB circuit, Testing and debugging, VHDL coding on Quartus II and ModelSim.

LAHORE UNIVERSITY OF MANAGEMENT SCIENCES-School of Science and Engineering (LUMS-SBASSE)

Bachelor's Thesis ***Sept 12 to May 13***

Maximum Power Point Tracking For Turbine-Generator Systems
Simulated and designed hardware circuits to extract maximum useful energy from renewable systems such as solar thermal, wind and micro-hydroelectric.

PROFESSIONAL EXPERIENCE

GRADUATE TEACHING ASSISTANT ***Aug 22 to May 23***

Graduate Teaching Assistant for EC413: Computer Organization and Assembly Language.
Lead discussion sections, manage staff of graders and lab assistants, substitute lecturer

VALIDATION ENGINEER ***Texas Instruments, Jan to Dec 16***

Perform validation measurements on the device over different conditions using lab equipment, automation software like Labview and Teststand.

- Improved the post-silicon validation process using methods to enhance data collection efficiency and test time reduction
- Developed new measurement techniques i.e. varied start-up timing tests, frequency measurements, load and line transients, stability analysis of closed loop systems
- Integrated new lab instruments into measurement automation to improve existing procedures

Provide product development support to design, system and other interfaces in the project team. This includes testing special design features of the device and datasheet graphs and supporting critical customer measurements.

WORKING STUDENT ***Texas Instruments***

Oct to Dec 15

Lab measurements and automation on Labview and Teststand.

Nov to Dec 14

Thermal and electrical measurements on different silicon types, efficiency analysis of converters, providing customers' application support.

CERTIFICATIONS

DEEP LEARNING SPECIALIZATION ***Coursera, May 25 to Present***

Build and Train Neural Networks, Building CNN and RNNs, work with HuggingFace tokenizers and transformer models, work with NLP and Word embeddings, apply deep learning to applications

IBM DATA SCIENCE PROFESSIONAL CERTIFICATE ***Coursera, July 20 to Oct 20***

Business methodology for Data Science ,IBM Watson Studio, Building Machine Learning models

DATA SCIENCE CAREER PATH ONLINE CERTIFICATION ***Codecademy, Feb 20 to June 20***

Data Analysis with Pandas, Data Visualization, Statistics with Numpy, Hypothesis Testing with SciPy, Web Scraping, Natural language processing

POWER ELECTRONICS SPECIALIZATION CERTIFICATION ***Coursera online certification, Oct 17 to Mar 18***

Power Electronics, Converter Circuits and Control

AWARDS

- **DISTINGUISHED COMPUTER ENGINEERING FELLOWSHIP -** Boston University (2021-2025)
- **BEST PAPER AWARD -** 25th International Symposium on Quality Electronic Design *(ISQED 2024)*
- **GOLD MEDAL -** Technical University Munich (Oct 2015)
- **DEUTSCHLAND STIPENDIUM SCHOLARSHIP** - Siemens and Technical University Munich (2014-15)
- **DEAN'S HONOR LIST** - LUMS School of Science & Engineering (2009-2013)

PUBLICATIONS

JOURNAL PUBLICATION

[1] Bobda, Christophe, et al. (2022) "The Future of FPGA Acceleration in Datacenters and the Cloud." *ACM Transactions on Reconfigurable Technology and Systems (TRETS)* 15.3: 1-42.

[2] Shahzad, Hafsah, et.al. (2025) "AnnotationGym:A Generic Framework for Automatic Source Code Annotation",(submitted).

CONFERENCE PUBLICATIONS

[3] Shahzad, Hafsah, et.al. (2024) "Smart Learning of GCC Flags for Function Size Reduction",(to be submitted*).*

[4] Shahzad, Hafsah, et.al. (2024) "A Neural Network Based GCC Cost Model for Faster Compiler Tuning", *28th IEEE High Performance Extreme Computing Conference (HPEC).*

[5] Shahzad, Hafsah, et.al.(2024) "AutoAnnotate: Reinforcement Learning based Code Annotation for High Level Synthesis",25th International Symposium on Quality Electronic Design *(ISQED).* ***Best Paper Award***

[6] Munafo, Robert; Shahzad,Hafsah et al (2023), "Improved Models for Policy-Agent Learning of Compiler Directives in HLS," *27th IEEE High Performance Extreme Computing Conference (HPEC)*.

[7] Shahzad, Hafsah, et.al (2022) "Reinforcement Learning Strategies for Compiler Optimization in High Level Synthesis", *8th Workshop on the LLVM Compiler Infrastructure in HPC- SC 2022 (LLVM-HPC)*.

[8] Shahzad, Hafsah, Ahmed Sanaullah, and Martin Herbordt (2021) "Survey and Future Trends for FPGA Cloud Architectures." *25th IEEE High Performance Extreme Computing Conference (HPEC)*.