# Digital Verification Diploma

Project_1_Synchronous FIFO

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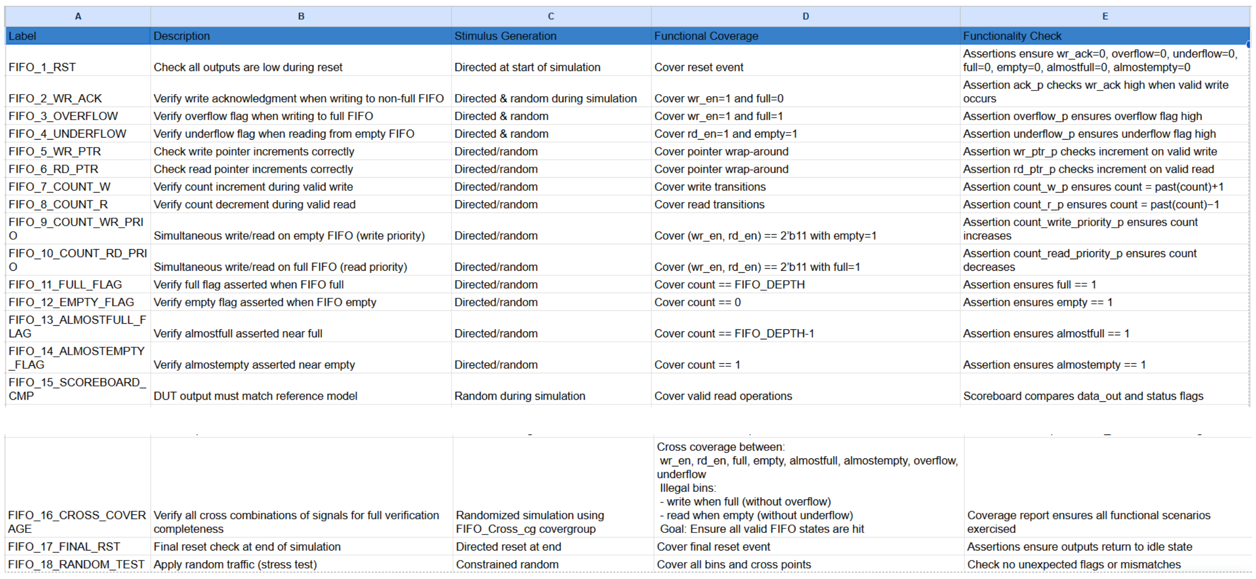
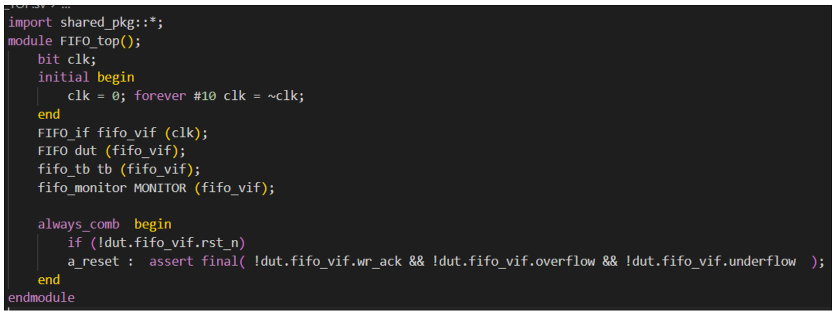
## Verification Plan



| A | B | C | D | E |
|---|---|---|---|---|
| Label | Description | Stimulus Generation | Functional Coverage | Functionality Check |
| FIFO_1_RST | Check all outputs are low during reset | Directed at start of simulation | Cover reset event | Assertions ensure wr_ack=0, overflow=0, underflow=0, full=0, empty=0, almostfull=0, almostempty=0 |
| FIFO_2_WR_ACK | Verify write acknowledgment when writing to non-full FIFO | Directed & random during simulation | Cover wr_en=1 and full=0 | Assertion ack_p checks wr_ack high when valid write occurs |
| FIFO_3_OVERFLOW | Verify overflow flag when writing to full FIFO | Directed & random | Cover wr_en=1 and full=1 | Assertion overflow_p ensures overflow flag high |
| FIFO_4_UNDERFLOW | Verify underflow flag when reading from empty FIFO | Directed & random | Cover rd_en=1 and empty=1 | Assertion underflow_p ensures underflow flag high |
| FIFO_5_WR_PTR | Check write pointer increments correctly | Directed/random | Cover pointer wrap-around | Assertion wr_ptr_p checks increment on valid write |
| FIFO_6_RD_PTR | Check read pointer increments correctly | Directed/random | Cover pointer wrap-around | Assertion rd_ptr_p checks increment on valid read |
| FIFO_7_COUNT_W | Verify count increment during valid write | Directed/random | Cover write transitions | Assertion count_w_p ensures count = past(count)+1 |
| FIFO_8_COUNT_R | Verify count decrement during valid read | Directed/random | Cover read transitions | Assertion count_r_p ensures count = past(count)−1 |
| FIFO_9_COUNT_WR_PRIO | Simultaneous write/read on empty FIFO (write priority) | Directed/random | Cover (wr_en, rd_en) == 2'b11 with empty=1 | Assertion count_write_priority_p ensures count increases |
| FIFO_10_COUNT_RD_PRIO | Simultaneous write/read on full FIFO (read priority) | Directed/random | Cover (wr_en, rd_en) == 2'b11 with full=1 | Assertion count_read_priority_p ensures count decreases |
| FIFO_11_FULL_FLAG | Verify full flag asserted when FIFO full | Directed/random | Cover count == FIFO_DEPTH | Assertion ensures full == 1 |
| FIFO_12_EMPTY_FLAG | Verify empty flag asserted when FIFO empty | Directed/random | Cover count == 0 | Assertion ensures empty == 1 |
| FIFO_13_ALMOSTFULL_FLAG | Verify almostfull asserted near full | Directed/random | Cover count == FIFO_DEPTH-1 | Assertion ensures almostfull == 1 |
| FIFO_14_ALMOSTEMPTY_FLAG | Verify almostempty asserted near empty | Directed/random | Cover count == 1 | Assertion ensures almostempty == 1 |
| FIFO_15_SCOREBOARD_CMP | DUT output must match reference model | Random during simulation | Cover valid read operations | Scoreboard compares data_out and status flags |
| FIFO_16_CROSS_COVERAGE | Verify all cross combinations of signals for full verification completeness | Randomized simulation using FIFO_Cross_cg covergroup | Cross coverage between: wr_en, rd_en, full, empty, almostfull, almostempty, overflow, underflow Illegal bins: - write when full (without overflow) - read when empty (without underflow) Goal: Ensure all valid FIFO states are hit | Coverage report ensures all functional scenarios exercised |
| FIFO_17_FINAL_RST | Final reset check at end of simulation | Directed reset at end | Cover final reset event | Assertions ensure outputs return to idle state |
| FIFO_18_RANDOM_TEST | Apply random traffic (stress test) | Constrained random | Cover all bins and cross points | Check no unexpected flags or mismatches |

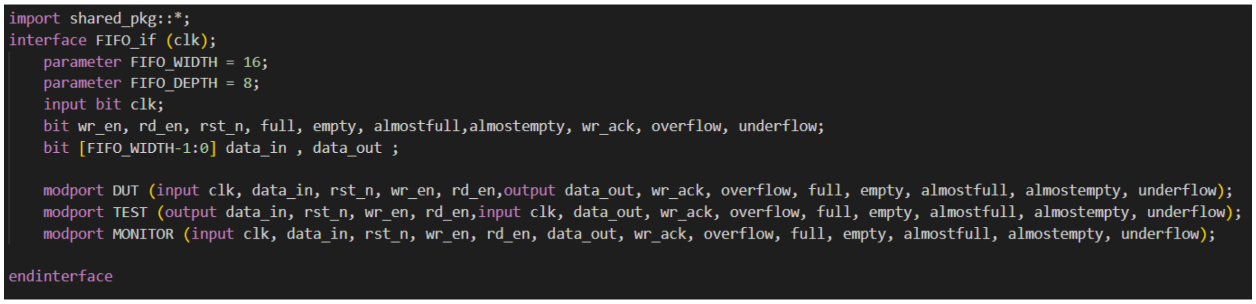
# Files code:

## Top File code



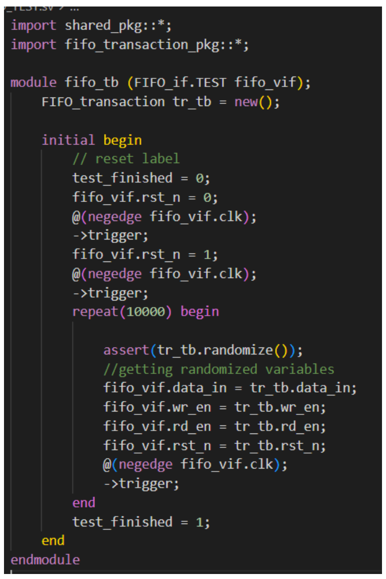
```
import shared_pkg::*;
module FIFO_top();
    bit clk;
    initial begin
        clk = 0; forever #10 clk = ~clk;
    end
    FIFO_if fifo_vif (clk);
    FIFO dut (fifo_vif);
    fifo_tb tb (fifo_vif);
    fifo_monitor MONITOR (fifo_vif);

    always_comb  begin
        if (!dut.fifo_vif.rst_n)
        a_reset :  assert final( !dut.fifo_vif.wr_ack && !dut.fifo_vif.overflow && !dut.fifo_vif.underflow  );
    end
endmodule
```

## Interface File code



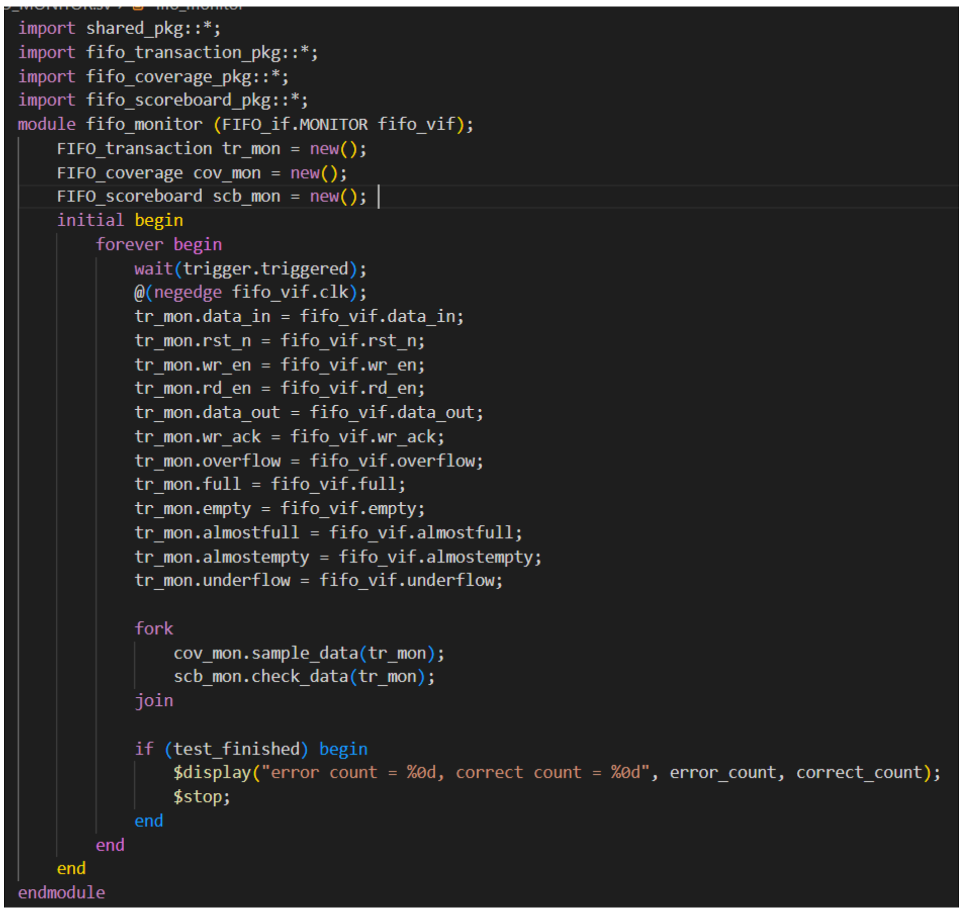
```
import shared_pkg::*;
interface FIFO_if (clk);
    parameter FIFO_WIDTH = 16;
    parameter FIFO_DEPTH = 8;
    input bit clk;
    bit wr_en, rd_en, rst_n, full, empty, almostfull,almostempty, wr_ack, overflow, underflow;
    bit [FIFO_WIDTH-1:0] data_in , data_out ;

    modport DUT (input clk, data_in, rst_n, wr_en, rd_en,output data_out, wr_ack, overflow, full, empty, almostfull, almostempty, underflow);
    modport TEST (output data_in, rst_n, wr_en, rd_en,input clk, data_out, wr_ack, overflow, full, empty, almostfull, almostempty, underflow);
    modport MONITOR (input clk, data_in, rst_n, wr_en, rd_en, data_out, wr_ack, overflow, full, empty, almostfull, almostempty, underflow);

endinterface
```

- ## Test File code



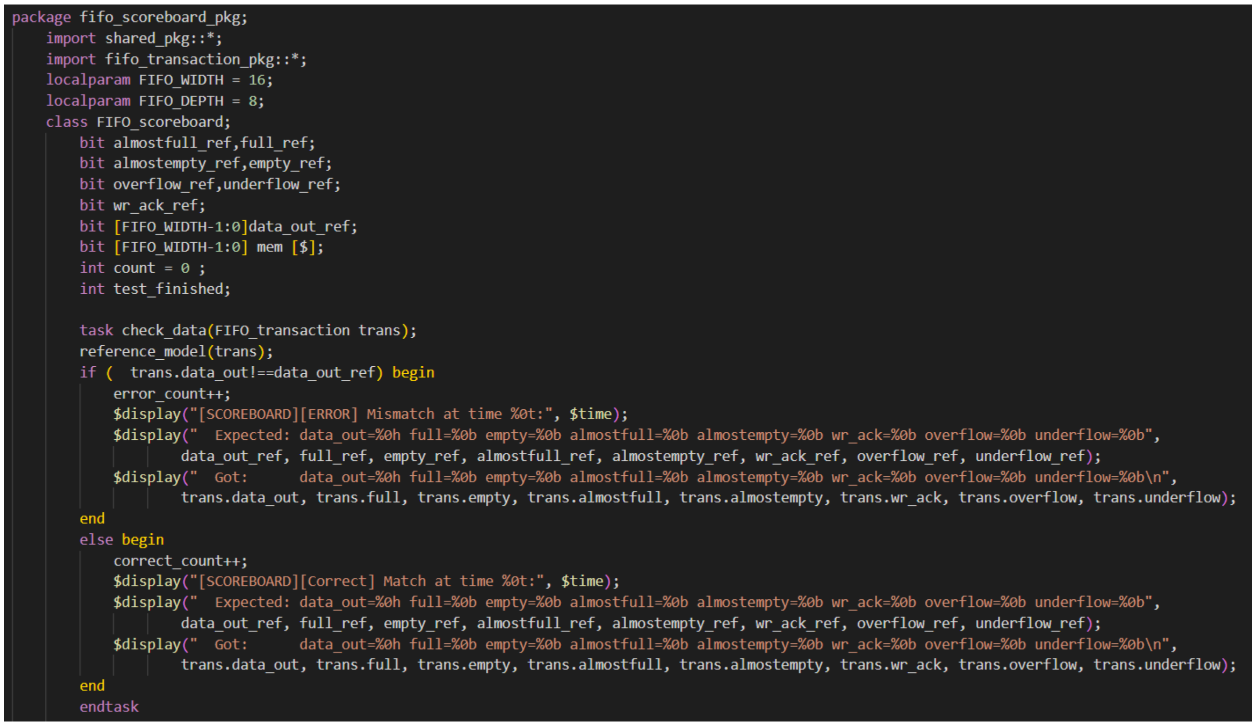
```
import shared_pkg::*;
import fifo_transaction_pkg::*;

module fifo_tb (FIFO_if.TEST fifo_vif);
    FIFO_transaction tr_tb = new();

    initial begin
        // reset label
        test_finished = 0;
        fifo_vif.rst_n = 0;
        @(negedge fifo_vif.clk);
        ->trigger;
        fifo_vif.rst_n = 1;
        @(negedge fifo_vif.clk);
        ->trigger;
        repeat(10000) begin

            assert(tr_tb.randomize());
            //getting randomized variables
            fifo_vif.data_in = tr_tb.data_in;
            fifo_vif.wr_en = tr_tb.wr_en;
            fifo_vif.rd_en = tr_tb.rd_en;
            fifo_vif.rst_n = tr_tb.rst_n;
            @(negedge fifo_vif.clk);
            ->trigger;
        end
        test_finished = 1;
    end
endmodule
```

- ## Monitor File code

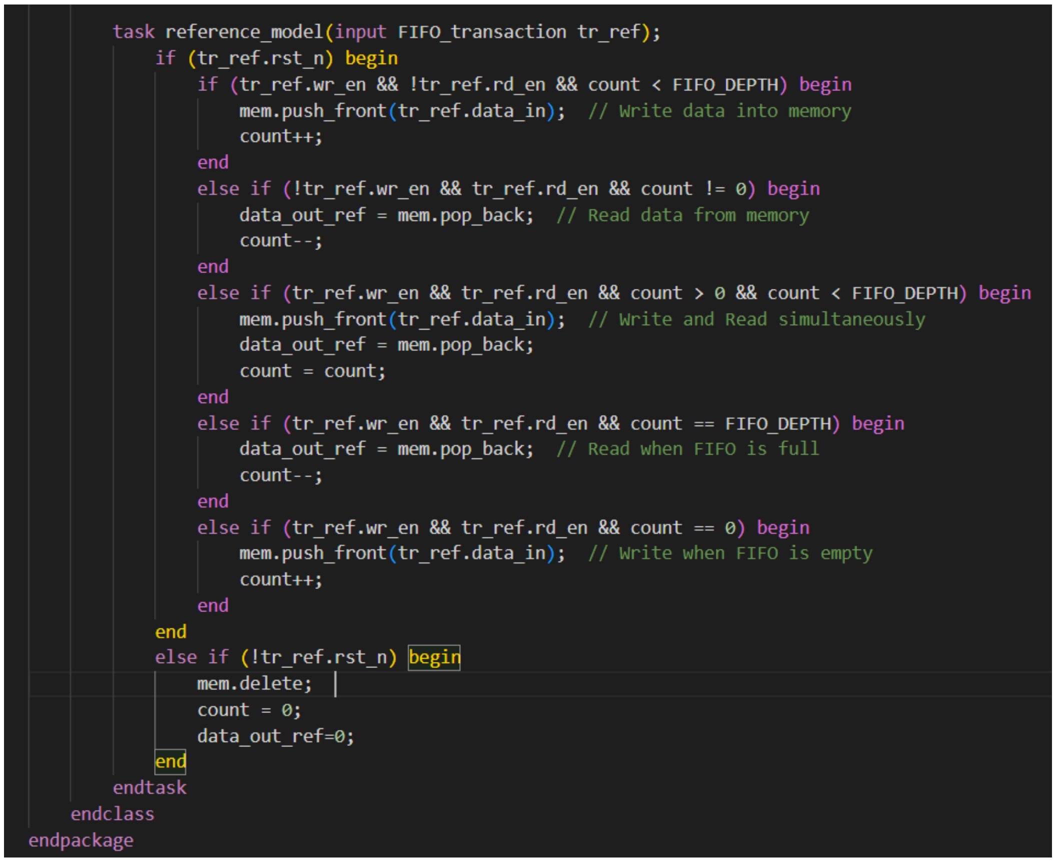


```
import shared_pkg::*;
import fifo_transaction_pkg::*;
import fifo_coverage_pkg::*;
import fifo_scoreboard_pkg::*;
module fifo_monitor (FIFO_if.MONITOR fifo_vif);
    FIFO_transaction tr_mon = new();
    FIFO_coverage cov_mon = new();
    FIFO_scoreboard scb_mon = new();
    initial begin
        forever begin
            wait(trigger.triggered);
            @(negedge fifo_vif.clk);
            tr_mon.data_in = fifo_vif.data_in;
            tr_mon.rst_n = fifo_vif.rst_n;
            tr_mon.wr_en = fifo_vif.wr_en;
            tr_mon.rd_en = fifo_vif.rd_en;
            tr_mon.data_out = fifo_vif.data_out;
            tr_mon.wr_ack = fifo_vif.wr_ack;
            tr_mon.overflow = fifo_vif.overflow;
            tr_mon.full = fifo_vif.full;
            tr_mon.empty = fifo_vif.empty;
            tr_mon.almostfull = fifo_vif.almostfull;
            tr_mon.almostempty = fifo_vif.almostempty;
            tr_mon.underflow = fifo_vif.underflow;

            fork
                cov_mon.sample_data(tr_mon);
                scb_mon.check_data(tr_mon);
            join

            if (test_finished) begin
                $display("error count = %0d, correct count = %0d", error_count, correct_count);
                $stop;
            end
        end
    end
endmodule
```

## Scoreboard File code

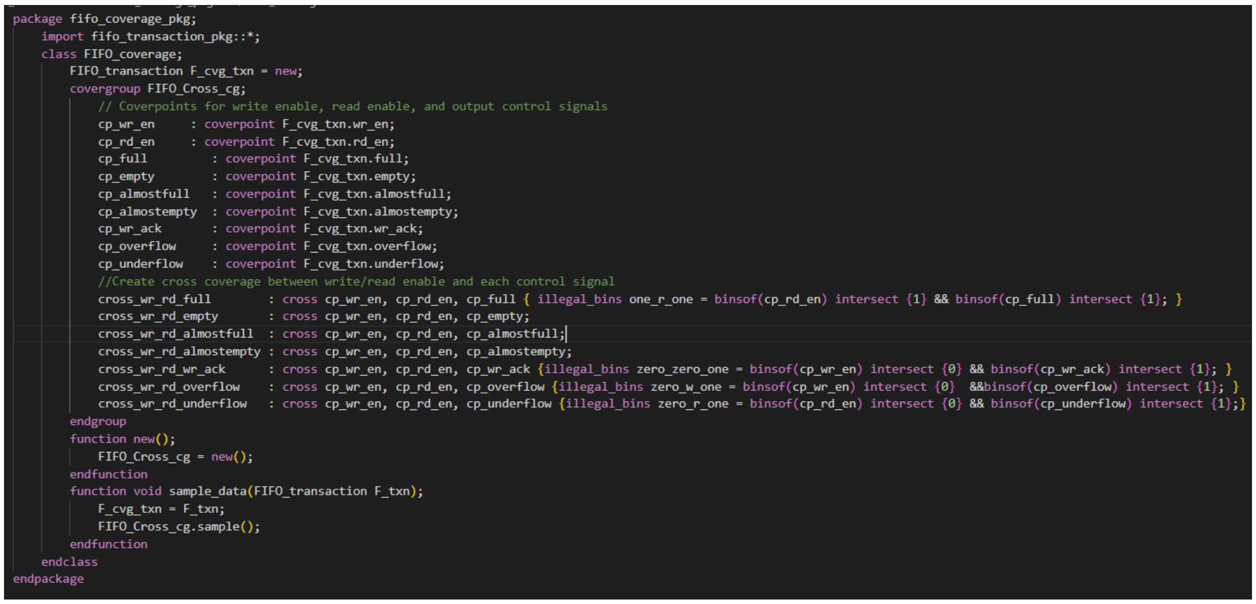


```systemverilog
package fifo_scoreboard_pkg;
    import shared_pkg::*;
    import fifo_transaction_pkg::*;
    localparam FIFO_WIDTH = 16;
    localparam FIFO_DEPTH = 8;
    class FIFO_scoreboard;
        bit almostfull_ref,full_ref;
        bit almostempty_ref,empty_ref;
        bit overflow_ref,underflow_ref;
        bit wr_ack_ref;
        bit [FIFO_WIDTH-1:0]data_out_ref;
        bit [FIFO_WIDTH-1:0] mem [$];
        int count = 0 ;
        int test_finished;

        task check_data(FIFO_transaction trans);
        reference_model(trans);
        if (  trans.data_out!==data_out_ref) begin
            error_count++;
            $display("[SCOREBOARD][ERROR] Mismatch at time %0t:", $time);
            $display("  Expected: data_out=%0h full=%0b empty=%0b almostfull=%0b almostempty=%0b wr_ack=%0b overflow=%0b underflow=%0b",
                    data_out_ref, full_ref, empty_ref, almostfull_ref, almostempty_ref, wr_ack_ref, overflow_ref, underflow_ref);
            $display("  Got:      data_out=%0h full=%0b empty=%0b almostfull=%0b almostempty=%0b wr_ack=%0b overflow=%0b underflow=%0b\n",
                    trans.data_out, trans.full, trans.empty, trans.almostfull, trans.almostempty, trans.wr_ack, trans.overflow, trans.underflow);
        end
        else begin
            correct_count++;
            $display("[SCOREBOARD][Correct] Match at time %0t:", $time);
            $display("  Expected: data_out=%0h full=%0b empty=%0b almostfull=%0b almostempty=%0b wr_ack=%0b overflow=%0b underflow=%0b",
                    data_out_ref, full_ref, empty_ref, almostfull_ref, almostempty_ref, wr_ack_ref, overflow_ref, underflow_ref);
            $display("  Got:      data_out=%0h full=%0b empty=%0b almostfull=%0b almostempty=%0b wr_ack=%0b overflow=%0b underflow=%0b\n",
                    trans.data_out, trans.full, trans.empty, trans.almostfull, trans.almostempty, trans.wr_ack, trans.overflow, trans.underflow);
        end
        endtask
```



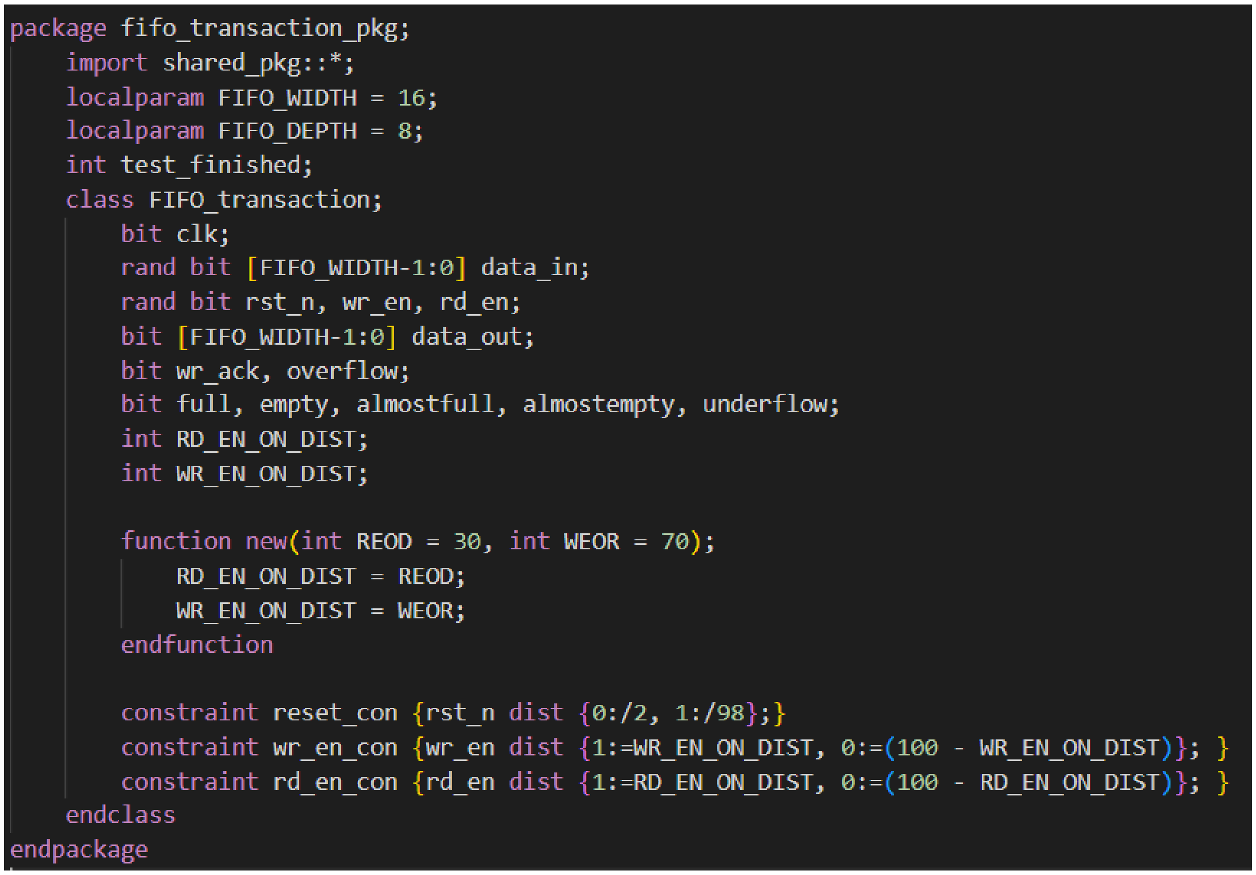
```systemverilog
        task reference_model(input FIFO_transaction tr_ref);
            if (tr_ref.rst_n) begin
                if (tr_ref.wr_en && !tr_ref.rd_en && count < FIFO_DEPTH) begin
                    mem.push_front(tr_ref.data_in);  // Write data into memory
                    count++;
                end
                else if (!tr_ref.wr_en && tr_ref.rd_en && count != 0) begin
                    data_out_ref = mem.pop_back;  // Read data from memory
                    count--;
                end
                else if (tr_ref.wr_en && tr_ref.rd_en && count > 0 && count < FIFO_DEPTH) begin
                    mem.push_front(tr_ref.data_in);  // Write and Read simultaneously
                    data_out_ref = mem.pop_back;
                    count = count;
                end
                else if (tr_ref.wr_en && tr_ref.rd_en && count == FIFO_DEPTH) begin
                    data_out_ref = mem.pop_back;  // Read when FIFO is full
                    count--;
                end
                else if (tr_ref.wr_en && tr_ref.rd_en && count == 0) begin
                    mem.push_front(tr_ref.data_in);  // Write when FIFO is empty
                    count++;
                end
            end
            else if (!tr_ref.rst_n) begin
                mem.delete;
                count = 0;
                data_out_ref=0;
            end
        endtask
    endclass
endpackage
```

## • Coverage File code



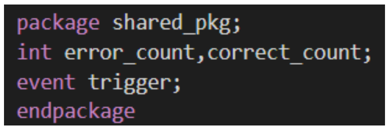
```
package fifo_coverage_pkg;
    import fifo_transaction_pkg::*;
    class FIFO_coverage;
        FIFO_transaction F_cvg_txn = new;
        covergroup FIFO_Cross_cg;
            // Coverpoints for write enable, read enable, and output control signals
            cp_wr_en      : coverpoint F_cvg_txn.wr_en;
            cp_rd_en      : coverpoint F_cvg_txn.rd_en;
            cp_full          : coverpoint F_cvg_txn.full;
            cp_empty         : coverpoint F_cvg_txn.empty;
            cp_almostfull    : coverpoint F_cvg_txn.almostfull;
            cp_almostempty   : coverpoint F_cvg_txn.almostempty;
            cp_wr_ack        : coverpoint F_cvg_txn.wr_ack;
            cp_overflow      : coverpoint F_cvg_txn.overflow;
            cp_underflow     : coverpoint F_cvg_txn.underflow;
            //Create cross coverage between write/read enable and each control signal
            cross_wr_rd_full        : cross cp_wr_en, cp_rd_en, cp_full { illegal_bins one_r_one = binsof(cp_rd_en) intersect {1} && binsof(cp_full) intersect {1}; }
            cross_wr_rd_empty       : cross cp_wr_en, cp_rd_en, cp_empty;
            cross_wr_rd_almostfull  : cross cp_wr_en, cp_rd_en, cp_almostfull;
            cross_wr_rd_almostempty : cross cp_wr_en, cp_rd_en, cp_almostempty;
            cross_wr_rd_wr_ack      : cross cp_wr_en, cp_rd_en, cp_wr_ack {illegal_bins zero_zero_one = binsof(cp_wr_en) intersect {0} && binsof(cp_wr_ack) intersect {1}; }
            cross_wr_rd_overflow    : cross cp_wr_en, cp_rd_en, cp_overflow {illegal_bins zero_w_one = binsof(cp_wr_en) intersect {0}  &&binsof(cp_overflow) intersect {1}; }
            cross_wr_rd_underflow   : cross cp_wr_en, cp_rd_en, cp_underflow {illegal_bins zero_r_one = binsof(cp_rd_en) intersect {0} && binsof(cp_underflow) intersect {1};}
        endgroup
        function new();
            FIFO_Cross_cg = new();
        endfunction
        function void sample_data(FIFO_transaction F_txn);
            F_cvg_txn = F_txn;
            FIFO_Cross_cg.sample();
        endfunction
    endclass
endpackage
```

## • Transaction File code



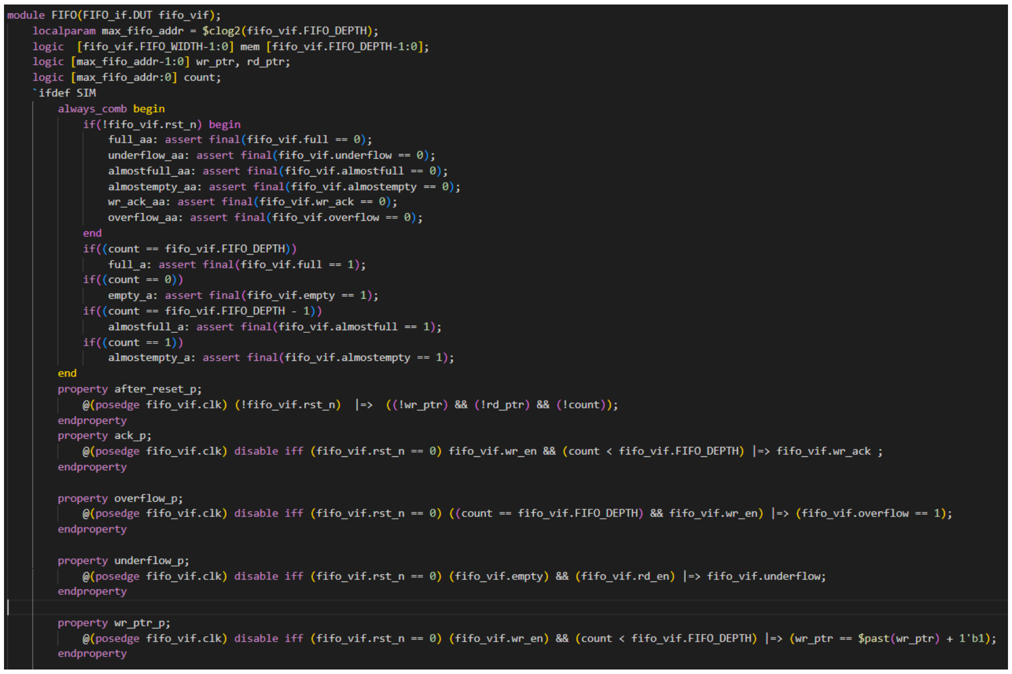
```
package fifo_transaction_pkg;
    import shared_pkg::*;
    localparam FIFO_WIDTH = 16;
    localparam FIFO_DEPTH = 8;
    int test_finished;
    class FIFO_transaction;
        bit clk;
        rand bit [FIFO_WIDTH-1:0] data_in;
        rand bit rst_n, wr_en, rd_en;
        bit [FIFO_WIDTH-1:0] data_out;
        bit wr_ack, overflow;
        bit full, empty, almostfull, almostempty, underflow;
        int RD_EN_ON_DIST;
        int WR_EN_ON_DIST;

        function new(int REOD = 30, int WEOR = 70);
            RD_EN_ON_DIST = REOD;
            WR_EN_ON_DIST = WEOR;
        endfunction

        constraint reset_con {rst_n dist {0:/2, 1:/98};}
        constraint wr_en_con {wr_en dist {1:=WR_EN_ON_DIST, 0:=(100 - WR_EN_ON_DIST)}; }
        constraint rd_en_con {rd_en dist {1:=RD_EN_ON_DIST, 0:=(100 - RD_EN_ON_DIST)}; }
    endclass
endpackage
```

## Shared_pkg File code

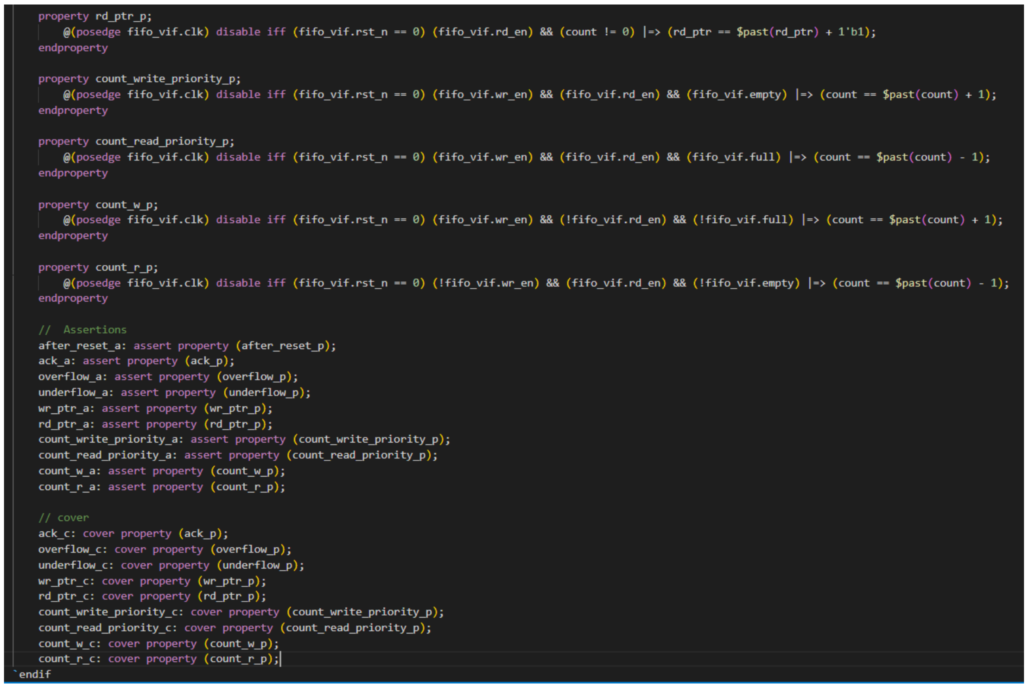


```
package shared_pkg;
int error_count,correct_count;
event trigger;
endpackage
```

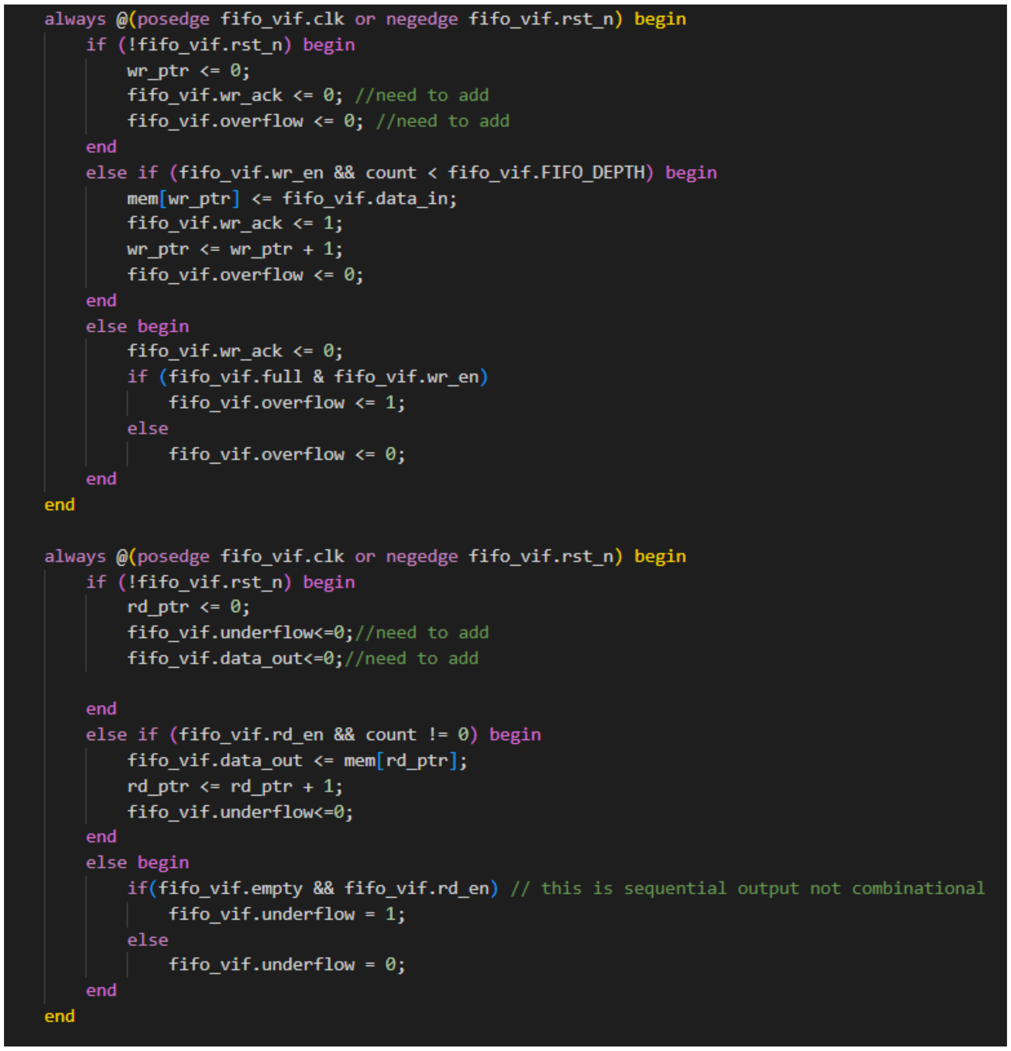
## Design & Assertion File code



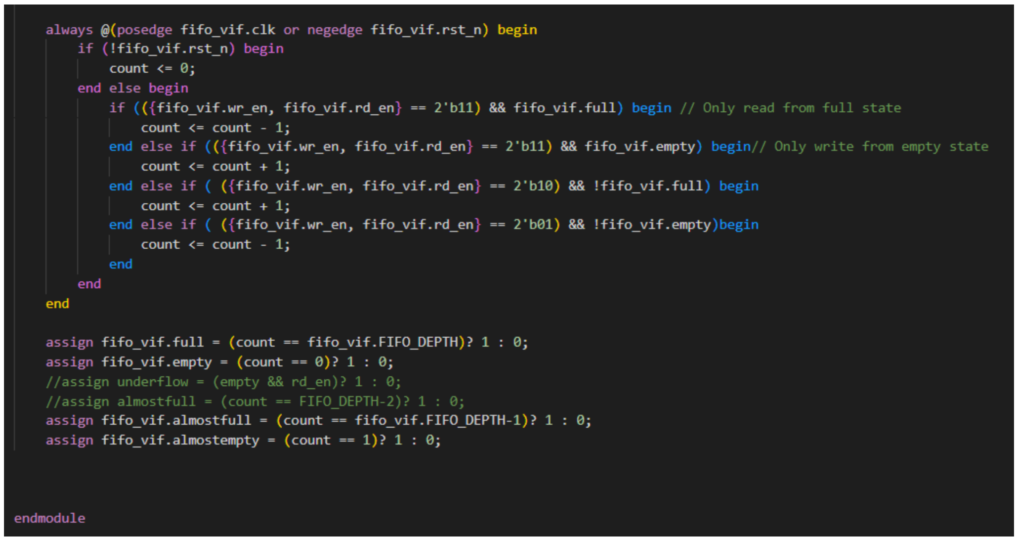
```
module FIFO(FIFO_if.DUT fifo_vif);
    localparam max_fifo_addr = $clog2(fifo_vif.FIFO_DEPTH);
    logic  [fifo_vif.FIFO_WIDTH-1:0] mem [fifo_vif.FIFO_DEPTH-1:0];
    logic [max_fifo_addr-1:0] wr_ptr, rd_ptr;
    logic [max_fifo_addr:0] count;
    `ifdef SIM
        always_comb begin
            if(!fifo_vif.rst_n) begin
                full_aa: assert final(fifo_vif.full == 0);
                underflow_aa: assert final(fifo_vif.underflow == 0);
                almostfull_aa: assert final(fifo_vif.almostfull == 0);
                almostempty_aa: assert final(fifo_vif.almostempty == 0);
                wr_ack_aa: assert final(fifo_vif.wr_ack == 0);
                overflow_aa: assert final(fifo_vif.overflow == 0);
            end
            if((count == fifo_vif.FIFO_DEPTH))
                full_a: assert final(fifo_vif.full == 1);
            if((count == 0))
                empty_a: assert final(fifo_vif.empty == 1);
            if((count == fifo_vif.FIFO_DEPTH - 1))
                almostfull_a: assert final(fifo_vif.almostfull == 1);
            if((count == 1))
                almostempty_a: assert final(fifo_vif.almostempty == 1);
        end
        property after_reset_p;
            @(posedge fifo_vif.clk) (!fifo_vif.rst_n)  |=>  ((!wr_ptr) && (!rd_ptr) && (!count));
        endproperty
        property ack_p;
            @(posedge fifo_vif.clk) disable iff (fifo_vif.rst_n == 0) fifo_vif.wr_en && (count < fifo_vif.FIFO_DEPTH) |=> fifo_vif.wr_ack ;
        endproperty

        property overflow_p;
            @(posedge fifo_vif.clk) disable iff (fifo_vif.rst_n == 0) ((count == fifo_vif.FIFO_DEPTH) && fifo_vif.wr_en) |=> (fifo_vif.overflow == 1);
        endproperty

        property underflow_p;
            @(posedge fifo_vif.clk) disable iff (fifo_vif.rst_n == 0) (fifo_vif.empty) && (fifo_vif.rd_en) |=> fifo_vif.underflow;
        endproperty

        property wr_ptr_p;
            @(posedge fifo_vif.clk) disable iff (fifo_vif.rst_n == 0) (fifo_vif.wr_en) && (count < fifo_vif.FIFO_DEPTH) |=> (wr_ptr == $past(wr_ptr) + 1'b1);
        endproperty
```



```
    property rd_ptr_p;
        @(posedge fifo_vif.clk) disable iff (fifo_vif.rst_n == 0) (fifo_vif.rd_en) && (count != 0) |=> (rd_ptr == $past(rd_ptr) + 1'b1);
    endproperty

    property count_write_priority_p;
        @(posedge fifo_vif.clk) disable iff (fifo_vif.rst_n == 0) (fifo_vif.wr_en) && (fifo_vif.rd_en) && (fifo_vif.empty) |=> (count == $past(count) + 1);
    endproperty

    property count_read_priority_p;
        @(posedge fifo_vif.clk) disable iff (fifo_vif.rst_n == 0) (fifo_vif.wr_en) && (fifo_vif.rd_en) && (fifo_vif.full) |=> (count == $past(count) - 1);
    endproperty

    property count_w_p;
        @(posedge fifo_vif.clk) disable iff (fifo_vif.rst_n == 0) (fifo_vif.wr_en) && (!fifo_vif.rd_en) && (!fifo_vif.full) |=> (count == $past(count) + 1);
    endproperty

    property count_r_p;
        @(posedge fifo_vif.clk) disable iff (fifo_vif.rst_n == 0) (!fifo_vif.wr_en) && (fifo_vif.rd_en) && (!fifo_vif.empty) |=> (count == $past(count) - 1);
    endproperty

    //  Assertions
    after_reset_a: assert property (after_reset_p);
    ack_a: assert property (ack_p);
    overflow_a: assert property (overflow_p);
    underflow_a: assert property (underflow_p);
    wr_ptr_a: assert property (wr_ptr_p);
    rd_ptr_a: assert property (rd_ptr_p);
    count_write_priority_a: assert property (count_write_priority_p);
    count_read_priority_a: assert property (count_read_priority_p);
    count_w_a: assert property (count_w_p);
    count_r_a: assert property (count_r_p);

    // cover
    ack_c: cover property (ack_p);
    overflow_c: cover property (overflow_p);
    underflow_c: cover property (underflow_p);
    wr_ptr_c: cover property (wr_ptr_p);
    rd_ptr_c: cover property (rd_ptr_p);
    count_write_priority_c: cover property (count_write_priority_p);
    count_read_priority_c: cover property (count_read_priority_p);
    count_w_c: cover property (count_w_p);
    count_r_c: cover property (count_r_p);
`endif
```



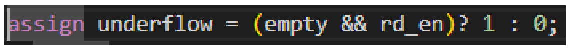
```
always @(posedge fifo_vif.clk or negedge fifo_vif.rst_n) begin
    if (!fifo_vif.rst_n) begin
        wr_ptr <= 0;
        fifo_vif.wr_ack <= 0; //need to add
        fifo_vif.overflow <= 0; //need to add
    end
    else if (fifo_vif.wr_en && count < fifo_vif.FIFO_DEPTH) begin
        mem[wr_ptr] <= fifo_vif.data_in;
        fifo_vif.wr_ack <= 1;
        wr_ptr <= wr_ptr + 1;
        fifo_vif.overflow <= 0;
    end
    else begin
        fifo_vif.wr_ack <= 0;
        if (fifo_vif.full & fifo_vif.wr_en)
            fifo_vif.overflow <= 1;
        else
            fifo_vif.overflow <= 0;
    end
end

always @(posedge fifo_vif.clk or negedge fifo_vif.rst_n) begin
    if (!fifo_vif.rst_n) begin
        rd_ptr <= 0;
        fifo_vif.underflow<=0;//need to add
        fifo_vif.data_out<=0;//need to add

    end
    else if (fifo_vif.rd_en && count != 0) begin
        fifo_vif.data_out <= mem[rd_ptr];
        rd_ptr <= rd_ptr + 1;
        fifo_vif.underflow<=0;
    end
    else begin
        if(fifo_vif.empty && fifo_vif.rd_en) // this is sequential output not combinational
            fifo_vif.underflow = 1;
        else
            fifo_vif.underflow = 0;
    end
end
```



```
    always @(posedge fifo_vif.clk or negedge fifo_vif.rst_n) begin
        if (!fifo_vif.rst_n) begin
            count <= 0;
        end else begin
            if (({fifo_vif.wr_en, fifo_vif.rd_en} == 2'b11) && fifo_vif.full) begin // Only read from full state
                count <= count - 1;
            end else if (({fifo_vif.wr_en, fifo_vif.rd_en} == 2'b11) && fifo_vif.empty) begin// Only write from empty state
                count <= count + 1;
            end else if ( ({fifo_vif.wr_en, fifo_vif.rd_en} == 2'b10) && !fifo_vif.full) begin
                count <= count + 1;
            end else if ( ({fifo_vif.wr_en, fifo_vif.rd_en} == 2'b01) && !fifo_vif.empty)begin
                count <= count - 1;
            end
        end
    end

    assign fifo_vif.full = (count == fifo_vif.FIFO_DEPTH)? 1 : 0;
    assign fifo_vif.empty = (count == 0)? 1 : 0;
    //assign underflow = (empty && rd_en)? 1 : 0;
    //assign almostfull = (count == FIFO_DEPTH-2)? 1 : 0;
    assign fifo_vif.almostfull = (count == fifo_vif.FIFO_DEPTH-1)? 1 : 0;
    assign fifo_vif.almostempty = (count == 1)? 1 : 0;



endmodule
```

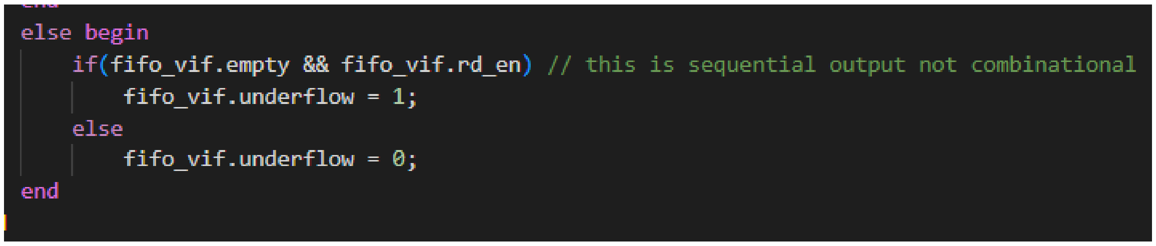
## Bugs Report:

### Bug_1: underflow signal was meant to be sequential



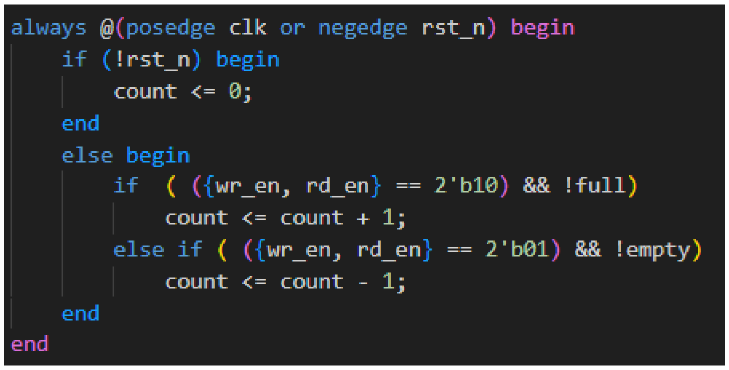
```
assign underflow = (empty && rd_en)? 1 : 0;
```

### Debug_1:



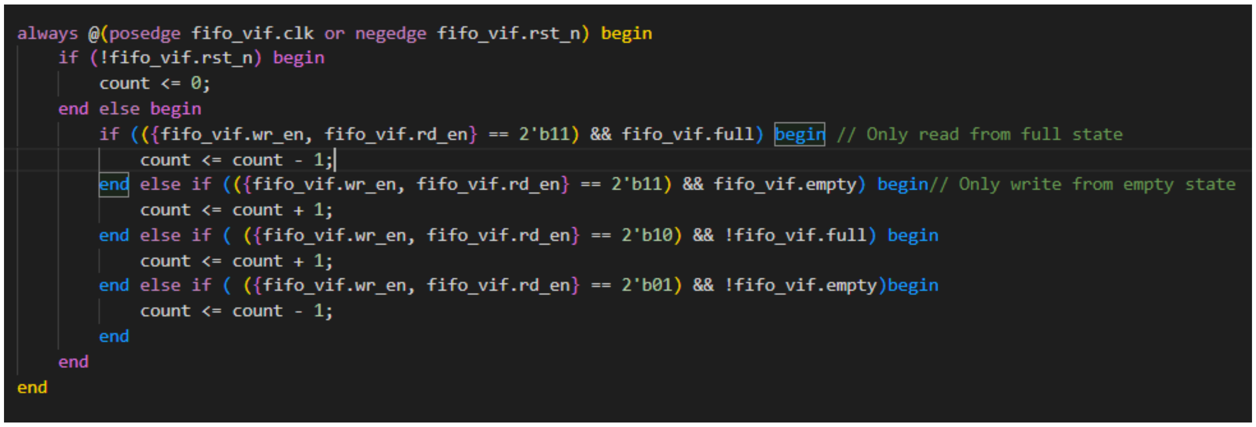
```
else begin
    if(fifo_vif.empty && fifo_vif.rd_en) // this is sequential output not combinational
        fifo_vif.underflow = 1;
    else
        fifo_vif.underflow = 0;
end
```

### Bug_2: Missing conditions



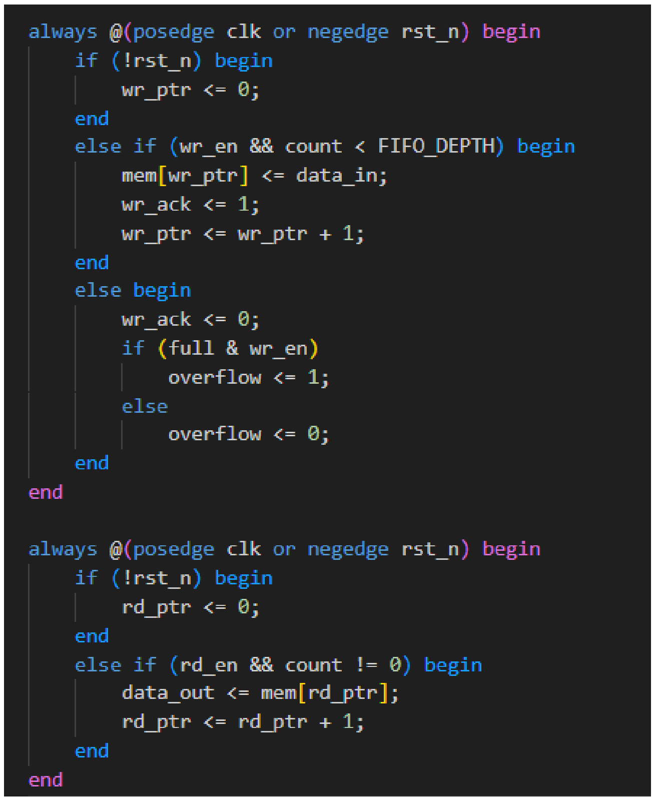
```
always @(posedge clk or negedge rst_n) begin
    if (!rst_n) begin
        count <= 0;
    end
    else begin
        if  ( ({wr_en, rd_en} == 2'b10) && !full)
            count <= count + 1;
        else if ( ({wr_en, rd_en} == 2'b01) && !empty)
            count <= count - 1;
    end
end
```

### Debug_2:



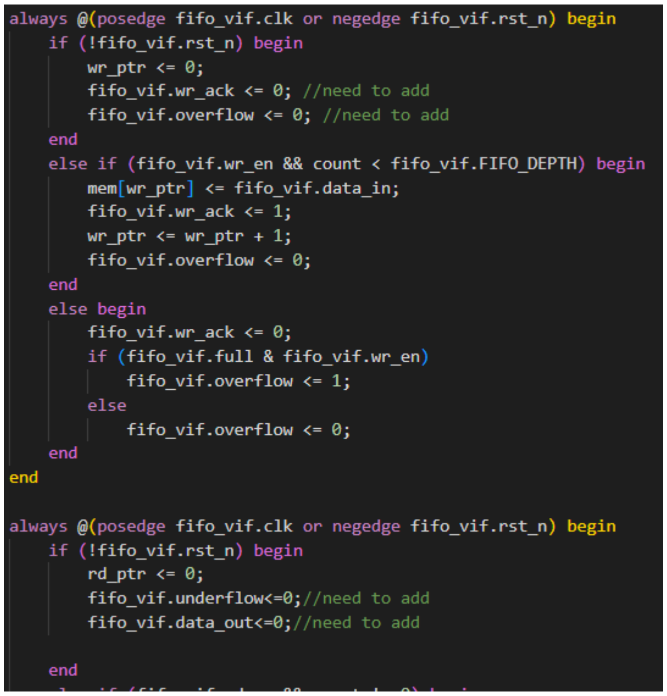
```
always @(posedge fifo_vif.clk or negedge fifo_vif.rst_n) begin
    if (!fifo_vif.rst_n) begin
        count <= 0;
    end else begin
        if (({fifo_vif.wr_en, fifo_vif.rd_en} == 2'b11) && fifo_vif.full) begin // Only read from full state
            count <= count - 1;
        end else if (({fifo_vif.wr_en, fifo_vif.rd_en} == 2'b11) && fifo_vif.empty) begin// Only write from empty state
            count <= count + 1;
        end else if ( ({fifo_vif.wr_en, fifo_vif.rd_en} == 2'b10) && !fifo_vif.full) begin
            count <= count + 1;
        end else if ( ({fifo_vif.wr_en, fifo_vif.rd_en} == 2'b01) && !fifo_vif.empty)begin
            count <= count - 1;
        end
    end
end
```

## Bug_3:Not Reset all  signals



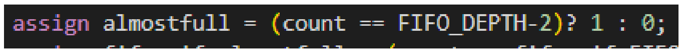
```
always @(posedge clk or negedge rst_n) begin
    if (!rst_n) begin
        wr_ptr <= 0;
    end
    else if (wr_en && count < FIFO_DEPTH) begin
        mem[wr_ptr] <= data_in;
        wr_ack <= 1;
        wr_ptr <= wr_ptr + 1;
    end
    else begin
        wr_ack <= 0;
        if (full & wr_en)
            overflow <= 1;
        else
            overflow <= 0;
    end
end

always @(posedge clk or negedge rst_n) begin
    if (!rst_n) begin
        rd_ptr <= 0;
    end
    else if (rd_en && count != 0) begin
        data_out <= mem[rd_ptr];
        rd_ptr <= rd_ptr + 1;
    end
end
```

## Debug_3:



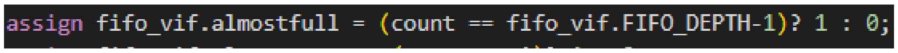
```
always @(posedge fifo_vif.clk or negedge fifo_vif.rst_n) begin
    if (!fifo_vif.rst_n) begin
        wr_ptr <= 0;
        fifo_vif.wr_ack <= 0; //need to add
        fifo_vif.overflow <= 0; //need to add
    end
    else if (fifo_vif.wr_en && count < fifo_vif.FIFO_DEPTH) begin
        mem[wr_ptr] <= fifo_vif.data_in;
        fifo_vif.wr_ack <= 1;
        wr_ptr <= wr_ptr + 1;
        fifo_vif.overflow <= 0;
    end
    else begin
        fifo_vif.wr_ack <= 0;
        if (fifo_vif.full & fifo_vif.wr_en)
            fifo_vif.overflow <= 1;
        else
            fifo_vif.overflow <= 0;
    end
end

always @(posedge fifo_vif.clk or negedge fifo_vif.rst_n) begin
    if (!fifo_vif.rst_n) begin
        rd_ptr <= 0;
        fifo_vif.underflow<=0;//need to add
        fifo_vif.data_out<=0;//need to add

    end
```

## Bug_4: Incorrect Almostfull Logic



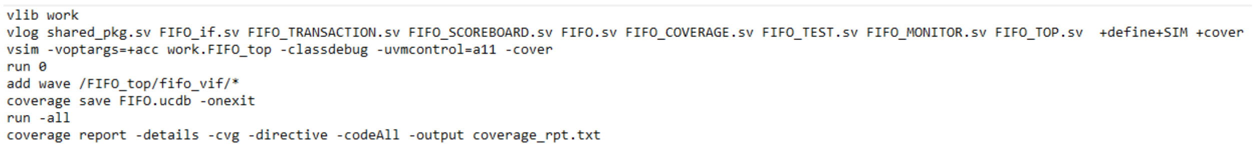
```
assign almostfull = (count == FIFO_DEPTH-2)? 1 : 0;
```

## Debug_4:



```
assign fifo_vif.almostfull = (count == fifo_vif.FIFO_DEPTH-1)? 1 : 0;
```

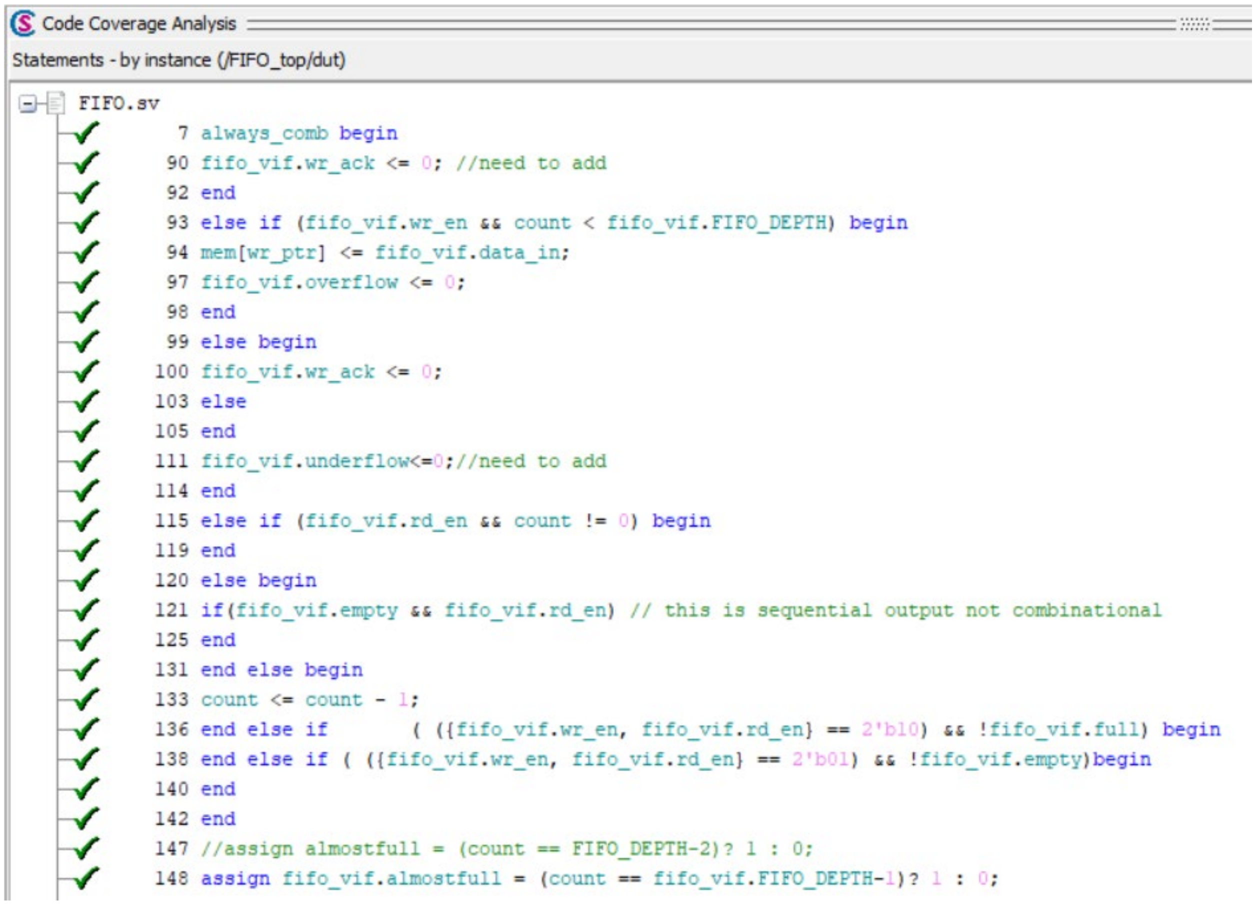
- ## Do file



```
vlib work
vlog shared_pkg.sv FIFO_if.sv FIFO_TRANSACTION.sv FIFO_SCOREBOARD.sv FIFO.sv FIFO_COVERAGE.sv FIFO_TEST.sv FIFO_MONITOR.sv FIFO_TOP.sv  +define+SIM +cover
vsim -voptargs=+acc work.FIFO_top -classdebug -uvmcontrol=a11 -cover
run 0
add wave /FIFO_top/fifo_vif/*
coverage save FIFO.ucdb -onexit
run -all
coverage report -details -cvg -directive -codeAll -output coverage_rpt.txt
```

- ## Coverage report text file

## Code Coverage :



Code Coverage Analysis

Statements - by instance (/FIFO_top/dut)

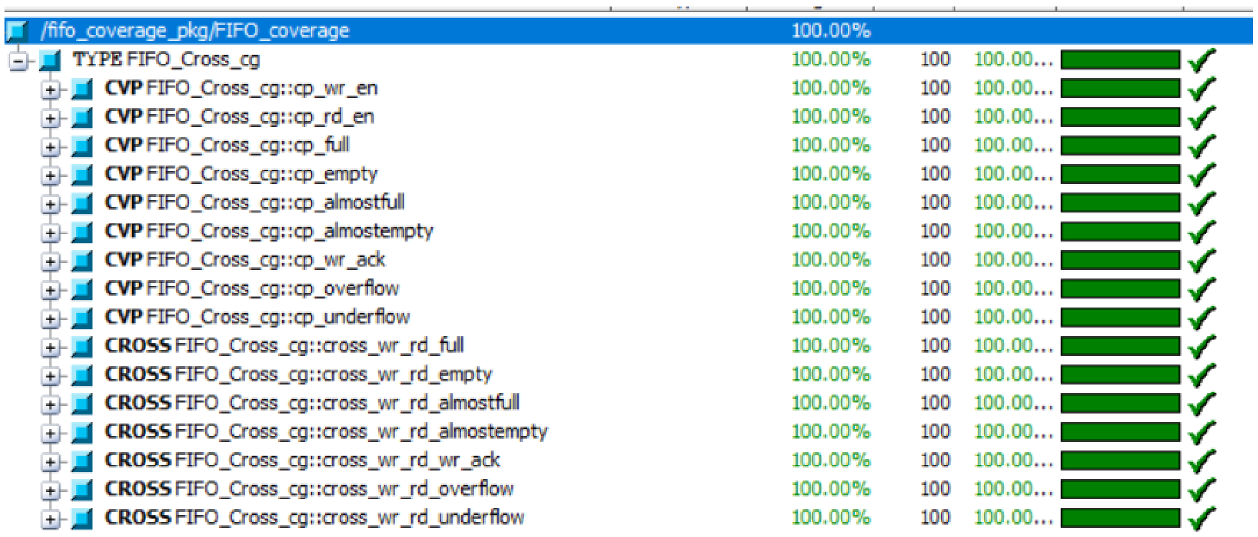
```
FIFO.sv
✓   7 always_comb begin
✓  90 fifo_vif.wr_ack <= 0; //need to add
✓  92 end
✓  93 else if (fifo_vif.wr_en && count < fifo_vif.FIFO_DEPTH) begin
✓  94 mem[wr_ptr] <= fifo_vif.data_in;
✓  97 fifo_vif.overflow <= 0;
✓  98 end
✓  99 else begin
✓ 100 fifo_vif.wr_ack <= 0;
✓ 103 else
✓ 105 end
✓ 111 fifo_vif.underflow<=0;//need to add
✓ 114 end
✓ 115 else if (fifo_vif.rd_en && count != 0) begin
✓ 119 end
✓ 120 else begin
✓ 121 if(fifo_vif.empty && fifo_vif.rd_en) // this is sequential output not combinational
✓ 125 end
✓ 131 end else begin
✓ 133 count <= count - 1;
✓ 136 end else if       ( ({fifo_vif.wr_en, fifo_vif.rd_en} == 2'b10) && !fifo_vif.full) begin
✓ 138 end else if ( ({fifo_vif.wr_en, fifo_vif.rd_en} == 2'b01) && !fifo_vif.empty)begin
✓ 140 end
✓ 142 end
✓ 147 //assign almostfull = (count == FIFO_DEPTH-2)? 1 : 0;
✓ 148 assign fifo_vif.almostfull = (count == fifo_vif.FIFO_DEPTH-1)? 1 : 0;
```

```
===============================================================================
=== Instance: /FIFO_top/dut
=== Design Unit: work.FIFO
===============================================================================
Branch Coverage:
    Enabled Coverage            Bins      Hits    Misses  Coverage
    ----------------            ----      ----    ------  --------
    Branches                      35        35         0   100.00%

================================Branch Details================================

Branch Coverage for instance /FIFO_top/dut

    Line         Item                      Count     Source 
    ----         ----                      -----     ------ 
  File FIFO.sv
------------------------------------IF Branch------------------------------------
    8                                       8433     Count coming in to IF
    8              1                         411     
                                            8022     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    16                                      8433     Count coming in to IF
    16             1                        2954     
                                            5479     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    18                                      8433     Count coming in to IF
    18             1                         569     
                                            7864     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    20                                      8433     Count coming in to IF
    20             1                        2291     
                                            6142     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    22                                      8433     Count coming in to IF
    22             1                         454     
                                            7979     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    91                                     10208     Count coming in to IF
    91             1                         415     
    96             1                        4162     
    102            1                        5631     
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    104                                     5631     Count coming in to IF
    104            1                        2641     
    106            1                        2990     
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    112                                    10208     Count coming in to IF
    112            1                         415     
    118            1                        2885     
    123            1                        6908     
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    124                                     6908     Count coming in to IF
    124            1                         110     
    126            1                        6798     
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    132                                     8667     Count coming in to IF
    132            1                         414     
```

```
   134          1                  8253
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
   135                            8253    Count coming in to IF
   135          1                  812
   137          1                   74
   139          1                 2899
   141          1                  884
                               3584    All False Count
Branch totals: 5 hits of 5 branches = 100.00%

------------------------------------IF Branch------------------------------------
   147                            4874    Count coming in to IF
   147          1                 1259
   147          2                 3615
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
   148                            4874    Count coming in to IF
   148          1                  238
   148          2                 4636
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
   151                            4874    Count coming in to IF
   151          1                 1557
   151          2                 3317
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
   152                            4874    Count coming in to IF
   152          1                  276
   152          2                 4598
Branch totals: 2 hits of 2 branches = 100.00%
Condition Coverage:
   Enabled Coverage           Bins   Covered    Misses  Coverage
   ----------------           ----     ----    ------  --------
   Conditions                  28       27       1   96.42%

================================Condition Details================================

Condition Coverage for instance /FIFO_top/dut --

  File FIFO.sv
----------------Focused Condition View-------------------
Line      16 Item    1  (count == fifo_vif.FIFO_DEPTH)
Condition totals: 1 of 1 input term covered = 100.00%

----------------Focused Condition View-------------------
Line      18 Item    1  (count == 0)
Condition totals: 1 of 1 input term covered = 100.00%

----------------Focused Condition View-------------------
Line      20 Item    1  (count == (fifo_vif.FIFO_DEPTH - 1))
Condition totals: 1 of 1 input term covered = 100.00%

----------------Focused Condition View-------------------
Line      22 Item    1  (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%

----------------Focused Condition View-------------------
Line      96 Item    1  (fifo_vif.wr_en && (count < fifo_vif.FIFO_DEPTH))
Condition totals: 2 of 2 input terms covered = 100.00%

----------------Focused Condition View-------------------
Line      104 Item    1  (fifo_vif.full & fifo_vif.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%

     Input Term   Covered  Reason for no coverage   Hint
    -----------  --------  -----------------------  --------------
   fifo_vif.full        N  '_0' not hit             Hit '_0'
  fifo_vif.wr_en        Y

    Rows:       Hits  FEC Target            Non-masking condition(s)
```

```
 --------- --------- -------------------- -------------------------
  Row   1:    ***0***  fifo_vif.full_0       fifo_vif.wr_en
  Row   2:          1  fifo_vif.full_1       fifo_vif.wr_en
  Row   3:          1  fifo_vif.wr_en_0      fifo_vif.full
  Row   4:          1  fifo_vif.wr_en_1      fifo_vif.full

----------------Focused Condition View-------------------
Line       118 Item    1  (fifo_vif.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%

----------------Focused Condition View-------------------
Line       124 Item    1  (fifo_vif.empty && fifo_vif.rd_en)
Condition totals: 2 of 2 input terms covered = 100.00%

----------------Focused Condition View-------------------
Line       135 Item    1  ((fifo_vif.rd_en && fifo_vif.wr_en) && fifo_vif.full)
Condition totals: 3 of 3 input terms covered = 100.00%

----------------Focused Condition View-------------------
Line       137 Item    1  ((fifo_vif.rd_en && fifo_vif.wr_en) && fifo_vif.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

----------------Focused Condition View-------------------
Line       139 Item    1  ((~fifo_vif.rd_en && fifo_vif.wr_en) && ~fifo_vif.full)
Condition totals: 3 of 3 input terms covered = 100.00%

----------------Focused Condition View-------------------
Line       141 Item    1  ((fifo_vif.rd_en && ~fifo_vif.wr_en) && ~fifo_vif.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

----------------Focused Condition View-------------------
Line       147 Item    1  (count == fifo_vif.FIFO_DEPTH)
Condition totals: 1 of 1 input term covered = 100.00%

----------------Focused Condition View-------------------
Line       148 Item    1  (count == 0)
Condition totals: 1 of 1 input term covered = 100.00%

----------------Focused Condition View-------------------
Line       151 Item    1  (count == (fifo_vif.FIFO_DEPTH - 1))
Condition totals: 1 of 1 input term covered = 100.00%

----------------Focused Condition View-------------------
Line       152 Item    1  (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%

Directive Coverage:
    Directives                      9         9         0   100.00%

DIRECTIVE COVERAGE:
--------------------------------------------------------------------------------------------
Name                                Design Design   Lang File(Line)      Hits Status
                                    Unit   UnitType
--------------------------------------------------------------------------------------------
/FIFO_top/dut/ack_c                 FIFO   Verilog  SVA  FIFO.sv(79)     4068 Covered
/FIFO_top/dut/overflow_c            FIFO   Verilog  SVA  FIFO.sv(80)     2587 Covered
/FIFO_top/dut/underflow_c           FIFO   Verilog  SVA  FIFO.sv(81)      108 Covered
/FIFO_top/dut/wr_ptr_c              FIFO   Verilog  SVA  FIFO.sv(82)     4068 Covered
/FIFO_top/dut/rd_ptr_c              FIFO   Verilog  SVA  FIFO.sv(83)     2822 Covered
/FIFO_top/dut/count_write_priority_c FIFO  Verilog  SVA  FIFO.sv(84)       72 Covered
/FIFO_top/dut/count_read_priority_c FIFO   Verilog  SVA  FIFO.sv(85)      797 Covered
/FIFO_top/dut/count_w_c             FIFO   Verilog  SVA  FIFO.sv(86)     2838 Covered
/FIFO_top/dut/count_r_c             FIFO   Verilog  SVA  FIFO.sv(87)      867 Covered
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      31        31         0   100.00%

================================Statement Details================================

Statement Coverage for instance /FIFO_top/dut --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File FIFO.sv
  7        1          8433
  90       1          10208
  92       1           415
  93       1           415
  94       1           415
  97       1          4162
  98       1          4162
  99       1          4162
  100      1          4162
  103      1          5631
  105      1          2641
  107      1          2990
  111      1          10208
  113      1           415
  114      1           415
  115      1           415
  119      1          2885
  120      1          2885
  121      1          2885
  125      1           110
  127      1          6798
  131      1          8667
  133      1           414
  136      1           812
  138      1            74
  140      1          2899
  142      1           884
  147      1          4875
  148      1          4875
  151      1          4875
  152      1          4875
Toggle Coverage:
  Enabled Coverage          Bins    Hits   Misses  Coverage
  ----------------          ----    ----   ------  --------
  Toggles                     20      20        0   100.00%
================================Toggle Details================================
Toggle Coverage for instance /FIFO_top/dut --
                         Node      1H->0L     0L->1H  "Coverage"
                         ---------------------------------------

Total Node Count     =        10
Toggled Node Count   =        10
Untoggled Node Count =         0

Toggle Coverage      =     100.00% (20 of 20 bins)
```

## Functional Coverage :



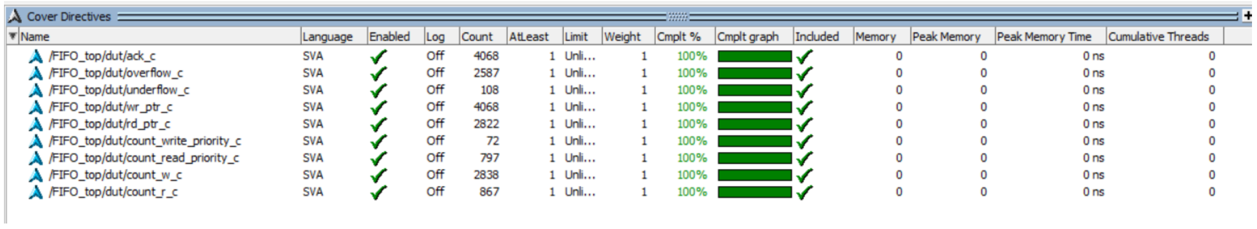
| | | | | | |
|---|---|---|---|---|---|
| /fifo_coverage_pkg/FIFO_coverage | 100.00% | | | | |
| TYPE FIFO_Cross_cg | 100.00% | 100 | 100.00... | 🟩 | ✓ |
| CVP FIFO_Cross_cg::cp_wr_en | 100.00% | 100 | 100.00... | 🟩 | ✓ |
| CVP FIFO_Cross_cg::cp_rd_en | 100.00% | 100 | 100.00... | 🟩 | ✓ |
| CVP FIFO_Cross_cg::cp_full | 100.00% | 100 | 100.00... | 🟩 | ✓ |
| CVP FIFO_Cross_cg::cp_empty | 100.00% | 100 | 100.00... | 🟩 | ✓ |
| CVP FIFO_Cross_cg::cp_almostfull | 100.00% | 100 | 100.00... | 🟩 | ✓ |
| CVP FIFO_Cross_cg::cp_almostempty | 100.00% | 100 | 100.00... | 🟩 | ✓ |
| CVP FIFO_Cross_cg::cp_wr_ack | 100.00% | 100 | 100.00... | 🟩 | ✓ |
| CVP FIFO_Cross_cg::cp_overflow | 100.00% | 100 | 100.00... | 🟩 | ✓ |
| CVP FIFO_Cross_cg::cp_underflow | 100.00% | 100 | 100.00... | 🟩 | ✓ |
| CROSS FIFO_Cross_cg::cross_wr_rd_full | 100.00% | 100 | 100.00... | 🟩 | ✓ |
| CROSS FIFO_Cross_cg::cross_wr_rd_empty | 100.00% | 100 | 100.00... | 🟩 | ✓ |
| CROSS FIFO_Cross_cg::cross_wr_rd_almostfull | 100.00% | 100 | 100.00... | 🟩 | ✓ |
| CROSS FIFO_Cross_cg::cross_wr_rd_almostempty | 100.00% | 100 | 100.00... | 🟩 | ✓ |
| CROSS FIFO_Cross_cg::cross_wr_rd_wr_ack | 100.00% | 100 | 100.00... | 🟩 | ✓ |
| CROSS FIFO_Cross_cg::cross_wr_rd_overflow | 100.00% | 100 | 100.00... | 🟩 | ✓ |
| CROSS FIFO_Cross_cg::cross_wr_rd_underflow | 100.00% | 100 | 100.00... | 🟩 | ✓ |

```
=== Instance: /fifo_coverage_pkg
=== Design Unit: work.fifo_coverage_pkg
==========================================================================
Covergroup Coverage:
  Covergroups              1      na      na   100.00%
    Coverpoints/Crosses       16      na      na      na
      Covergroup Bins       66      66       0   100.00%
----------------------------------------------------------------------------------------------------
Covergroup                              Metric      Goal      Bins    Status
----------------------------------------------------------------------------------------------------
 TYPE /fifo_coverage_pkg/FIFO_coverage/FIFO_Cross_cg
                                   100.00%       100        -    Covered
  covered/total bins:                        66       66        -
  missing/total bins:                         0       66        -
  % Hit:                           100.00%       100        -
  Coverpoint cp_wr_en                        100.00%       100        -    Covered
    covered/total bins:                       2        2        -
    missing/total bins:                       0        2        -
    % Hit:                         100.00%       100        -
    bin auto[0]                         3052        1        -    Covered
    bin auto[1]                         6950        1        -    Covered
  Coverpoint cp_rd_en                        100.00%       100        -    Covered
    covered/total bins:                       2        2        -
    missing/total bins:                       0        2        -
    % Hit:                         100.00%       100        -
    bin auto[0]                         6955        1        -    Covered
    bin auto[1]                         3047        1        -    Covered
  Coverpoint cp_full                       100.00%       100        -    Covered
    covered/total bins:                       2        2        -
    missing/total bins:                       0        2        -
    % Hit:                         100.00%       100        -
    bin auto[0]                         6103        1        -    Covered
    bin auto[1]                         3899        1        -    Covered
  Coverpoint cp_empty                        100.00%       100        -    Covered
    covered/total bins:                       2        2        -
    missing/total bins:                       0        2        -
    % Hit:                         100.00%       100        -
    bin auto[0]                         9646        1        -    Covered
    bin auto[1]                          356        1        -    Covered
  Coverpoint cp_almostfull                     100.00%       100        -    Covered
    covered/total bins:                       2        2        -
    missing/total bins:                       0        2        -
    % Hit:                         100.00%       100        -
    bin auto[0]                         7418        1        -    Covered
    bin auto[1]                         2584        1        -    Covered
  Coverpoint cp_almostempty                     100.00%       100        -    Covered
    covered/total bins:                       2        2        -
    missing/total bins:                       0        2        -
    % Hit:                         100.00%       100        -
    bin auto[0]                         9524        1        -    Covered
    bin auto[1]                          478        1        -    Covered
  Coverpoint cp_wr_ack                       100.00%       100        -    Covered
    covered/total bins:                       2        2        -
    missing/total bins:                       0        2        -
    % Hit:                         100.00%       100        -
    bin auto[0]                         5840        1        -    Covered
    bin auto[1]                         4162        1        -    Covered
  Coverpoint cp_overflow                      100.00%       100        -    Covered
    covered/total bins:                       2        2        -
    missing/total bins:                       0        2        -
    % Hit:                         100.00%       100        -
    bin auto[0]                         7361        1        -    Covered
    bin auto[1]                         2641        1        -    Covered
  Coverpoint cp_underflow                      100.00%       100        -    Covered
    covered/total bins:                       2        2        -
    missing/total bins:                       0        2        -
    % Hit:                         100.00%       100        -
    bin auto[0]                         9892        1        -    Covered
    bin auto[1]                          110        1        -    Covered
  Cross cross_wr_rd_full                     100.00%       100        -    Covered
    covered/total bins:                       6        6        -
    missing/total bins:                       0        6        -
    % Hit:                         100.00%       100        -
    Auto, Default and User Defined Bins:
      bin <auto[1],auto[1],auto[0]>            2111        1        -    Covered
```

```
        bin <auto[0],auto[1],auto[0]>          936       1       -   Covered
        bin <auto[1],auto[0],auto[1]>          3088       1       -   Covered
        bin <auto[1],auto[0],auto[0]>          1751       1       -   Covered
        bin <auto[0],auto[0],auto[1]>          811       1       -   Covered
        bin <auto[0],auto[0],auto[0]>          1305       1       -   Covered
      Illegal and Ignore Bins:
        illegal_bin one_r_one                  0              -   ZERO
    Cross cross_wr_rd_empty                  100.00%      100       -   Covered
      covered/total bins:                    8       8       -
      missing/total bins:                    0       8       -
      % Hit:                          100.00%      100       -
      Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>          36       1       -   Covered
        bin <auto[0],auto[1],auto[1]>          85       1       -   Covered
        bin <auto[1],auto[0],auto[1]>          111       1       -   Covered
        bin <auto[0],auto[0],auto[1]>          124       1       -   Covered
        bin <auto[1],auto[1],auto[0]>          2075       1       -   Covered
        bin <auto[0],auto[1],auto[0]>          851       1       -   Covered
        bin <auto[1],auto[0],auto[0]>          4728       1       -   Covered
        bin <auto[0],auto[0],auto[0]>          1992       1       -   Covered
    Cross cross_wr_rd_almostfull              100.00%      100       -   Covered
      covered/total bins:                    8       8       -
      missing/total bins:                    0       8       -
      % Hit:                          100.00%      100       -
      Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>          1328       1       -   Covered
        bin <auto[0],auto[1],auto[1]>          359       1       -   Covered
        bin <auto[1],auto[0],auto[1]>          386       1       -   Covered
        bin <auto[0],auto[0],auto[1]>          511       1       -   Covered
        bin <auto[1],auto[1],auto[0]>          783       1       -   Covered
        bin <auto[0],auto[1],auto[0]>          577       1       -   Covered
        bin <auto[1],auto[0],auto[0]>          4453       1       -   Covered
        bin <auto[0],auto[0],auto[0]>          1605       1       -   Covered
    Cross cross_wr_rd_almostempty              100.00%      100       -   Covered
      covered/total bins:                    8       8       -
      missing/total bins:                    0       8       -
      % Hit:                          100.00%      100       -
      Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>          177       1       -   Covered
        bin <auto[0],auto[1],auto[1]>          38       1       -   Covered
        bin <auto[1],auto[0],auto[1]>          164       1       -   Covered
        bin <auto[0],auto[0],auto[1]>          99       1       -   Covered
        bin <auto[1],auto[1],auto[0]>          1934       1       -   Covered
        bin <auto[0],auto[1],auto[0]>          898       1       -   Covered
        bin <auto[1],auto[0],auto[0]>          4675       1       -   Covered
        bin <auto[0],auto[0],auto[0]>          2017       1       -   Covered
    Cross cross_wr_rd_wr_ack                 100.00%      100       -   Covered
      covered/total bins:                    6       6       -
      missing/total bins:                    0       6       -
      % Hit:                          100.00%      100       -
      Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>          1263       1       -   Covered
        bin <auto[1],auto[0],auto[1]>          2899       1       -   Covered
        bin <auto[1],auto[1],auto[0]>          848       1       -   Covered
        bin <auto[0],auto[1],auto[0]>          936       1       -   Covered
        bin <auto[1],auto[0],auto[0]>          1940       1       -   Covered
        bin <auto[0],auto[0],auto[0]>          2116       1       -   Covered
      Illegal and Ignore Bins:
        illegal_bin zero_zero_one              0              -   ZERO
    Cross cross_wr_rd_overflow               100.00%      100       -   Covered
      covered/total bins:                    6       6       -
      missing/total bins:                    0       6       -
      % Hit:                          100.00%      100       -
      Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>          812       1       -   Covered
        bin <auto[1],auto[0],auto[1]>          1829       1       -   Covered
        bin <auto[1],auto[1],auto[0]>          1299       1       -   Covered
        bin <auto[0],auto[1],auto[0]>          936       1       -   Covered
        bin <auto[1],auto[0],auto[0]>          3010       1       -   Covered
        bin <auto[0],auto[0],auto[0]>          2116       1       -   Covered
      Illegal and Ignore Bins:
        illegal_bin zero_w_one                 0              -   ZERO
    Cross cross_wr_rd_underflow              100.00%      100       -   Covered
      covered/total bins:                    6       6       -
      missing/total bins:                    0       6       -
    % Hit:                          100.00%      100       -
    Auto, Default and User Defined Bins:
      bin <auto[1],auto[1],auto[1]>            74       1       -   Covered
      bin <auto[1],auto[1],auto[0]>           2037       1       -   Covered
      bin <auto[0],auto[1],auto[1]>            36       1       -   Covered
      bin <auto[0],auto[1],auto[0]>            900       1       -   Covered
      bin <auto[1],auto[0],auto[0]>           4839       1       -   Covered
      bin <auto[0],auto[0],auto[0]>           2116       1       -   Covered
    Illegal and Ignore Bins:
      illegal_bin zero_r_one                   0               -   ZERO
Statement Coverage:
  Enabled Coverage          Bins     Hits   Misses  Coverage
  ----------------          ----     ----   ------  --------
  Statements                   4       4       0  100.00%
================================Statement Details================================
Statement Coverage for instance /fifo_coverage_pkg --
  Line       Item                 Count    Source
  ----       ----                 -----    ------
 File FIFO_COVERAGE.sv
  4           1                   1
  26          1                   1
  29          1                10002
  30          1                10002
COVERGROUP COVERAGE:
---------------------------------------------------------------------------------------------------------
Covergroup                              Metric      Goal      Bins   Status
---------------------------------------------------------------------------------------------------------
 TYPE /fifo_coverage_pkg/FIFO_coverage/FIFO_Cross_cg
                             100.00%      100       -   Covered
  covered/total bins:                     66       66       -
  missing/total bins:                      0       66       -
  % Hit:                          100.00%      100       -
  Coverpoint cp_wr_en                     100.00%      100       -   Covered
    covered/total bins:                    2       2       -
    missing/total bins:                    0       2       -
    % Hit:                          100.00%      100       -
    bin auto[0]                       3052       1       -   Covered
    bin auto[1]                       6950       1       -   Covered
  Coverpoint cp_rd_en                     100.00%      100       -   Covered
    covered/total bins:                    2       2       -
    missing/total bins:                    0       2       -
    % Hit:                          100.00%      100       -
    bin auto[0]                       6955       1       -   Covered
    bin auto[1]                       3047       1       -   Covered
  Coverpoint cp_full                    100.00%      100       -   Covered
    covered/total bins:                    2       2       -
    missing/total bins:                    0       2       -
    % Hit:                          100.00%      100       -
    bin auto[0]                       6103       1       -   Covered
    bin auto[1]                       3899       1       -   Covered
  Coverpoint cp_empty                     100.00%      100       -   Covered
    covered/total bins:                    2       2       -
    missing/total bins:                    0       2       -
    % Hit:                          100.00%      100       -
    bin auto[0]                       9646       1       -   Covered
    bin auto[1]                        356       1       -   Covered
  Coverpoint cp_almostfull                  100.00%      100       -   Covered
    covered/total bins:                    2       2       -
    missing/total bins:                    0       2       -
    % Hit:                          100.00%      100       -
    bin auto[0]                       7418       1       -   Covered
    bin auto[1]                       2584       1       -   Covered
  Coverpoint cp_almostempty                  100.00%      100       -   Covered
    covered/total bins:                    2       2       -
    missing/total bins:                    0       2       -
    % Hit:                          100.00%      100       -
    bin auto[0]                       9524       1       -   Covered
    bin auto[1]                        478       1       -   Covered
  Coverpoint cp_wr_ack                    100.00%      100       -   Covered
    covered/total bins:                    2       2       -
    missing/total bins:                    0       2       -
    % Hit:                          100.00%      100       -
    bin auto[0]                       5840       1       -   Covered
    bin auto[1]                       4162       1       -   Covered
  Coverpoint cp_overflow                   100.00%      100       -   Covered
```

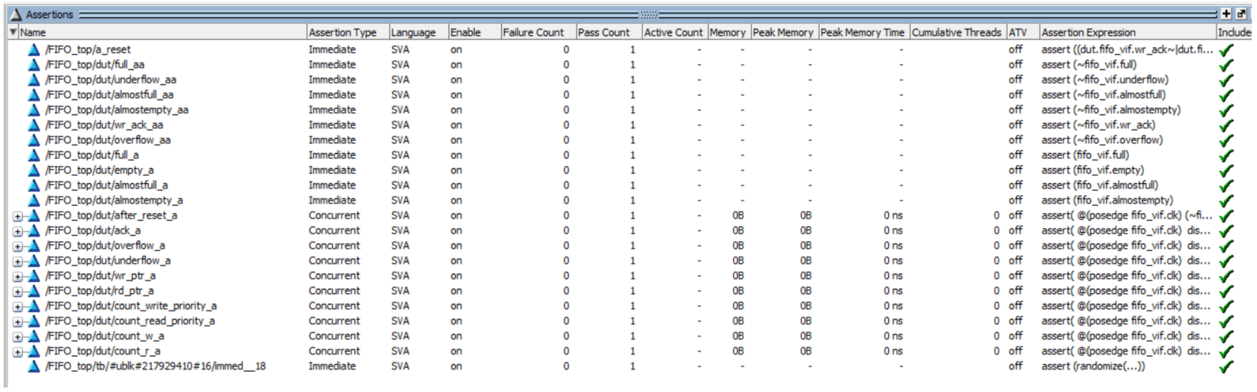
```
   covered/total bins:                     2       2       -
   missing/total bins:                     0       2       -
   % Hit:                        100.00%      100       -
   bin auto[0]                          7361       1       -   Covered
   bin auto[1]                          2641       1       -   Covered
 Coverpoint cp_underflow                  100.00%      100       -   Covered
   covered/total bins:                     2       2       -
   missing/total bins:                     0       2       -
   % Hit:                        100.00%      100       -
   bin auto[0]                          9892       1       -   Covered
   bin auto[1]                           110       1       -   Covered
 Cross cross_wr_rd_full                 100.00%      100       -   Covered
   covered/total bins:                     6       6       -
   missing/total bins:                     0       6       -
   % Hit:                        100.00%      100       -
   Auto, Default and User Defined Bins:
     bin <auto[1],auto[1],auto[0]>          2111       1       -   Covered
     bin <auto[0],auto[1],auto[0]>           936       1       -   Covered
     bin <auto[1],auto[0],auto[1]>          3088       1       -   Covered
     bin <auto[1],auto[0],auto[0]>          1751       1       -   Covered
     bin <auto[0],auto[0],auto[1]>           811       1       -   Covered
     bin <auto[0],auto[0],auto[0]>          1305       1       -   Covered
   Illegal and Ignore Bins:
     illegal_bin one_r_one                   0               -   ZERO
 Cross cross_wr_rd_empty                 100.00%      100       -   Covered
   covered/total bins:                     8       8       -
   missing/total bins:                     0       8       -
   % Hit:                        100.00%      100       -
   Auto, Default and User Defined Bins:
     bin <auto[1],auto[1],auto[1]>            36       1       -   Covered
     bin <auto[0],auto[1],auto[1]>            85       1       -   Covered
     bin <auto[1],auto[0],auto[1]>           111       1       -   Covered
     bin <auto[0],auto[0],auto[1]>           124       1       -   Covered
     bin <auto[1],auto[1],auto[0]>          2075       1       -   Covered
     bin <auto[0],auto[1],auto[0]>           851       1       -   Covered
     bin <auto[1],auto[0],auto[0]>          4728       1       -   Covered
     bin <auto[0],auto[0],auto[0]>          1992       1       -   Covered
 Cross cross_wr_rd_almostfull              100.00%      100       -   Covered
   covered/total bins:                     8       8       -
   missing/total bins:                     0       8       -
   % Hit:                        100.00%      100       -
   Auto, Default and User Defined Bins:
     bin <auto[1],auto[1],auto[1]>          1328       1       -   Covered
     bin <auto[0],auto[1],auto[1]>           359       1       -   Covered
     bin <auto[1],auto[0],auto[1]>           386       1       -   Covered
     bin <auto[0],auto[0],auto[1]>           511       1       -   Covered
     bin <auto[1],auto[1],auto[0]>           783       1       -   Covered
     bin <auto[0],auto[1],auto[0]>           577       1       -   Covered
     bin <auto[1],auto[0],auto[0]>          4453       1       -   Covered
     bin <auto[0],auto[0],auto[0]>          1605       1       -   Covered
 Cross cross_wr_rd_almostempty              100.00%      100       -   Covered
   covered/total bins:                     8       8       -
   missing/total bins:                     0       8       -
   % Hit:                        100.00%      100       -
   Auto, Default and User Defined Bins:
     bin <auto[1],auto[1],auto[1]>           177       1       -   Covered
     bin <auto[0],auto[1],auto[1]>            38       1       -   Covered
     bin <auto[1],auto[0],auto[1]>           164       1       -   Covered
     bin <auto[0],auto[0],auto[1]>            99       1       -   Covered
     bin <auto[1],auto[1],auto[0]>          1934       1       -   Covered
     bin <auto[0],auto[1],auto[0]>           898       1       -   Covered
     bin <auto[1],auto[0],auto[0]>          4675       1       -   Covered
     bin <auto[0],auto[0],auto[0]>          2017       1       -   Covered
 Cross cross_wr_rd_wr_ack                100.00%      100       -   Covered
   covered/total bins:                     6       6       -
   missing/total bins:                     0       6       -
   % Hit:                        100.00%      100       -
   Auto, Default and User Defined Bins:
     bin <auto[1],auto[1],auto[1]>          1263       1       -   Covered
     bin <auto[1],auto[0],auto[1]>          2899       1       -   Covered
     bin <auto[1],auto[1],auto[0]>           848       1       -   Covered
     bin <auto[0],auto[1],auto[0]>           936       1       -   Covered
     bin <auto[1],auto[0],auto[0]>          1940       1       -   Covered
     bin <auto[0],auto[0],auto[0]>          2116       1       -   Covered
   Illegal and Ignore Bins:
      illegal_bin zero_zero_one                 0               -   ZERO
  Cross cross_wr_rd_overflow                100.00%      100       -    Covered
    covered/total bins:                        6       6       -
    missing/total bins:                        0       6       -
    % Hit:                            100.00%      100       -
    Auto, Default and User Defined Bins:
      bin <auto[1],auto[1],auto[1]>            812       1       -   Covered
      bin <auto[1],auto[0],auto[1]>           1829       1       -   Covered
      bin <auto[1],auto[1],auto[0]>           1299       1       -   Covered
      bin <auto[0],auto[1],auto[0]>            936       1       -   Covered
      bin <auto[1],auto[0],auto[0]>           3010       1       -   Covered
      bin <auto[0],auto[0],auto[0]>           2116       1       -   Covered
    Illegal and Ignore Bins:
      illegal_bin zero_w_one                  0               -   ZERO
  Cross cross_wr_rd_underflow               100.00%      100       -    Covered
    covered/total bins:                        6       6       -
    missing/total bins:                        0       6       -
    % Hit:                            100.00%      100       -
    Auto, Default and User Defined Bins:
      bin <auto[1],auto[1],auto[1]>             74       1       -   Covered
      bin <auto[1],auto[1],auto[0]>           2037       1       -   Covered
      bin <auto[0],auto[1],auto[1]>             36       1       -   Covered
      bin <auto[0],auto[1],auto[0]>            900       1       -   Covered
      bin <auto[1],auto[0],auto[0]>           4839       1       -   Covered
      bin <auto[0],auto[0],auto[0]>           2116       1       -   Covered
    Illegal and Ignore Bins:
      illegal_bin zero_r_one                  0               -   ZERO
TOTAL COVERGROUP COVERAGE: 100.00%  COVERGROUP TYPES: 1
```

## Assertions Coverage:



Cover Directives

| Name | Language | Enabled | Log | Count | AtLeast | Limit | Weight | Cmplt % | Cmplt graph | Included | Memory | Peak Memory | Peak Memory Time | Cumulative Threads |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| /FIFO_top/dut/ack_c | SVA | ✓ | Off | 4068 | 1 | Unli... | 1 | 100% | 🟩 | ✓ | 0 | 0 | 0 ns | 0 |
| /FIFO_top/dut/overflow_c | SVA | ✓ | Off | 2587 | 1 | Unli... | 1 | 100% | 🟩 | ✓ | 0 | 0 | 0 ns | 0 |
| /FIFO_top/dut/underflow_c | SVA | ✓ | Off | 108 | 1 | Unli... | 1 | 100% | 🟩 | ✓ | 0 | 0 | 0 ns | 0 |
| /FIFO_top/dut/wr_ptr_c | SVA | ✓ | Off | 4068 | 1 | Unli... | 1 | 100% | 🟩 | ✓ | 0 | 0 | 0 ns | 0 |
| /FIFO_top/dut/rd_ptr_c | SVA | ✓ | Off | 2822 | 1 | Unli... | 1 | 100% | 🟩 | ✓ | 0 | 0 | 0 ns | 0 |
| /FIFO_top/dut/count_write_priority_c | SVA | ✓ | Off | 72 | 1 | Unli... | 1 | 100% | 🟩 | ✓ | 0 | 0 | 0 ns | 0 |
| /FIFO_top/dut/count_read_priority_c | SVA | ✓ | Off | 797 | 1 | Unli... | 1 | 100% | 🟩 | ✓ | 0 | 0 | 0 ns | 0 |
| /FIFO_top/dut/count_w_c | SVA | ✓ | Off | 2838 | 1 | Unli... | 1 | 100% | 🟩 | ✓ | 0 | 0 | 0 ns | 0 |
| /FIFO_top/dut/count_r_c | SVA | ✓ | Off | 867 | 1 | Unli... | 1 | 100% | 🟩 | ✓ | 0 | 0 | 0 ns | 0 |

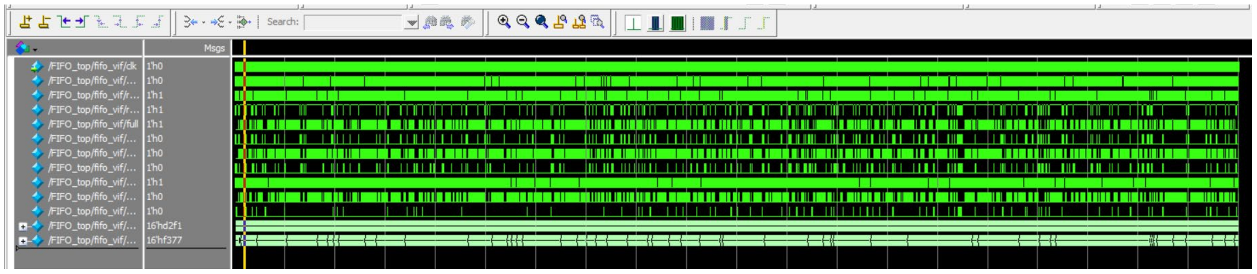


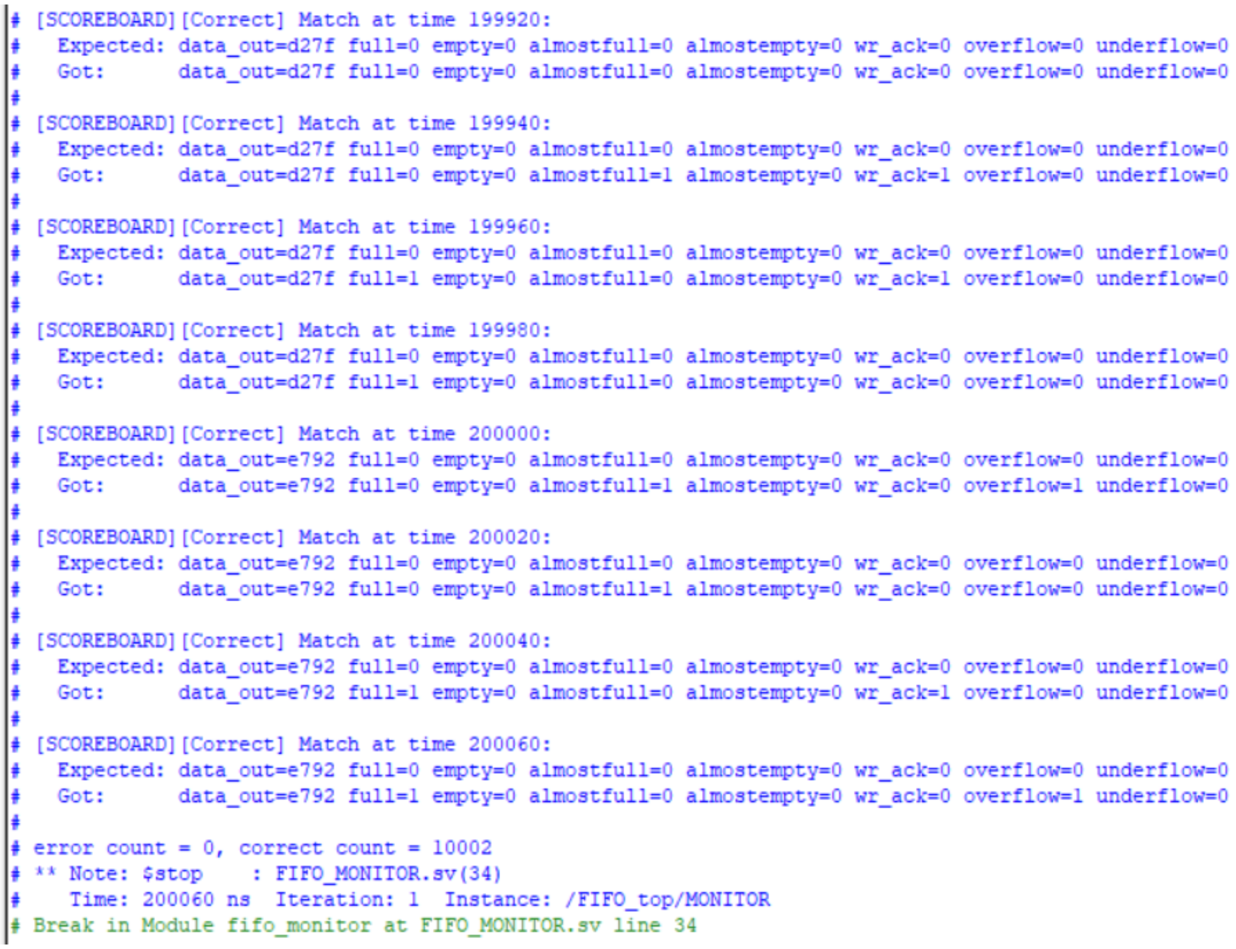
Assertions

| Name | Assertion Type | Language | Enable | Failure Count | Pass Count | Active Count | Memory | Peak Memory | Peak Memory Time | Cumulative Threads | ATV | Assertion Expression | Include |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| /FIFO_top/a_reset | Immediate | SVA | on | 0 | 1 | - | - | - | - |  | off | assert ((dut.fifo_vif.wr_ack~\|dut.fi... | ✓ |
| /FIFO_top/dut/full_aa | Immediate | SVA | on | 0 | 1 | - | - | - | - |  | off | assert (~fifo_vif.full) | ✓ |
| /FIFO_top/dut/underflow_aa | Immediate | SVA | on | 0 | 1 | - | - | - | - |  | off | assert (~fifo_vif.underflow) | ✓ |
| /FIFO_top/dut/almostfull_aa | Immediate | SVA | on | 0 | 1 | - | - | - | - |  | off | assert (~fifo_vif.almostfull) | ✓ |
| /FIFO_top/dut/almostempty_aa | Immediate | SVA | on | 0 | 1 | - | - | - | - |  | off | assert (~fifo_vif.almostempty) | ✓ |
| /FIFO_top/dut/wr_ack_aa | Immediate | SVA | on | 0 | 1 | - | - | - | - |  | off | assert (~fifo_vif.wr_ack) | ✓ |
| /FIFO_top/dut/overflow_aa | Immediate | SVA | on | 0 | 1 | - | - | - | - |  | off | assert (~fifo_vif.overflow) | ✓ |
| /FIFO_top/dut/full_a | Immediate | SVA | on | 0 | 1 | - | - | - | - |  | off | assert (fifo_vif.full) | ✓ |
| /FIFO_top/dut/empty_a | Immediate | SVA | on | 0 | 1 | - | - | - | - |  | off | assert (fifo_vif.empty) | ✓ |
| /FIFO_top/dut/almostfull_a | Immediate | SVA | on | 0 | 1 | - | - | - | - |  | off | assert (fifo_vif.almostfull) | ✓ |
| /FIFO_top/dut/almostempty_a | Immediate | SVA | on | 0 | 1 | - | - | - | - |  | off | assert (fifo_vif.almostempty) | ✓ |
| /FIFO_top/dut/after_reset_a | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert( @(posedge fifo_vif.clk) (~fi... | ✓ |
| /FIFO_top/dut/ack_a | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert( @(posedge fifo_vif.clk) dis... | ✓ |
| /FIFO_top/dut/overflow_a | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert( @(posedge fifo_vif.clk) dis... | ✓ |
| /FIFO_top/dut/underflow_a | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert( @(posedge fifo_vif.clk) dis... | ✓ |
| /FIFO_top/dut/wr_ptr_a | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert( @(posedge fifo_vif.clk) dis... | ✓ |
| /FIFO_top/dut/rd_ptr_a | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert( @(posedge fifo_vif.clk) dis... | ✓ |
| /FIFO_top/dut/count_write_priority_a | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert( @(posedge fifo_vif.clk) dis... | ✓ |
| /FIFO_top/dut/count_read_priority_a | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert( @(posedge fifo_vif.clk) dis... | ✓ |
| /FIFO_top/dut/count_w_a | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert( @(posedge fifo_vif.clk) dis... | ✓ |
| /FIFO_top/dut/count_r_a | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert( @(posedge fifo_vif.clk) dis... | ✓ |
| /FIFO_top/tb/#ublk#217929410#16/immed__18 | Immediate | SVA | on | 0 | 1 | - | - | - | - |  | off | assert (randomize(...)) | ✓ |

```
DIRECTIVE COVERAGE:
--------------------------------------------------------------------------------------
Name                          Design Design  Lang File(Line)     Hits Status
                              Unit   UnitType
--------------------------------------------------------------------------------------
/FIFO_top/dut/ack_c                  FIFO   Verilog  SVA  FIFO.sv(79)     4068 Covered
/FIFO_top/dut/overflow_c             FIFO   Verilog  SVA  FIFO.sv(80)     2587 Covered
/FIFO_top/dut/underflow_c            FIFO   Verilog  SVA  FIFO.sv(81)      108 Covered
/FIFO_top/dut/wr_ptr_c               FIFO   Verilog  SVA  FIFO.sv(82)     4068 Covered
/FIFO_top/dut/rd_ptr_c               FIFO   Verilog  SVA  FIFO.sv(83)     2822 Covered
/FIFO_top/dut/count_write_priority_c FIFO   Verilog  SVA  FIFO.sv(84)       72 Covered
/FIFO_top/dut/count_read_priority_c  FIFO   Verilog  SVA  FIFO.sv(85)      797 Covered
/FIFO_top/dut/count_w_c              FIFO   Verilog  SVA  FIFO.sv(86)     2838 Covered
/FIFO_top/dut/count_r_c              FIFO   Verilog  SVA  FIFO.sv(87)      867 Covered
TOTAL DIRECTIVE COVERAGE: 100.00%  COVERS: 9
```

## QuestaSim waveform snippets


Search:
Msgs
/FIFO_top/fifo_vif/clk 1'h0
/FIFO_top/fifo_vif/... 1'h0
/FIFO_top/fifo_vif/r... 1'h1
/FIFO_top/fifo_vif/r... 1'h1
/FIFO_top/fifo_vif/full 1'h1
/FIFO_top/fifo_vif/... 1'h0
/FIFO_top/fifo_vif/... 1'h0
/FIFO_top/fifo_vif/... 1'h0
/FIFO_top/fifo_vif/... 1'h1
/FIFO_top/fifo_vif/... 1'h0
/FIFO_top/fifo_vif/... 1'h0
/FIFO_top/fifo_vif/... 16'hd2f1
/FIFO_top/fifo_vif/... 16'hf377


```
# [SCOREBOARD][Correct] Match at time 199920:
#   Expected: data_out=d27f full=0 empty=0 almostfull=0 almostempty=0 wr_ack=0 overflow=0 underflow=0
#   Got:      data_out=d27f full=0 empty=0 almostfull=0 almostempty=0 wr_ack=0 overflow=0 underflow=0
#
# [SCOREBOARD][Correct] Match at time 199940:
#   Expected: data_out=d27f full=0 empty=0 almostfull=0 almostempty=0 wr_ack=0 overflow=0 underflow=0
#   Got:      data_out=d27f full=0 empty=0 almostfull=1 almostempty=0 wr_ack=1 overflow=0 underflow=0
#
# [SCOREBOARD][Correct] Match at time 199960:
#   Expected: data_out=d27f full=0 empty=0 almostfull=0 almostempty=0 wr_ack=0 overflow=0 underflow=0
#   Got:      data_out=d27f full=1 empty=0 almostfull=0 almostempty=0 wr_ack=1 overflow=0 underflow=0
#
# [SCOREBOARD][Correct] Match at time 199980:
#   Expected: data_out=d27f full=0 empty=0 almostfull=0 almostempty=0 wr_ack=0 overflow=0 underflow=0
#   Got:      data_out=d27f full=1 empty=0 almostfull=0 almostempty=0 wr_ack=0 overflow=0 underflow=0
#
# [SCOREBOARD][Correct] Match at time 200000:
#   Expected: data_out=e792 full=0 empty=0 almostfull=0 almostempty=0 wr_ack=0 overflow=0 underflow=0
#   Got:      data_out=e792 full=0 empty=0 almostfull=1 almostempty=0 wr_ack=0 overflow=1 underflow=0
#
# [SCOREBOARD][Correct] Match at time 200020:
#   Expected: data_out=e792 full=0 empty=0 almostfull=0 almostempty=0 wr_ack=0 overflow=0 underflow=0
#   Got:      data_out=e792 full=0 empty=0 almostfull=1 almostempty=0 wr_ack=0 overflow=0 underflow=0
#
# [SCOREBOARD][Correct] Match at time 200040:
#   Expected: data_out=e792 full=0 empty=0 almostfull=0 almostempty=0 wr_ack=0 overflow=0 underflow=0
#   Got:      data_out=e792 full=1 empty=0 almostfull=0 almostempty=0 wr_ack=1 overflow=0 underflow=0
#
# [SCOREBOARD][Correct] Match at time 200060:
#   Expected: data_out=e792 full=0 empty=0 almostfull=0 almostempty=0 wr_ack=0 overflow=0 underflow=0
#   Got:      data_out=e792 full=1 empty=0 almostfull=0 almostempty=0 wr_ack=0 overflow=1 underflow=0
#
# error count = 0, correct count = 10002
# ** Note: $stop    : FIFO_MONITOR.sv(34)
#    Time: 200060 ns  Iteration: 1  Instance: /FIFO_top/MONITOR
# Break in Module fifo_monitor at FIFO_MONITOR.sv line 34
```