Serial Peripheral Interface (SPI) with Direct Memory-Mapped PSRAM Interface

1. Overview

This SPI controller has been desined based on the SiFive’s Serial Peripheral Interface (SPI) controller. This SPI controller adds the direct memory-mapped PSRAM interface function to the SiFive's SPI controller. Refer to *SiFive FE310-G002 Manual* for the specification of the SiFives’s SPI controller.

The direct memory-mapped PSRAM interface function has been designed to work with AP Memory’s SPI PSRAMs, such as APS6404L-3SQN.

2. Memory Map

The memory map for the SPI control registers is shown in Table 1. The SPI memory map has been designed to require only naturally-aligned 32-bit memory accesses.

Table 1: Register offsets within the SPI memory map.

Offset	Name	Description
0x00	sckdiv	Serial clock divisor
0x04	sckmode	Serial clock mode
0x08	Reserved	
0x0C	Reserved	
0x10	csid	Chip select ID
0x14	csdef	Chip select default
0x18	csmode	Chip select mode
0x1C	Reserved	
0x20	Reserved	
0x24	Reserved	
0x28	delay0	Delay control 0
0x2C	delay1	Delay control 1
0x30	Reserved	
0x34	Reserved	
0x38	Reserved	
0x3C	Reserved	

0x40	fmt	Frame format
0x44	Reserved	
0x48	txdata	Tx FIFO data
0x4C	rxdaa	Rx FIFO data
0x50	txmark	Tx FIFO watermark
0x54	rxmark	Rx FIFO watermark
0x58	Reserved	
0x5C	Reserved	
0x60	fctrl	SPI Flash interface control
0x64	ffmt	SPI Flash interface format
0x68	**rctrl**	**SPI PSRAM interface control**
0x6C	Reserved	
0x70	ie	SPI interrupt enable
0x74	ip	SPI interurpt pending

Refer to *SiFive FE310-G002 Manual* for the specification of the registers other than SPI PSRAM Interface Control Register (`rctrl`).

3. SPI PSRAM Interface Control Register (`rctrl`)

The `rctrl` register defines the SPI PSRAM write command code issued by the SPI controller when the direct memory-mapped region is accessed. The read command code and the command format are defined by the SPI Flash Instruction Format Register (`ffmt`).

The register defines the page size of PSRAM. Burst accesses to the PSRAM do not cross page boundaries.

The register defines the maximum continuous active period of chip enable to the PSRAM. When the continuous active period exceeds the value set in the register, the chip enable is negated. Set the period to meet the PSRAM's AC characteristic.

Table 2 describes the function and reset value of each field.

Table 2: SPI PSRAM Interface Control Register

SPI PSRAM Interface Control Register (`rctrl`)				
Register Offset		0x68		
Bits	Field Name	Attr.	Rst.	Description
[7:0]	wcmd_code	RW	0x02	Value of write command code
[11:8]	page_size	RW	0x9	Page size (2^{page_size} bytes)

[23:12]	max_cen_cyc	RW	0x080	Maximum continuous active period of chip enable in the SPI controller’s input clock cycles.
[31:24]	Reserved			