NRAM as a potential DRAM replacement

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Abstract. DRAM is globally used in for example over mobile devices, deskop pcs and data centers and it has been improved over 50 years. As a result, improving DRAM becomes more difficult. Meanwhile new materials have been discovered and people have started to test, if they could be a better alternative for DRAM. In this paper we're discussing the motivation, why replacing DRAM might be more suitable than trying to keep improving DRAM and why NRAM is a potential replacement for DRAM.

Keywords: DRAM · NRAM · Carbon nanotubes

1 Introduction

DRAM was invented in 1970 and has been excessively used since then for various electronic devices. For this reason researchers are constantly trying to improve the performance and efficiency of DRAM to keep up with the other electronic components like a central processing unit (CPU) of a personal computer (PC) in order to not becoming a bottle neck to them.

We will take a rough overview of DRAM itself and look into some of its characteristics and its challenges and why NRAM *could* be a replacement for DRAM in the future.

2 DRAM

A *Dynamic Random Access Memory (DRAM)* is mostly known for its excessive usage in PCs and mobile devices, due to its low cost and increasing improvement over the time. In order to understand if it's even worth it to try to replace DRAM with another technology, we will have to take a look into it's functionality what it implies.

2.1 Organization

One DRAM-Module holds in general several storage-matrices as shown in figure 2.1. If we want to access a specific cell, which holds the data 1 or 0, from the matrix, we'd set a current on the given *Word Line* from figure 2 which is selected by a multiplexer in the *Row Address Selection* from figure 2.1.

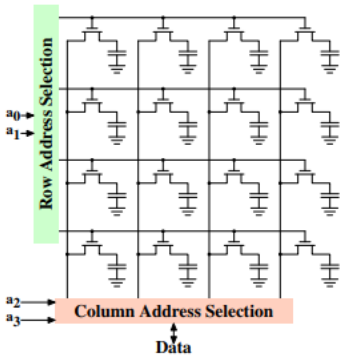

Fig. 1. A storage-matrix made out of DRAM cells as shown in figure 2.

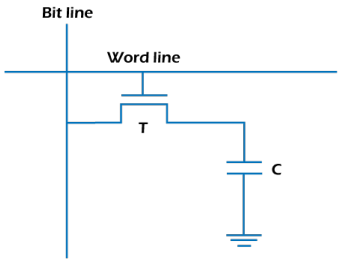

Fig. 2. A DRAM-cell where the capacitor (C) holds the state of the cell by holding the electrons, to represent the state *SET* and holding none electrons to represent the state *UNSET*.

Reading After setting a current on the given *Word Line*, the transistor *T* lets the electrons pass through it and moves the electrons inside the capacitor to the bit line, if there are any. Then the electric charge is read from the bit line and stored in a buffer where the column selection decides which bits should be moved into the data bus to send them to their destination.

Writing Writing into a DRAM cell works similar as reading from it. The difference is mainly, that we've already set the value on the bit line which is simply going through the transistor and then to the capacitor which will hold the value afterwards.

2.2 Disadvantages and challenges

Now after getting a rough overview how the two main actions (*reading* and *writing*) work, we can now go to its challenges and why they exist.

Refresh times One property of a capacitor is that it loses its charge, which would result into information loss. In order to avoid this, the DRAM module schedules a refresh after some milliseconds on the capacitors to avoid losing the information. No memory-operation can be executed during the refreshing time and also power has to be used for this action. Due to this property of losing the charge if the DRAM module doesn't receive power, DRAM belongs to the type of *volatile* memory [14].

To sum it up: DRAM allows only a specific time window where we can work with the actual data.

Variable Retention Time The maximum duration for a DRAM cell to hold it's value is also called its *retention time*. In general, good DRAM cells have a

high retention time and thus a low leakage from the capacitor while bad DRAM cells are the opposite, they have a low retention time due to a high leakage from the capacitor. There's the *Variable Retention Time Phaenomen (VRT)* which describes the behaviour of DRAM cells which randomly switch between good and bad DRAM cells. There are some solutions like an on-die ECC (Error Correcting Code) which fixes most of the data corruptions due to VTR but with the cost of more required space for an additional cell array and a higher power consumption [14].

To sum it up: DRAM suffers from non-deterministic behaviour of the capacitor which requires additional hardware to avoid them.

Thermal limits On the one hand DRAM modules are working very reliable from 0°C to about 85°C. Starting from 85°C to about 95°C it starts to get some smaller errors until it goes above 95°C where it starts losing data. But on the other hand automotive and other industries are using DRAM modules in wider temperature spans, up to 125°C. The higher the temperature gets, the higher the leakage of a capacitor becomes as well hence the capacitor needs to be refreshed more often but setting a current on the cell is also creating heat so it's a dead end if a DRAM module becomes too hot. That's where a shutdown is the only way out [14].

To sum it up: The industry requires more resistant memory modules to operate under difficult environments but DRAM is reaching its limits to fulfill them.

Limited minimum size It's desired to decrease the total size of a DRAM cell in order to put more cells for the same amount of space but this road can't be followed forever. There's an aspect ratio between the size of the DRAM cell and its effectiveness: The smaller a DRAM cell gets the smaller the capacitor has to become as well. Hence its charge-capacity will also decrease and more frequent refresh times are required to avoid unwanted data loss. To present the latest DDR5 has DRAM cells of about 15 nm and DRAM cells can't become smaller then 10nm otherwise they aren't effective enough to be used, so the limit is almost reached [14] [4].

To sum it up: DRAM cells are reaching their minimal size, hence the density can't be improved for a long time anymore.

Row-Hammer attack The required recharging times leads to an unsolvable challenge for DRAM-modules, called "row hammer" as explained in [12]. To sum it up, it's possible to flip some bits but unwanted, by frequently accessing it's nearby rows which will discharge the capacitors of our target row faster and if the recharge-timing can't keep up, the state of the capacitor will alter which could result into possible security exploits or data corruption [14].

To sum it up: DRAM suffers from an unfix able security issue where workarounds are only possible.

2.3 Summary

As we can see, DRAM includes various issues with only little space for improvement, if there's any. This is mostly due to the capacitor which is an essential component for a DRAM cell and improving the capacitor isn't possible. Therefore a replacement for the capacitor to hold the data is a possible way to fix or avoid the problems as told before. And now we'll introduce such a possible replacement for the capacitor and with that the DRAM cell: Nano-RAM.

3 NRAM

Nano-RAM or *Nanotube-RAM* (NRAM) is a different computer memory technology from the company *Nantero* who invented NRAM. Instead of relying on a capacitor as DRAM does it makes use of *carbon nanotubes* to save the state of a memory cell. We'll dive into some properties of carbon nanotubes first to get a rough understanding what a NRAM cell is made of.

3.1 Carbon Nanotubes

Carbon Nanotubes (CNT) are in general a very interesting material due to its various use cases for example as a building material, for solar cells but also for transistors and this is thanks to their structure which we will introduce now.

Structure CNTs consist only of carbon atoms whereby the carbon atoms have a honeycomb structure with hexagons and three bonding partners each. They can have different amount of layers as you can see in 3. CNTs with only a single wall are called *single-walled carbon nanotubes* (SWCNT) and CNTs with more than one layer are called *multi-walled carbon nanotubes* (MWCNT). The diameter of a SWCNT is commonly below about 2.5 nm while the diameter of a MWCNT in general starts from about 5 nm [10].

CNTs can be also either open or closed tubes, empty and filled tubes (for example with silver, liquid or noble gases). Depending on the structure, the electrical conductivity within the tube is metallic or semi-conductive. There are even CNTs which are superconducting at low temperatures. CNTs with an ideally hexagonal structure have a uniform thickness and are linear but kinked or narrowing tubes which even contain pentagonal carbon rings are also possible [2].

MWCNTs also share a lot of properties with graphite because the distance between two layers in a MWCNT (3.40Å) and graphite (3.35Å) are almost identical and both are only made out of carbon. As a result CNTs can be described by the same way as graphene by lattice vectors as shown in 4.

The greenish part should represent the CNT from a side view as if you'd hold the tube in front of you and each tube opening is at the top and at the bottom. As a result the vector $\vec{C_h}$ is the tangent of the tube which represents the line as if we would cut through the CNT. The vectors $\vec{a_1}$ and $\vec{a_2}$ are spanning a so-called

Fig. 3. On the left you can see a SWCNT and on the right a MWCNT .

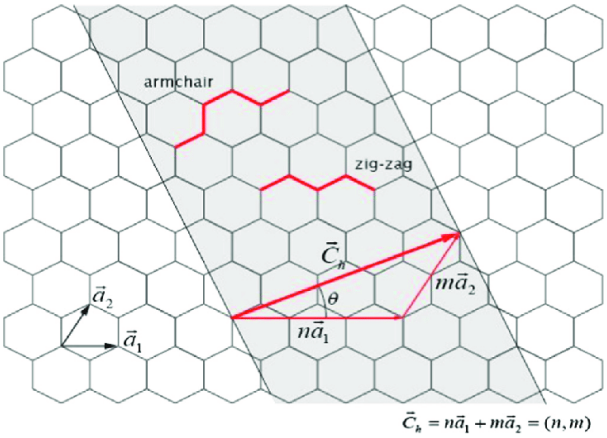

Fig. 4. Graphene honeycomb grid of a rolled up CNT .

unit cell. Both are basis vectors, hence linear independent, for the honeywomb. So $\vec{C}_h$ can be written (or calculated) as

$$\vec{C}_h = na_1 + ma_2$$

where $n, m \in \mathbb{Z}$. Also, due to the hexagonal symmetry it implies that $0 \leq |m| \leq n$. θ can be calculated by na_1 and ma_2 hence the degree of how the honeywomb got rolled up can be calculated as well. Therefore n and m are providing all necessary information to calculate other values from the CNT. They are often written as an index pair (n, m) to identify and distinguish all possible CNTs . Some types of index pairs have been named but since there are too many possible index pairs to give every single index pair a distinct name, three different classes of CNTs have been created: *armchair* if $n = m$ (see figure 5, *zigzag* if $m = 0$ (see figure 6), otherwise *chiral* [10].

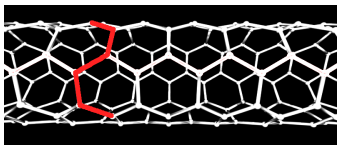

Fig. 5. An armchair CNT with a $(4, 4)$ configuration.

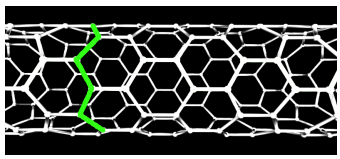

Fig. 6. A zigzag CNT with a $(8, 0)$ configuration.

Properties The index pair (n, m) also determines which kind of CNTs are metallic or semiconducting. If $\frac{(n-m)}{3}$ is an integer, then the CNT is metallic or else semiconducting. This means for example that all armchair CNTs are metallic and some zigzag or chiral CNTs are either metallic or semi conductive [2].

Regarding the electronics industry, CNTs have some other very attractive electrical properties: Their current carrying capacity is estimated to be 1000 times higher than that of copper wires and with a thermal conductivity of $6000\frac{W}{m*K}$ at room temperature, it's almost twice as high as that of diamond with $3320\frac{W}{m*K}$ so it's one of the best naturally heat conductors. As said before, they can also be used as semiconductors which makes them an attractive alternative for creating transistors which can withstand higher voltages and temperatures - and therefore higher clock frequencies - than silicon transistors [2].

Production One of the most common and promising ways to produce CNTs is by a *catalytic vapor phase deposition (CVD)* of carbon due to its simplicity regarding the required equipment, its operation and lower cost in comparison to other production methods [15]. Figure 7 shows a simple form of a CVD setup.

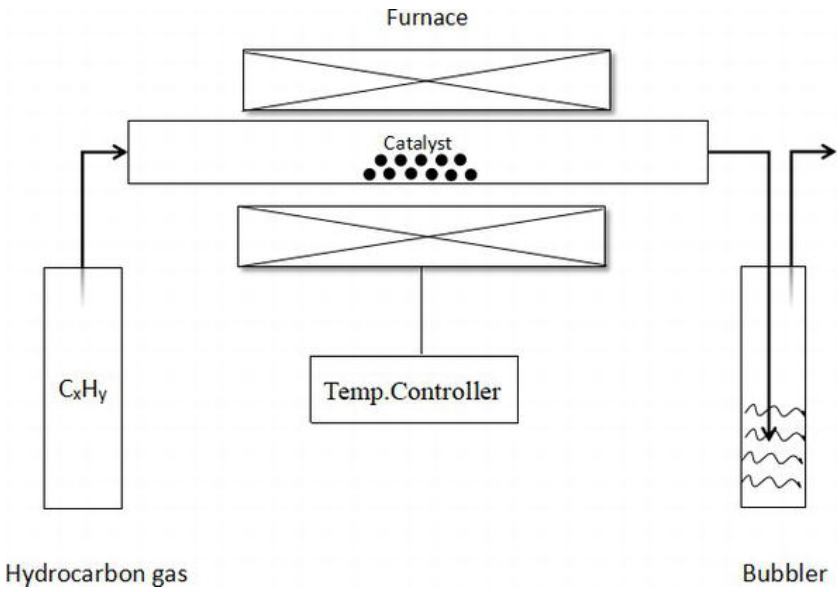

Fig. 7. Simple form of CVD setup to create CNTs.

In order to produce the CNTs with the CVD setup, a continuously flow of carbon atom-containing gas gets inserted into a tubular reactor which contains the catalyst and substrates at a sufficiently high temperature. The carbon atom-containing gas gets split up into carbon and hydrogen atoms at the substrate. From there, the carbon atoms are forming a CNT while the hydrogen keeps flowing through the tube and exits it [15].

3.2 The NRAM cell

As already told before CNTs have some very interesting properties for using them in transistors as they are behaving like a metal or a semiconductor, depending on their structure and in theory it has a lot of improvements in comparison to DRAM as shown in figure 8.

NRAM cells, as shown in figure 9, contain various amount of CNTs which influence the resistance of the cell: CNTs which are touching each other result into a lower cell resistance while not touching each other results into the opposite. This can be used to differentiate between 1s and 0s. In this case SET represents 0 and RESET 1. The data can be read by applying a little current between the upper and bottom electrode and test if a current flows through the cell. If the NRAM cell is in the SET state, no current is flowing due to the high resistance otherwise, if it's flowing, then the NRAM cell is in the RESET state due to the low resistance.

The state can be toggled by applying a small voltage greater than the read voltage between the top and bottom electrode. If the cell is in the SET state,

Timing	DDR4 SDRAM ns	DDR4 NRAM ns	DDR5 SDRAM ns
Row cycle	47.00	46.25	50.18
Access time	17.14	13.50	18.18
Row to column	15.00	23.00	18.18
Precharge	15.00	14.25	18.18
Write recovery	15.00	23.00	30.00
Activate to precharge	32.00	32.00	32.00
Refresh	350.00	0	350.00

Fig. 8. A comparison between DDR4 NRAM and DDR4 SDRAM and DDR5 SDRAM.

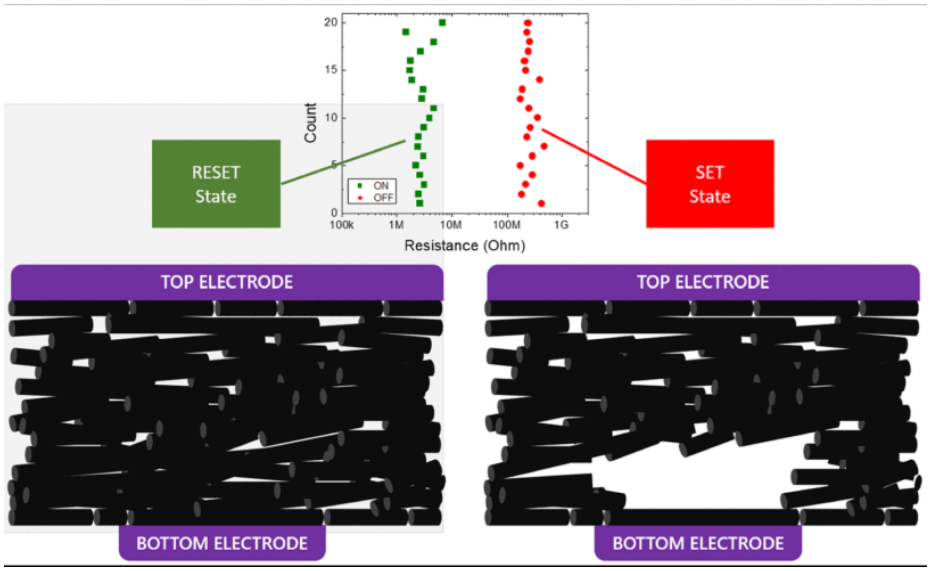

Fig. 9. A NRAM cell with its two different states. The black tubes should represent the nanotubes.

then the applied voltage will cause an electrostatic attraction between the CNTs. After the applied voltage is removed the CNTs remain in their state thanks to the Van-der-Waal's forces. Applying a small voltage (which is still greater than the read voltage) to the NRAM cell again will generate CNT phonon excitations with enough energy to separate the CNT from their conjunction points [7].

3.3 Advantages of NRAM in comparison to DRAM

Now after getting a rough overview of how a NRAM cell stores its data, we will introduce its improvements in comparison to DRAM and why it solves the issues of DRAM.

Non-Volatile Since the NRAM cells hold each state after setting it, NRAM belongs to the type of *non-volative memory* which means that the state of a cell doesn't get lost after removing the power supply. This gives us the opportunity for example to improve the boot up time of systems since their state after a full system shutdown still remains in the memory and it can continue where it stopped.

Better efficiency Compared to DRAM, NRAM doesn't require refresh times. Hence power is only required for reading and writing into the NRAM cell. In total NRAM can reduce the required memory power by between 21% and 50% compared to DRAM [9].

Also without the required refresh times there will be more time for computational relevant memory accesses which results into faster computation times.

Better Resistance Since it's required to have a higher activation energy than 5 eV to switch between the states of a NRAM cell, environmental noise like radiation, magnetism and vibration, which could cause problems to DRAM cells, can't affect NRAM cells. Those also have been tested on the space shuttle Atlantis without any problems [7] [9].

In addition to that, longer CNTs have a good thermal conductivity [11] [9] which reduces the risk of overheating the hardware.

Regarding endurance, it's assumed that the state of a NRAM cell can hold up to 300 years at over 300°C which makes NRAM attractive for the automotive for example [9].

Higher density and no Row-Hammer attack The minimal size for NRAM with less than 7nm [7] is smaller than the minimal size for DRAM cells. In addition to that no additional hardware is required to prevent row-hammer-attacks as this kind of attack doesn't exist for NRAM cells. That also counts variable retention times in since they also can't occur as NRAM cells aren't leaking anything. Thus there's more space which could be used for additional NRAM cells for a higher capacity and a better cost-per-area ratio, since no additional security-hardware is required.

3.4 State of the art

As we could see throughout this paper, NRAM seems to solve all problems from DRAM in *theory*, but that's not it: A NRAM module of 16 Mb was created and tested by [13] under a difficult environment where DRAM can't operate due to the high temperature. Not only that, the transistor size could even be reduced by 49%. Nevertheless at present there are no commercial products available yet and activity about NRAM became silent although Nantero told that there will be already chips available before 2010 [5] or soon after 2017 [1]. But companies are still believing on the technology and funded Nantero with $31.5 million dollar [6]. Fujitsu even acquired a licence of Nantero to start mass produce NRAM modules but that didn't happen either [3].

4 Summary

As we can see, in theory NRAM is a good candidate to replace DRAM with its improvements regarding efficiency, security, speed and future proof, but it lacks the full proof in practice. Time will tell us when NRAM modules are available and if they fulfill their expectations.

5 Image sources

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