Lab Report #1

Digital Logic Design

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Submitted to:

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Introduction to basic logic gates IC's On Digital Logic Trainer and Proteus Simulation.

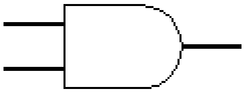
Part 1:

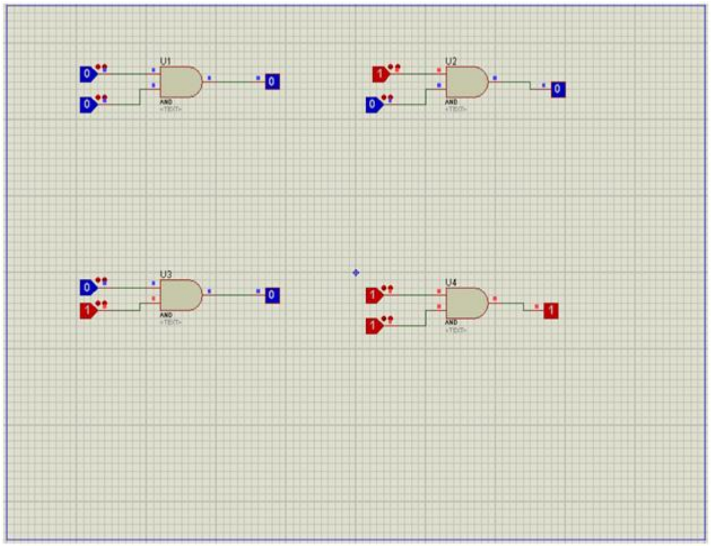
Verifying basic logic gates on proteus

AND Gate:

AND gate gives high output only when both inputs are 1, otherwise gives 0. It is clear from the name "and". If both a and b are true, then output is true.

Functionally: AND = a.b





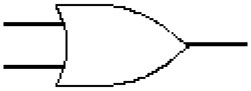
A	B	F = A . B

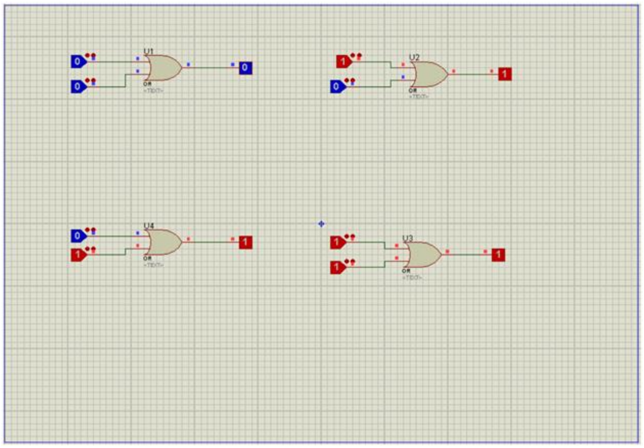
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate:

OR gate gives high output if any one of its inputs is 1 and even if both inputs are 1. Only condition for or gate to give low output is when both inputs are low. As the name “or” suggests. Input is 1 when either a or b is 1.

Functionally OR = a+b





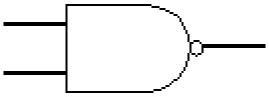
A	B	F = A + B
0	0	0
0	1	1

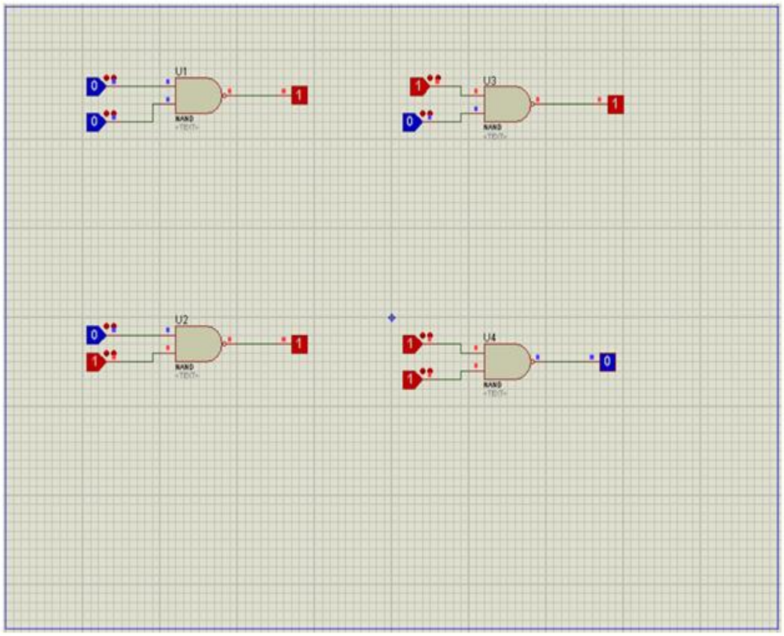
1	0	1
1	1	1

NAND Gate:

NAND gate is negation of and gate. It gives 0 output when both of its inputs are 1 and give 1 output in all other cases.

Functionally NAND = ~(a.b)





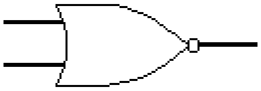
A	B	F = A . B	~F

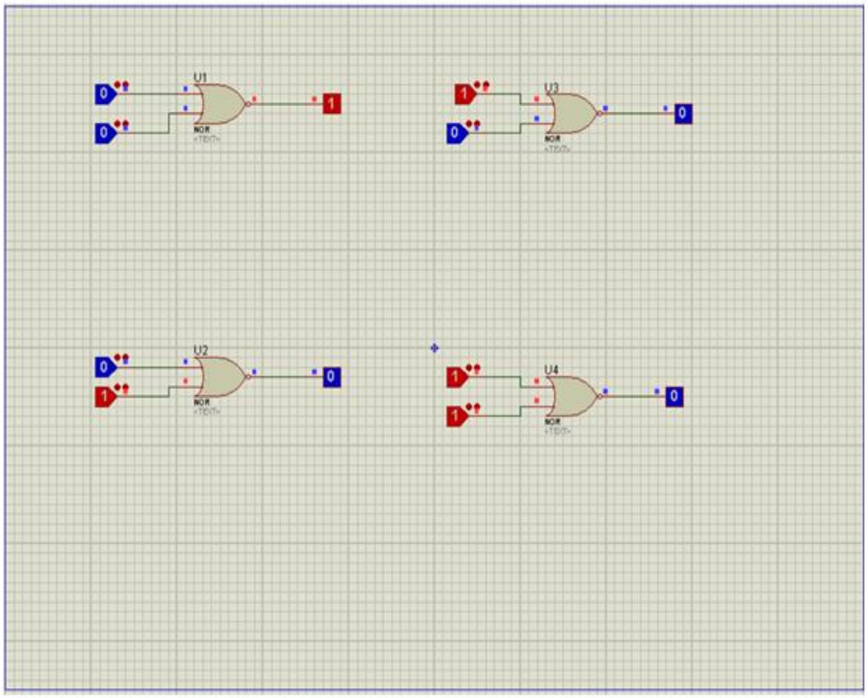
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

NOR gate:

NOR gate is negation of OR gate. It gives 1 output only when both inputs are 0, otherwise gives 0.

Functionally NOR = ~(a+b)





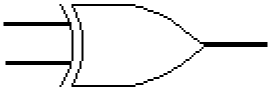
A	B	F = A + B	F’

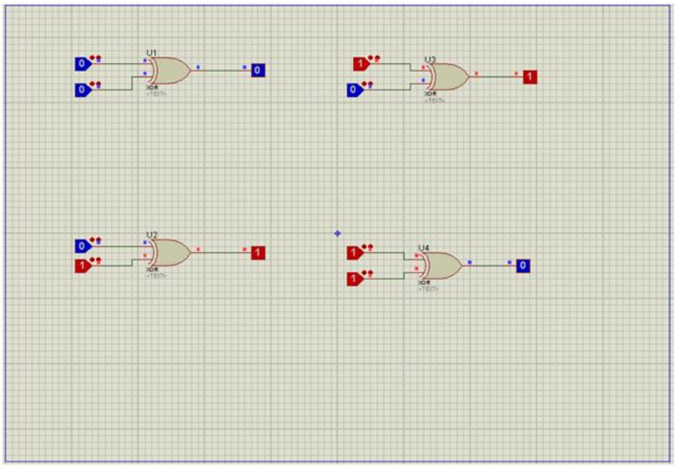
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

XOR Gate:

XOR gate gives 1 as output when either one of the inputs is 1 and other is 0. It gives 0 if inputs are same. In case of inputs more than 2, even 1’s make output 0 and odd 1’s make output 1.

Functionally XOR = (a.~b) + (~a.b)





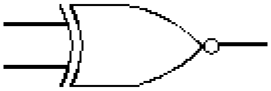
A	B	F = AB’ + A’B
0	0	0
0	1	1

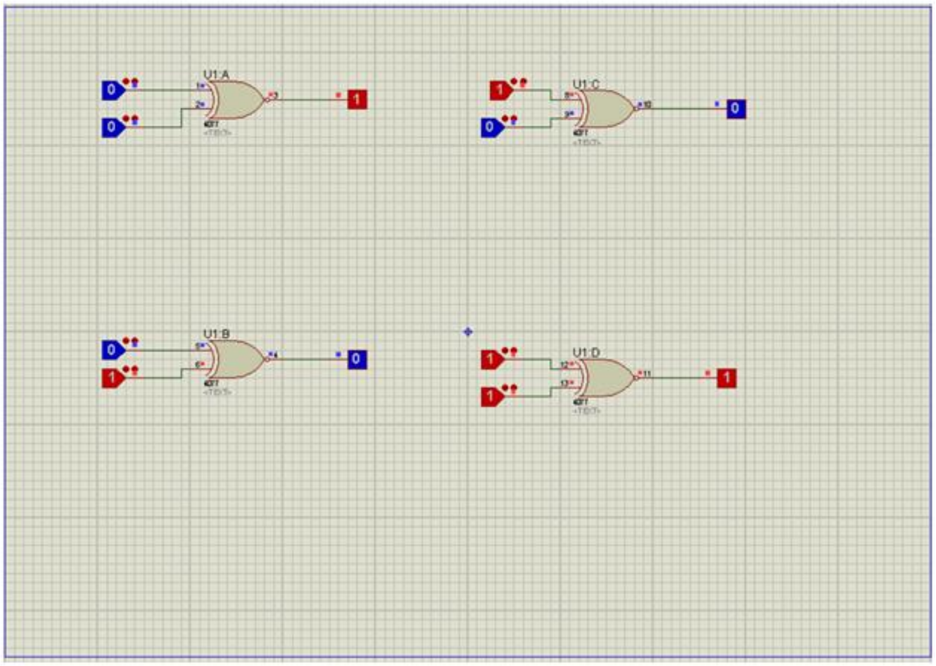
1	0	1
1	1	0

XNOR Gate:

XNOR gate is negation of XOR gate. It gives high output when both inputs are 1 or in case of more than 2 inputs, even inputs are 1.

Functionally XNOR = ~((a.~b)+(~a.b))





A	B	F = AB’ + A’B	~F

0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

Part 2: Verifying logic gates on IC’s

Apparatus:

- IC’s
- Connecting wires
- Bread board
- KL-31001 work station

Procedure:

- Put IC’s with AND, OR, NOT gates on work table.
- Verify basic AND, OR, NOT gates by connecting inputs to supply with wires and outputs to led.
- Combine basic gates to make NAND, NOR, XOR, XNOR gates.
- Verify these combinations of gates by connecting to supply and led.

Truth Table:

A	**B**	**AND**	**OR**	**XOR**	**NAND**	**NOR**	**XNOR**
0	0	0	0	0	1	1	1
0	1	0	1	1	1	0	0
1	0	0	1	1	1	0	0

1	1	1	1	0	0	0	1

POST LAB TASK

Make a list of Logic Gate ICs of TTL and CMOS family along with the ICs name

	7400 Series	4000 Series
1	Quad 2-input AND (7408)	Quad 2-input AND (4081)
2	Quad 2-input OR (7432)	Quad 2-input OR (4071)
3	Hex 1-input NOT (7404)	Hex 1-input NOT (4069)
4	Quad 2-input NOR (7402)	Quad 2-input NOR (4001)
5	Quad 2-input NAND (7400)	Quad 2-input NAND (4011)
6	Quad 2-input XOR (7486)	Quad 2-input XOR (4070)
7	Quad 2-input XNOR (747266)	Quad 2-input XNOR (4077)
8	Triple 3-Input AND (7411)	Triple 3-Input AND (4073)
9	Triple 3-Input OR (744075)	Triple 3-Input OR (4075)
10	Triple 3-Input NOR (7427)	Triple 3-input NAND (4023)
11	Triple 3-Input NAND (7010)	Triple 3-Input NOR (4025)
12	Dual 4-input AND (7421)	Dual 4-Input AND (4082)
13	Dual 4-input OR (744072)	Dual 4-Input OR (4072)
14	Dual 4-input NOR (7429)	Dual 4-input NAND (4012)
15	Dual 4-input NAND (7420)	Dual 4-Input NOR (4002)

Q 2: What is Fan-in and Fan-out?

Fanning-in and Fanning-out the maximum number of input signals that can feed a logic cell's input equations is referred to as fan-in. The maximum number of output signals fed by a logic cell's output equations is referred to as fan-out.

Critical Analysis

In the lab 01 of DLD we learned some basics of DLD like we learned how to use to use bread board in the lab and we prepared the basic gates on the bread board likewise we learned how to make the circuits of different basic gates and the most important we started identifying the gates just by looking at the codes written on IC'S. After doing this by the means of hardware we did the same verification using the software named PROTEUS and attached the screenshots in the lab report.