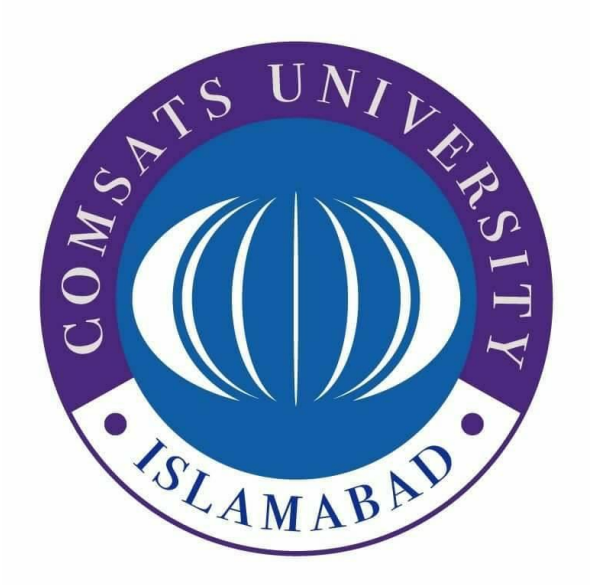
Lab Report #2

Digital Logic Design



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Submitted to:

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Boolean Function Implementation using Universal gates

Equipment Required:

- Bread Board
- Wires
- Logic Gate IC's
- Power Supply
- KL-31001 Digital Logic Lab

Background Theory:

NOR and NAND gates are called universal gates as all gates can be made from these two gates. Any Boolean equation can be made using only these two gates. There are many benefits to doing this as it is much simpler to implement functions and it saves production costs as well.

Lab Tasks:

Part 1:

Implement Any Logic Expression Using Only NAND Gates:

Procedure:

- Simulate NOT, AND, OR, XOR and XNOR gates in Proteus software by using NAND gates. Verify their truth tables.
- Insert IC on the trainer's breadboard.
- Use any one or more of the NAND gates of the IC for this experiment.

- One or more Logic switches of the trainer can be used as input for the NAND gate.
- For output indication, connect the output pin of the circuit to any one of the LED's of the trainer.

Verification of NOT function:

Procedure:

- Connect the circuit as shown in the figure.
- Connect +5V to pin 14(Vcc) and Ground pin to 7 (GND) of the IC.
- By setting the switches to 1 and 0, verify that the output (F) of the circuit conforms to that of a NOT gate. Record your observations in a table.

Figure:

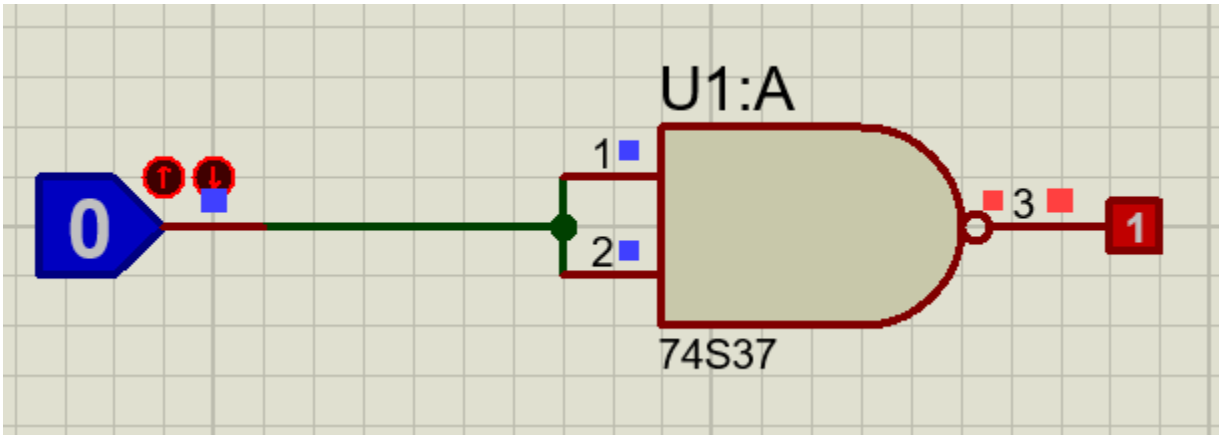

Table:

Input	Output
A	F
0	1
1	0

Verification of AND function:

Procedure:

- Connect the circuit as shown in the figure.
- Connect +5V to pin 14(Vcc) and Ground pin to 7 (GND) of the IC.
- By setting the switches to 1 and 0, verify that the output (F) of the circuit conforms to that of a AND gate. Record your observations in a table.

Figure:

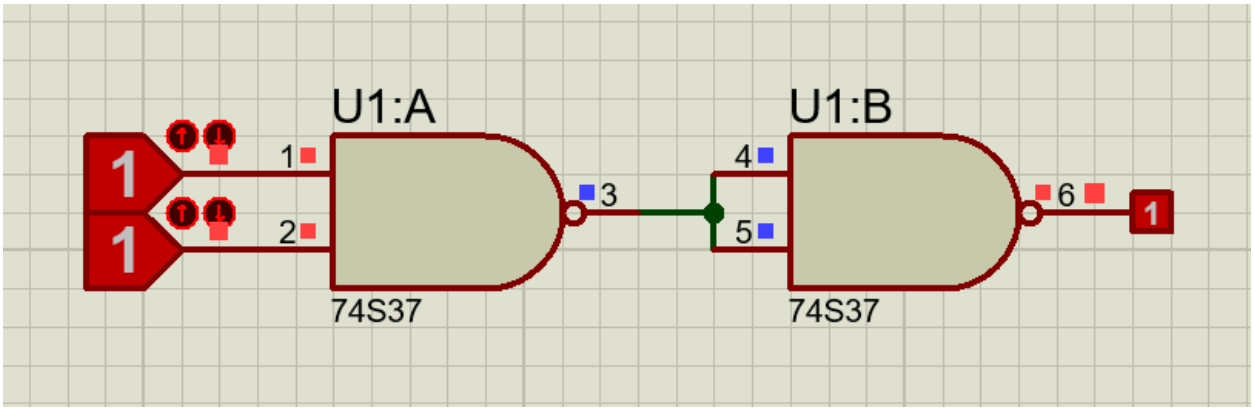

Table:

Input		Output
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

Verification of OR function:

Procedure:

- Connect the circuit as shown in the figure.
- Connect +5V to pin 14(Vcc) and Ground pin to 7 (GND) of the IC.
- By setting the switches to 1 and 0, verify that the output (F) of the circuit conforms to that of a OR gate. Record your observations in a table.

Figure:

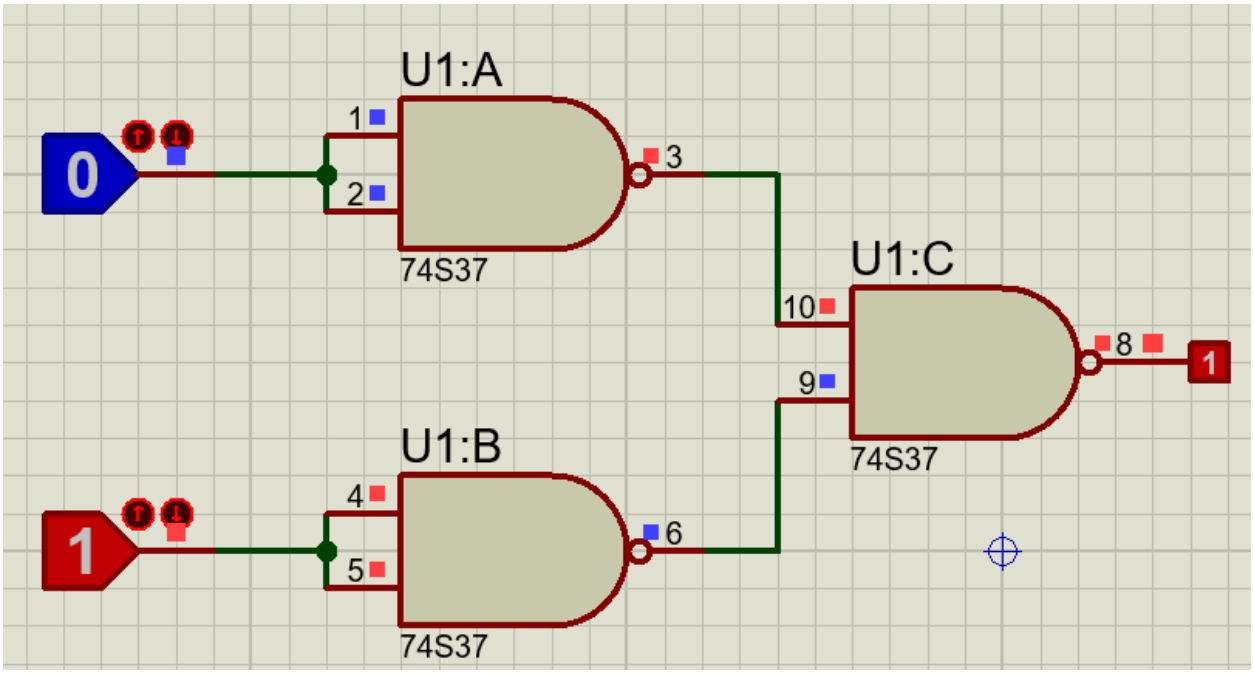

Table:

Input		Output
A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

Verification of XOR function:

Procedure:

- Connect the circuit as shown in the figure.
- Connect +5V to pin 14(Vcc) and Ground pin to 7 (GND) of the IC.
- By setting the switches to 1 and 0, verify that the output (F) of the circuit conforms to that of a XOR gate. Record your observations in a table.

Figure:

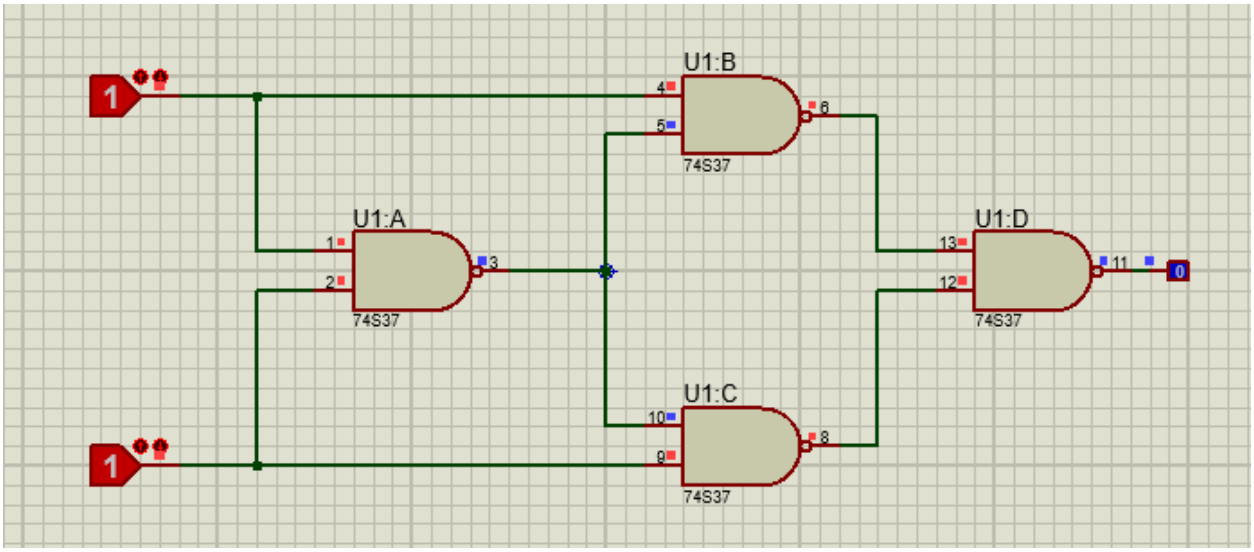

Table:

Input		Output
A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

Verification of XNOR function:

Procedure:

- Connect the circuit as shown in the figure.
- Connect +5V to pin 14(Vcc) and Ground pin to 7 (GND) of the IC.
- By setting the switches to 1 and 0, verify that the output (F) of the circuit conforms to that of a XNOR gate. Record your observations in a table.

Figure:

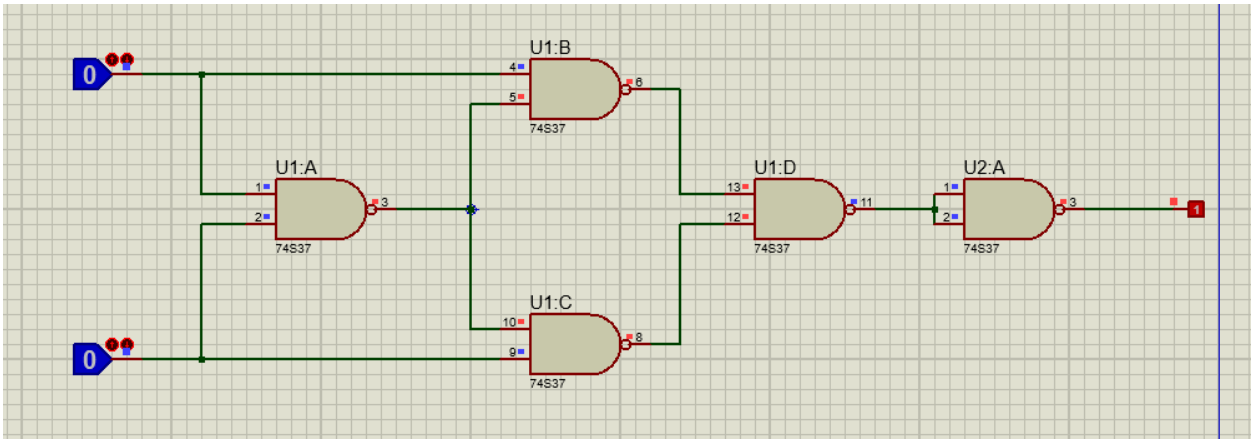

Table:

Input		Output
A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

Lab Tasks:

Part 2:

Implement Any Logic Expression Using Only NOR Gates:

Procedure:

- Simulate NOT, AND, OR, XOR and XNOR gates in Proteus software by using NOR gates. Verify their truth tables.
- Insert IC on the trainer's breadboard.
- Use any one or more of the NOR gates of the IC for this experiment.
- One or more Logic switches of the trainer can be used as input for the NOR gate.
- For output indication, connect the output pin of the circuit to any one of the LED's of the trainer.

Verification of NOT function:

Procedure:

- Connect the circuit as shown in the figure.
- Connect +5V to pin 14(Vcc) and Ground pin to 7 (GND) of the IC.

- By setting the switches to 1 and 0, verify that the output (F) of the circuit conforms to that of a NOT gate. Record your observations in a table.

Figure:

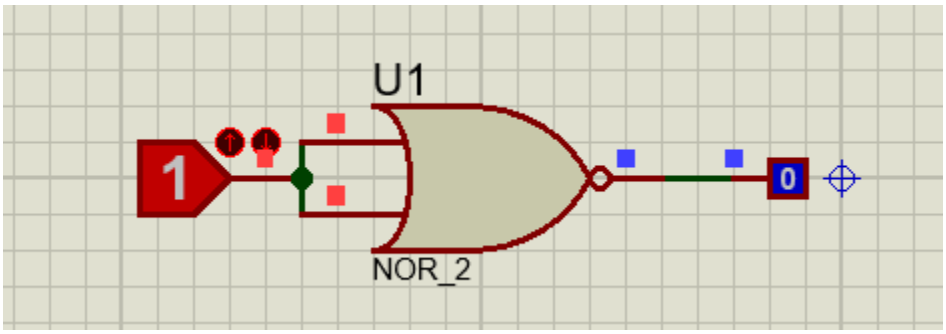

Table:

Input	Output
A	F
0	1
1	0

Verification of AND function:

Procedure

- Connect the circuit as shown in the figure.
- Connect +5V to pin 14(Vcc) and Ground pin to 7 (GND) of the IC.

- By setting the switches to 1 and 0, verify that the output (F) of the circuit conforms to that of a AND gate. Record your observations in a table.

Figure:

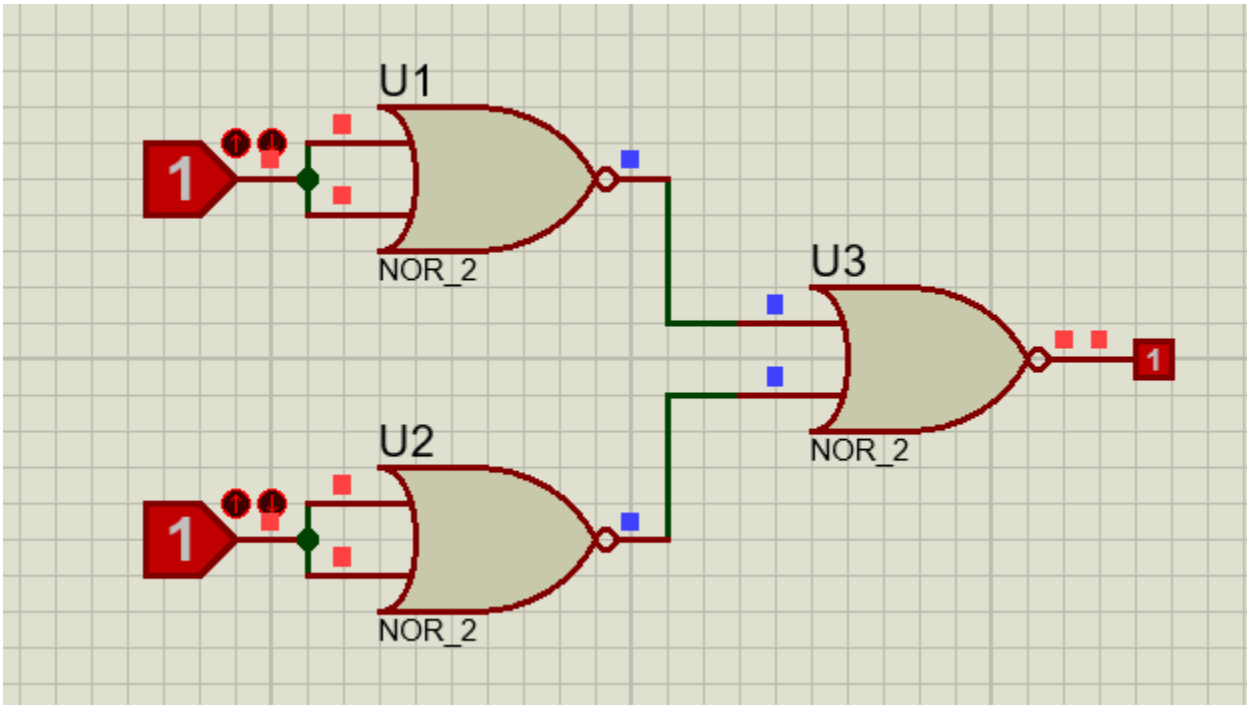

Table:

Input		Output
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

Verification of OR function:

Procedure:

- Connect the circuit as shown in the figure.
- Connect +5V to pin 14(Vcc) and Ground pin to 7 (GND) of the IC.

- By setting the switches to 1 and 0, verify that the output (F) of the circuit conforms to that of a OR gate. Record your observations in a table.

Figure:

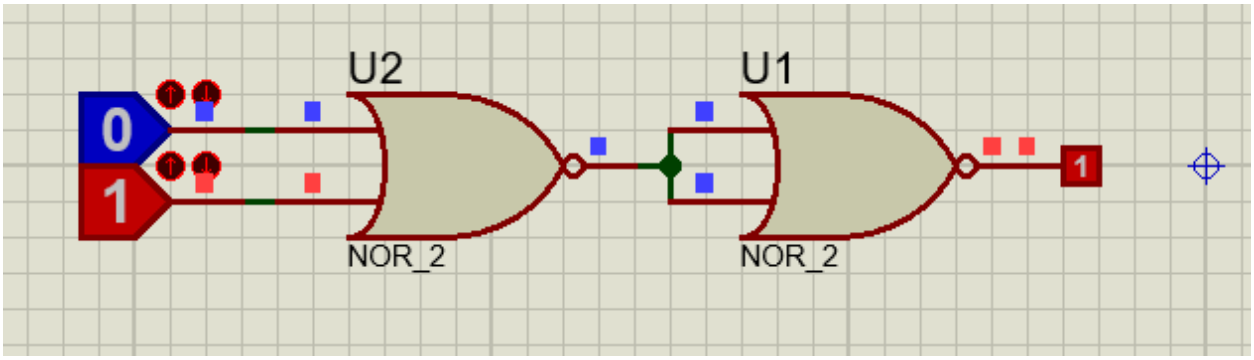

Table:

Input		Output
A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

Verification of XOR function:

Procedure:

- Connect the circuit as shown in the figure.
- Connect +5V to pin 14(Vcc) and Ground pin to 7 (GND) of the IC.

- By setting the switches to 1 and 0, verify that the output (F) of the circuit conforms to that of a XOR gate. Record your observations in a table.

Figure:

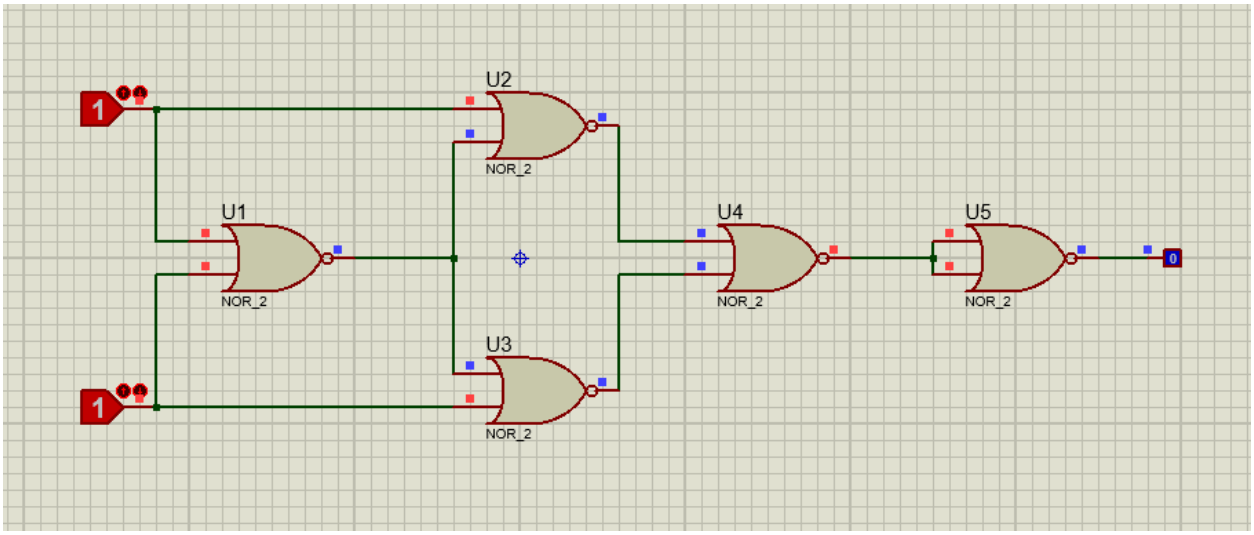

Table:

Input		Output
A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

Verification of XNOR function:

Procedure:

- Connect the circuit as shown in the figure.

- Connect +5V to pin 14(Vcc) and Ground pin to 7 (GND) of the IC.
- By setting the switches to 1 and 0, verify that the output (F) of the circuit conforms to that of a XNOR gate. Record your observations in a table.

Figure:

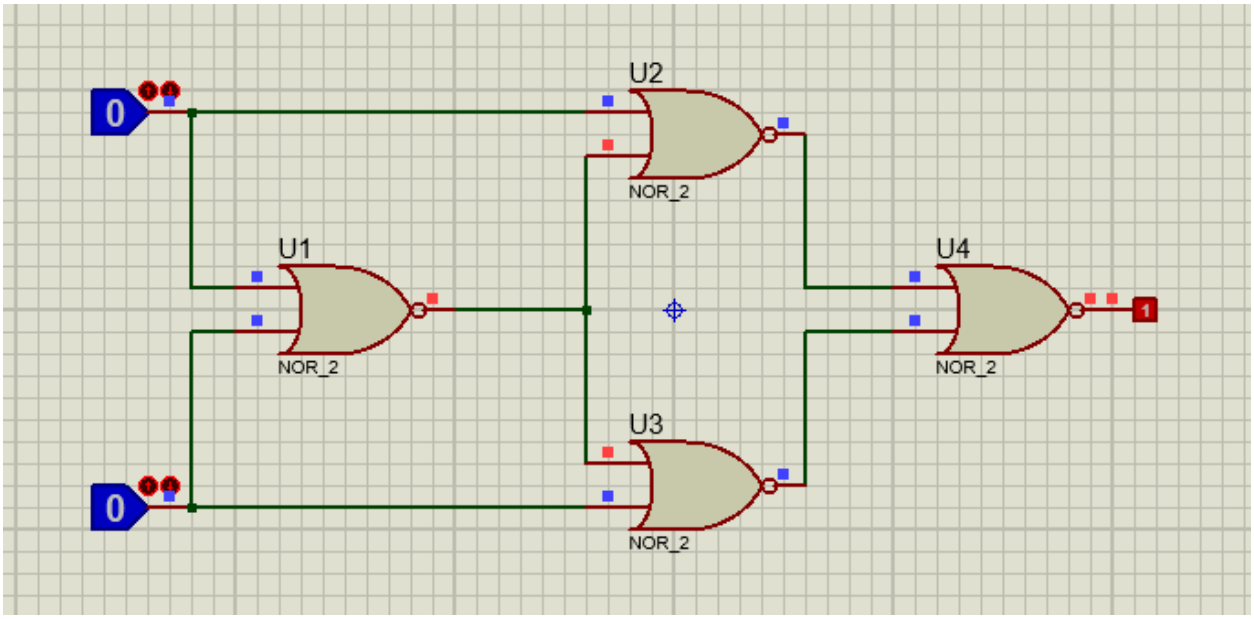

Table:

Input		Output
A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

Critical Analysis

In this lab we used NAND gate to produce other gates such as AND using NAND, NOT using NAND, OR using NAND, XOR using NAND and XNOR using NAND. Basically in this lab we performed different circuits options to make the particular gate using NAND gate. During the process we used different equipments such as bread board, and particular IC's as well as power supply was necessary

during this lab. After the verification by NAND gate we were to implement verification of any logic expressions using only NOR gate with the same equipment we used during the task 01. After all these hardware work then comes software part we verified both of tasks using PROTEUS with the help of some basic commands such as Logic state and Logic Prob(big) and attached the verified screenshots in the lab reports.