CS-382 Computer Architecture and Organization Fall 2022

Lab 9 · Let's Make Some Memories ☺

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1 Task 1: Make Memory

In this lab we will focus on random access memory (RAM) in Logisim-Evolution, and more specifically, we will create an instruction memory with program counter (PC).

On the left panel, choose "Memory", and you will see both RAM and ROM, and please choose RAM. A typical RAM is shown as in the follow picture. Note if your RAM looks different, go to attribute panel, and choose "Logisim-Evolution" for Appearance.

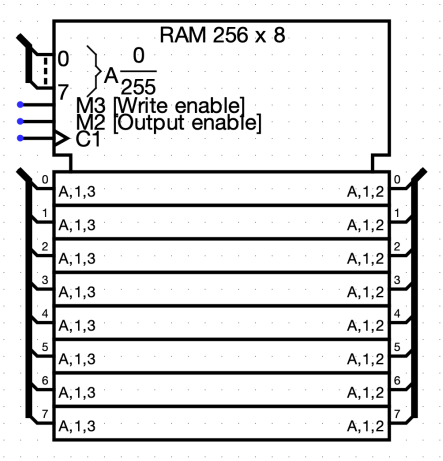

Figure 1

By default, this RAM can store 255 bytes, so it has 255 unique addresses, and therefore the address bus is 8 bit wide (why?). The address bus is at the left top corner with number "0" and "7". For port M3, please connect it with a constant 0, and for M2 with a constant 1. Also, please connect it with a clock for port C1.

The left is the data bus for write, and right for read. In this lab, you only need to connect the read port with an 8-bit wide output pin to show the content we read from the RAM, while leaving write port unattached.

1.1 Loading Content to RAM

Once you're done with the steps above, you can start simulation, and you'll see the RAM has data in it, as in Figure 2. There you see on the left these are addresses in hexadecimal, and each row has six bytes. If you're in the simulation mode, you can click on every byte, and type the data you want to store there. However, if you reset the simulation, all the data will be gone. A good idea is to store the memory data into a text file, called **image file**. To do this, right click the memory, and choose "Save Image", and store it somewhere. Next time when you want to load them into the RAM, just right click and choose "Load Image".

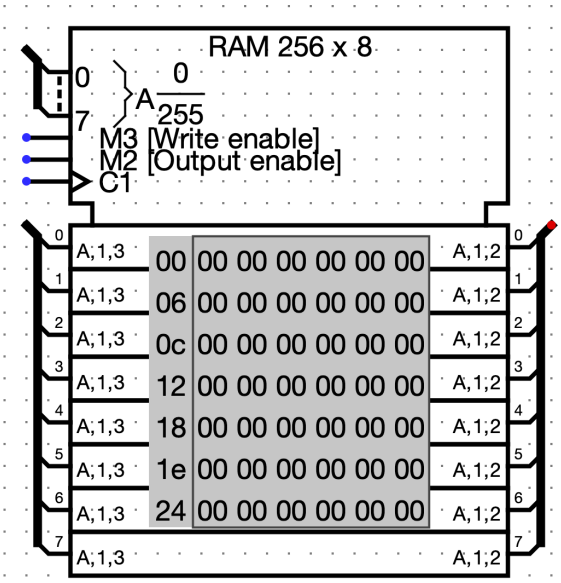

Figure 2

1.2 Automatic Reader

In this task, we will want to read every byte at a constant speed from RAM. Therefore, we need a register that connects to the address bus of the RAM and can update itself. Let's call that PC ☺.

Consider for each clock cycle, we need to read from the memory, and also update PC, so RAM and PC should be controlled by the same clock. Also, because we want to advance the memory address by one byte, we need to connect the PC with an adder, and add constant 1 as the other input of the adder.

In sum, you need the following components:

- Clock;

- Adder;
- Register;
- Output pin;
- RAM;
- Constants.

All of them can be found in the left panel of Logisim-Evolution.

2 Requirements

- You must write your name and pledge in the `.circ` file that contains the RAM;
- You must label the register and the output pin;
- You must create and save an image file that can be loaded into your RAM, starting from address `0x0` to `0x5` (6 bytes in total). Any valid data is fine;
- Once simulation started, your circuit must be able to read one byte at a time automatically, shown in the output pin.

Deliverable

One `.circ` files and one image file.