Lab 2 Report

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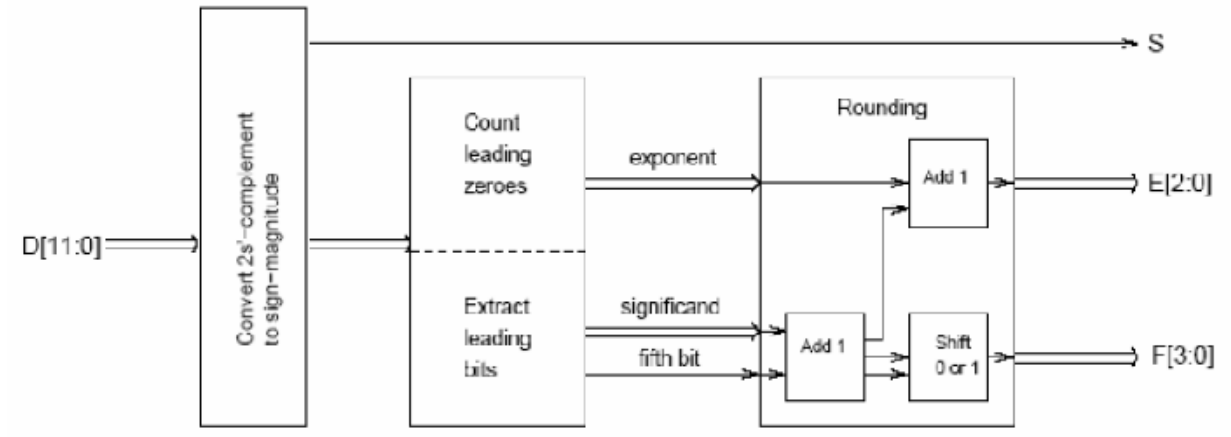
Introduction and requirement: Summarize background information about the lab and the detailed design requirements. It's very important to make sure you are designing the right thing before starting.

In this lab, we designed and tested a combinational circuit that converts a 12-bit linear encoding of an analog signal into a compounded 8-bit Floating Point (FP) Representation. In the 8-bit FP representation, the most significant bit is the sign, the next 3 bits are the exponent, and the last 4 bits are the significand.

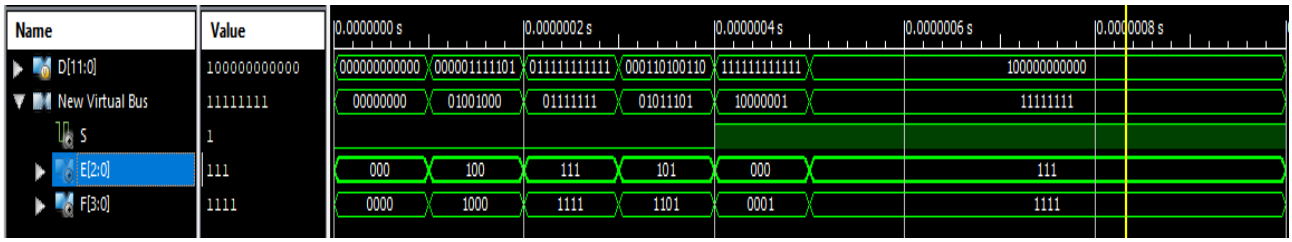
Design description: Document the design aspects including the basic description of the design, modular architecture, interactions among the modules, and interface of each major module. You should include schematics for the system architecture. You can also include figures for state machines and Verilog code when needed.

The first step is for us to convert the 2's complement to sign magnitude and obtain the sign bit, which is done in the signMagn task. Within the parse task, we count the number of leading 0's to determine the exponent, and we take the first 4 bits after the last leading 0 and store it as the significand. We also take the 5th bit after the last leading 0 to determine whether we need to round up or not. Within the rounding task, we create a register with the bit width 1 larger than the significand and copy the significand into it, and if this 5th bit is 1 (meaning we should round up), we add 1 to the new register, and then check if it overflowed by seeing if the most significant bit is 1. If it did overflow, we copy the first 4 bits of the new register to the output and add 1 to the exponent. Similarly, we check if the exponent overflows and output the largest possible floating point value in that case.



Simulation documentation: Document all the simulation efforts (what requirements are tested and what the test cases are), document bugs found during simulation, and provide simulation waveforms.

The simulation converted the numbers [0, 125, 2047, 422, -1, -2048] from 12-bit signed representation to the 8-bit FP representation. Below is a picture of the simulation waveform. One bug we found because of the waveform was that we assigned the sign bit output to our significand by accident.



Conclusion: Summary of the design. Difficulties you encountered, and how you dealt with them. General suggestions for improving the lab, if any.

In this lab, we designed and tested a combinational circuit that converts a 12-bit linear encoding of an analog signal into a compounded 8-bit Floating Point (FP) Representation. We implemented 3 tasks, one to convert the 2's complement to sign magnitude and obtain the sign bit, one to obtain the significand, exponent, and 5^{th} bit based on the number of leading 0's, and one more for rounding. We encountered difficulty with navigating Verilog (we are not big fans). No general suggestions for improving the lab (perhaps an AC in the room would be nice).