1. **Introduction and requirement (10%). Summarize background information about  
   the lab and the detailed design requirements. It’s very important to make sure you  
   are designing the right thing before starting.**

In this lab, we are designing a stopwatch circuit and implementing it on the Nexys™3 Spartan-6 FPGA Board. The digits of the stopwatch that we implement will be displayed on the on-board seven segment display. There will be 2 inputs that control the time stored, SEL and ADJ. The SEL input determines whether we are adjusting seconds or minutes, and the ADJ determines whether we are in normal mode or adjustment mode. There will also be a button for resetting the time, and another for pausing and resuming the time.

1. **Design description (15%). Document the design aspects including the basic  
   description of the design, modular architecture, interactions among the modules,  
   and interface of each major module. You should include schematics for the system**

**architecture. You can also include figures for state machines and Verilog code  
when needed**.

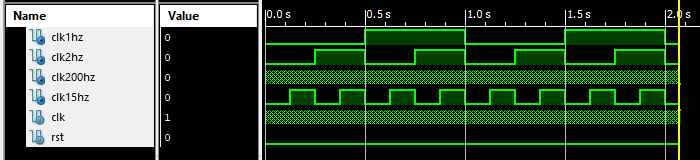
We have implemented multiple modules that all work together. The debouncer module handles the debouncing of all the signals. The toggle module takes a continuous signal as input and transforms it into a toggle. The clock module generates the necessary clocks, which are 1hz, 2hz, 4hz, and 700hz (though the names in code are 1, 2, 15, and 200hz respectively). The watch module handles the processing of the entire stopwatch by taking the clocks, pause and reset buttons, select and set as inputs, and performing the necessary operations based on what buttons are selected on the board and outputs 4 signals: seconds1, seconds2, minutes 1 and minutes 2. Finally, the displayDriver module displays the correct numbers on the stopwatch by enabling the correct segments on the seven segment display.

1. **Simulation documentation (10%). Document all the simulation efforts (what**

**requirements are tested and what the test cases are), document bugs found during**

**simulation, and provide simulation waveforms.**

We used the test bench to simulate the timing of the internal clocks.



The rest of the testing was done on the board. We found and fixed multiple timing bugs.

1. **Conclusion (5%). Summary of the design. Difficulties you encountered, and how**

**you dealt with them. General suggestions for improving the lab, if any.**

The stopwatch that was designed is displayed on the seven segment display on the Nexys™3 Spartan-6 FPGA Board, and has multiple functionalities. We are able to reset the stopwatch, pause and resume the time, and also set the seconds or minutes at 2hz when in adjustment mode. One of the biggest issues we encountered was the debouncing, as it was causing the buttons to not work properly.