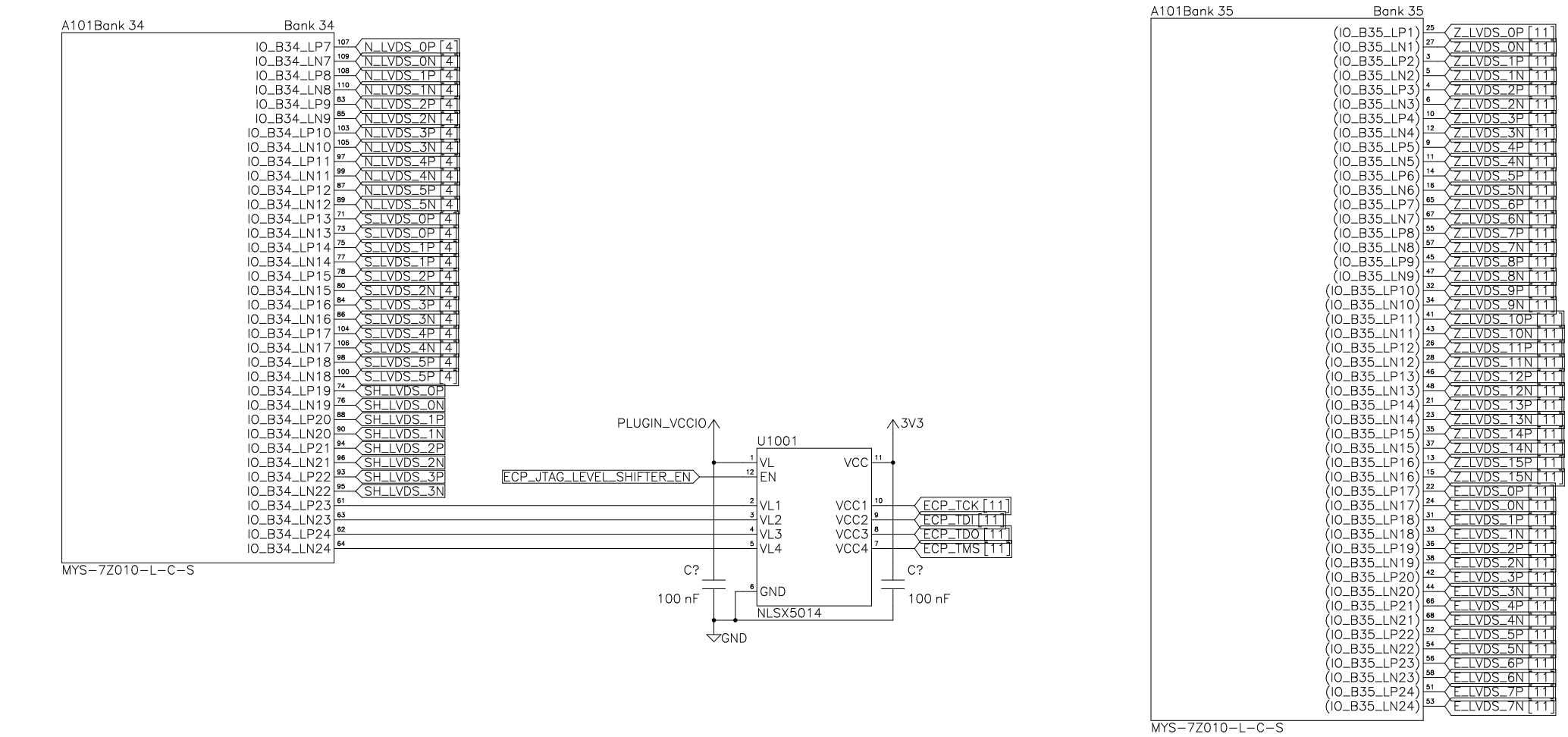
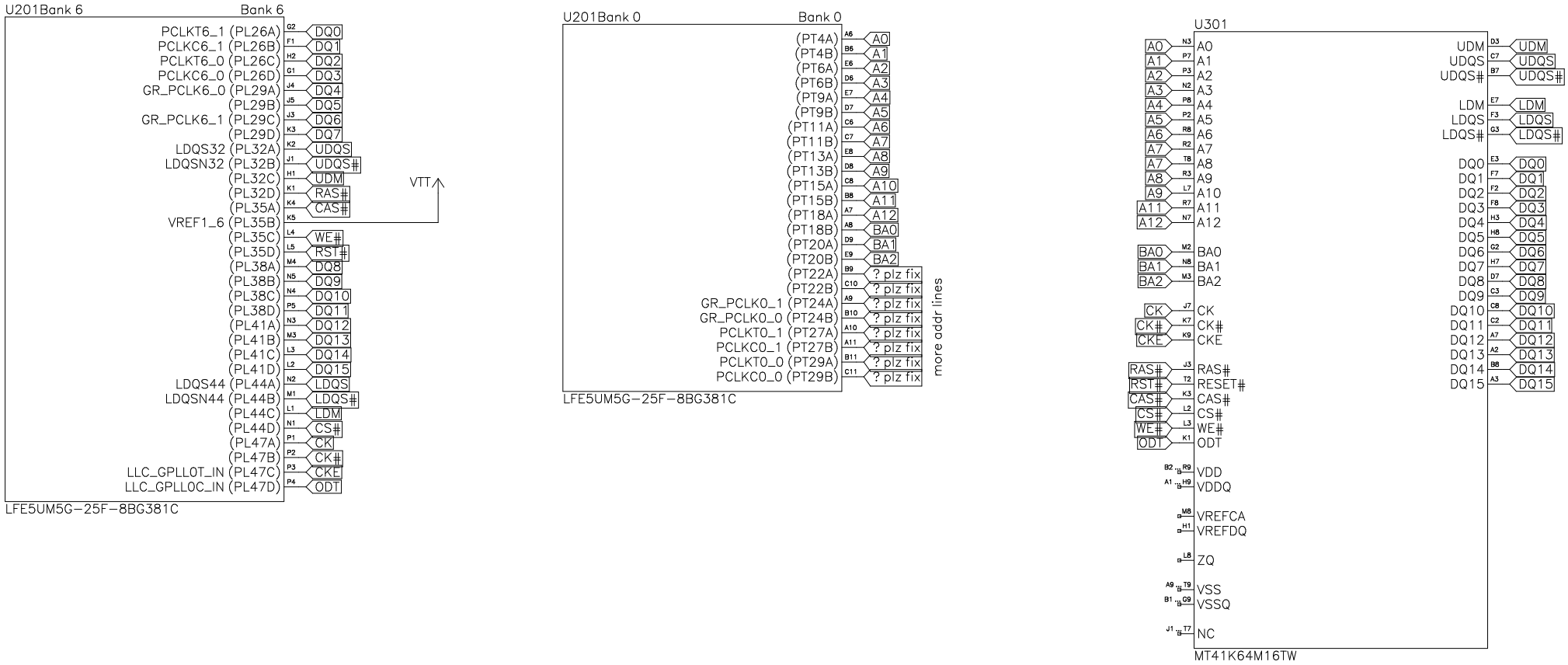


Sheet: zturn lite	Number: 1/11
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	
Date: 20200324	open source hardware

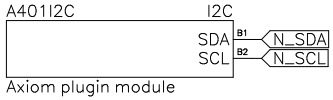
Sheet ecp	Number 2/11
Project Axiom micro rev3	Revision 0
Drawn by anuejn & vup	
License CERN-OHL-S V2	open source hardware
Date 20200324	



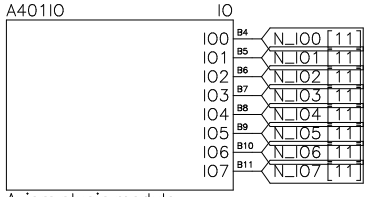
THIS STUFF NEEDS TERMINATION

Sheet: RAM	Number: 3/11
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN–OHL–S V2	open source hardware
Date: 20200324	

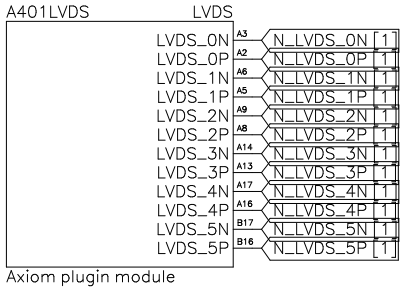
plugin north



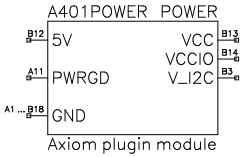
Axiom plugin module



Axiom plugin module

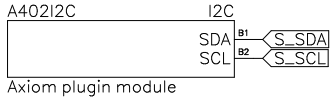


Axiom plugin module

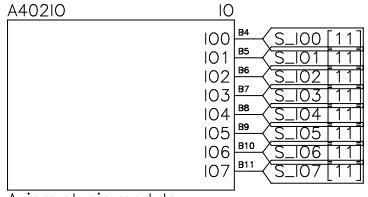


Axiom plugin module

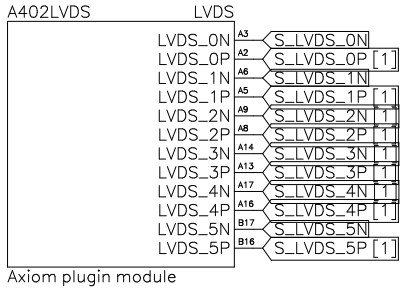
plugin south



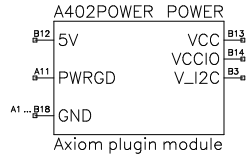
Axiom plugin module



Axiom plugin module



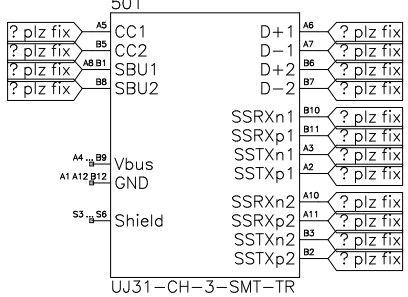
Axiom plugin module

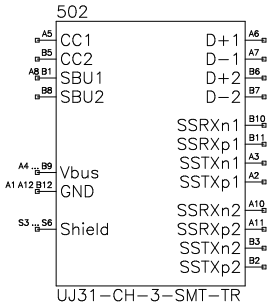


Axiom plugin module

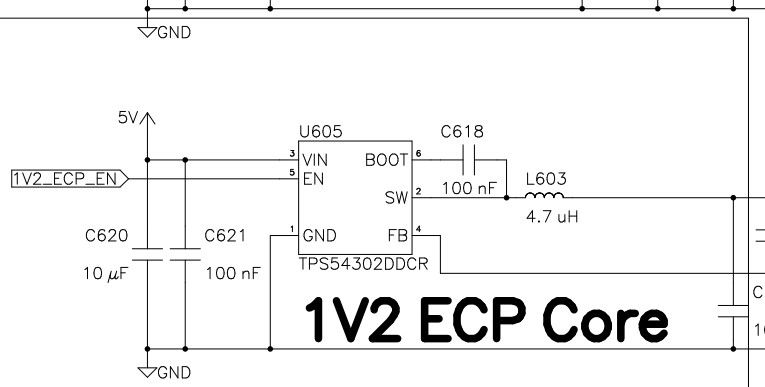
Sheet plugin	Number 4/11
Project Axiom micro rev3	Revision 0
Drawn by anuejn & vup	
License CERN-OHL-S V2	open source hardware
Date 20200324	

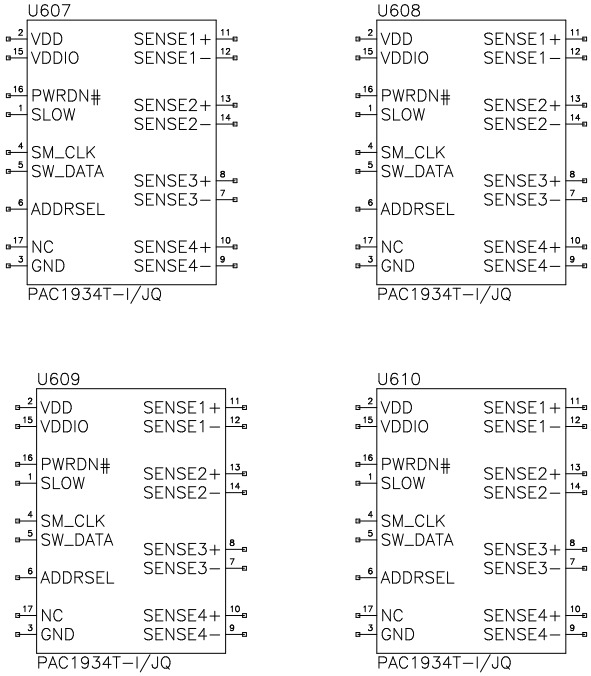
We probably want to be a upwards facing port?
CC1/2 need pullups / pulldowns

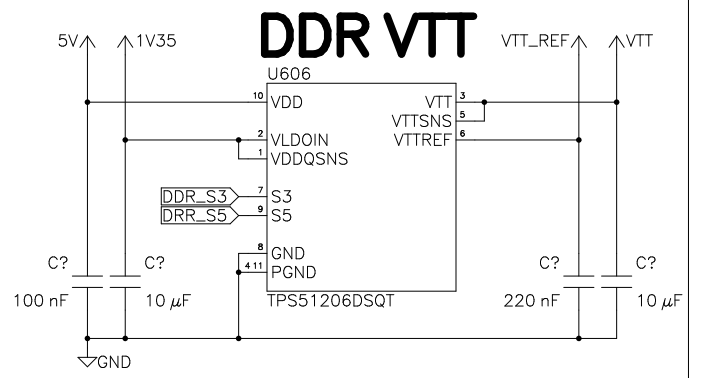




Sheet: USB	Number: 5/11
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN−OHL−S V2	open source hardware
Date: 20200324	

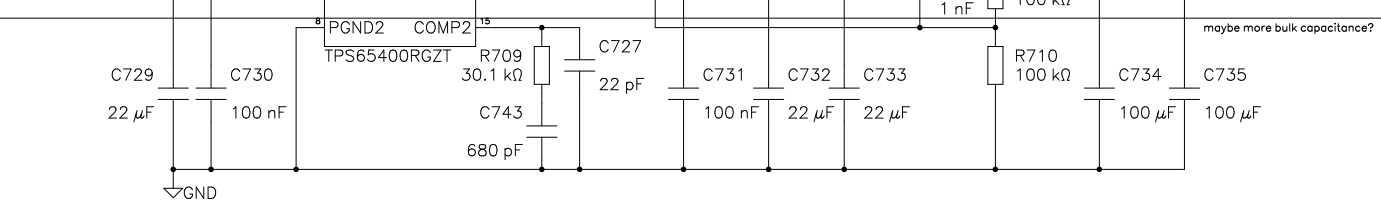


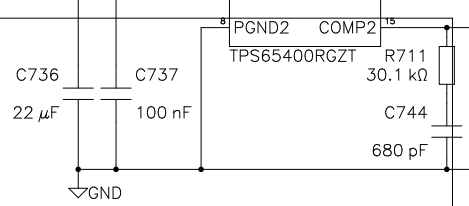




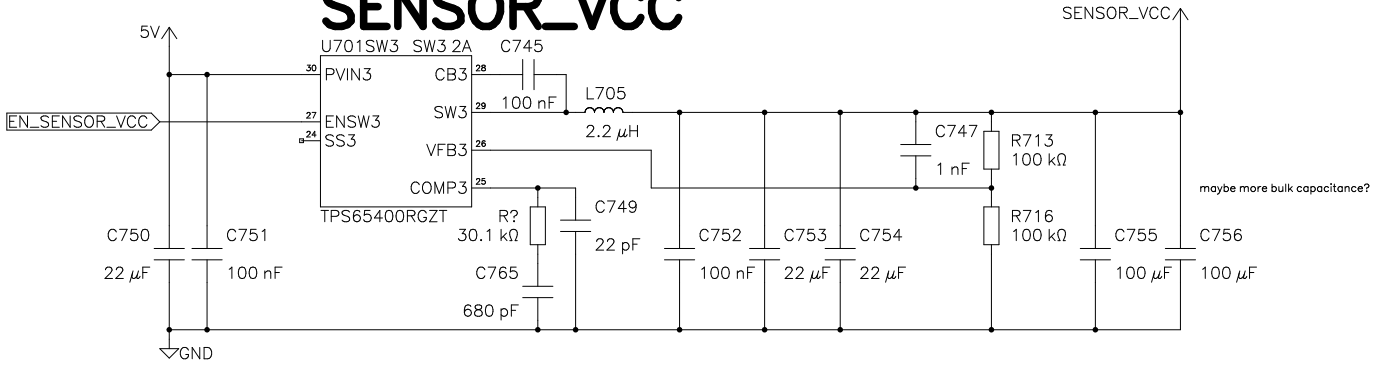
positive terminal of the VTT pin output capacitor(s) as a separate trace from the high current path from VTT. Consider adding a low−pass R−C filter at the VTTSNS pin in case output capacitor(s) is larger than 2 mΩ. The R−C filter time constant should be approx lower than the time constant of the VTT output capacitance and ESR.

Sheet: power fixed	Number: 6/11
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN−OHL−S V2	open source hardware
Date: 20200324	

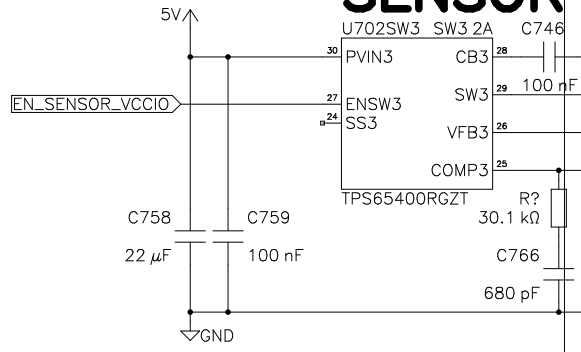




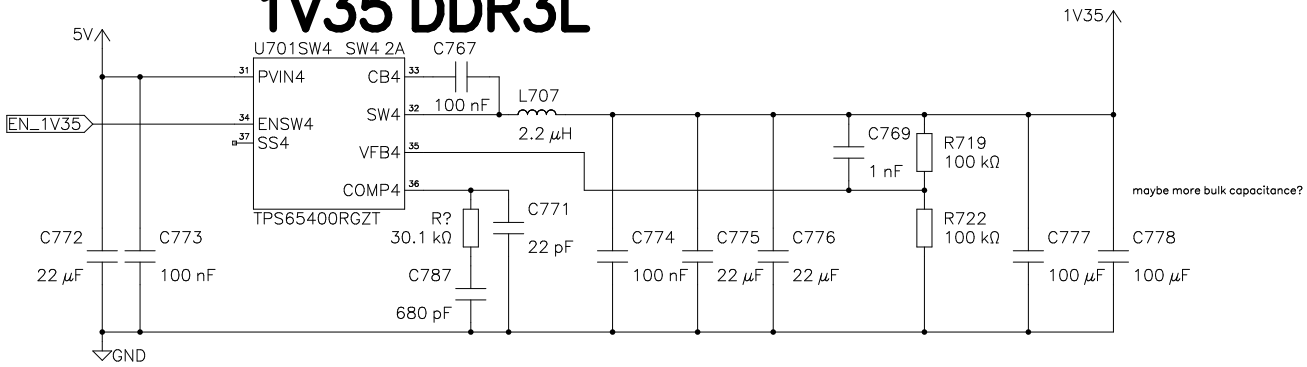
SENSOR_VCC



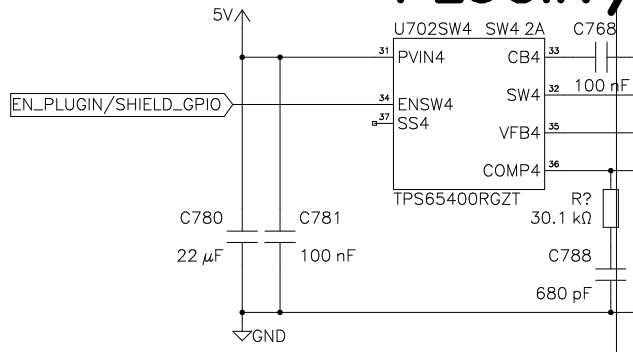
SENSOR

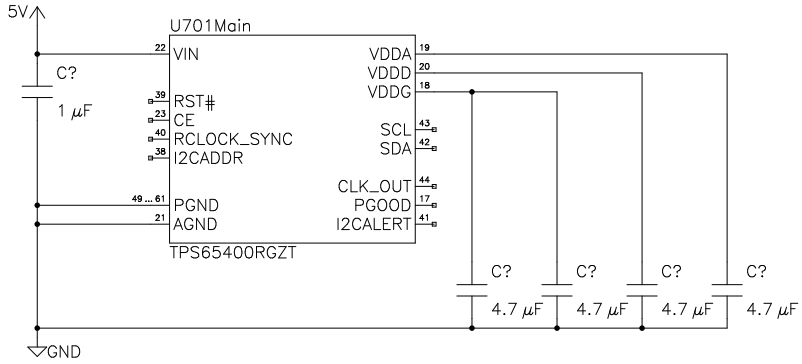


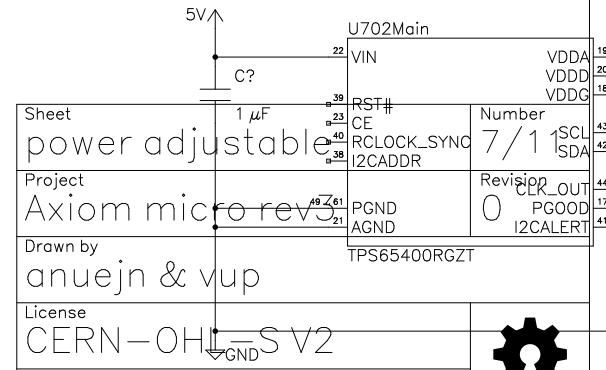
1V35 DDR3L



PLUGIN

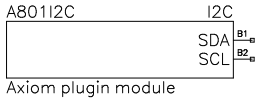


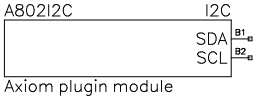


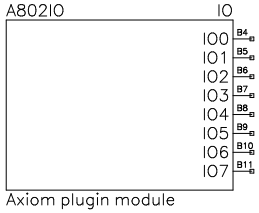


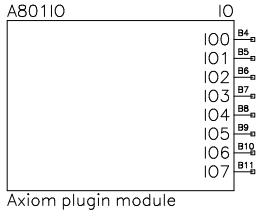
Sheet: power adjustable	Number: 7/11
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	
Date: 20200324	

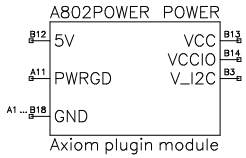
open source hardware

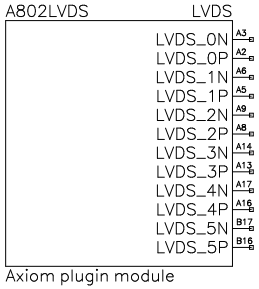


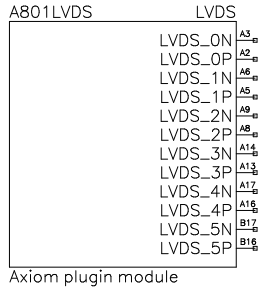


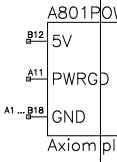






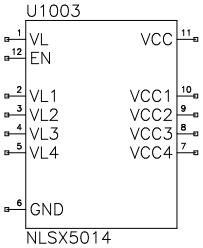


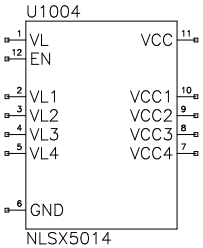


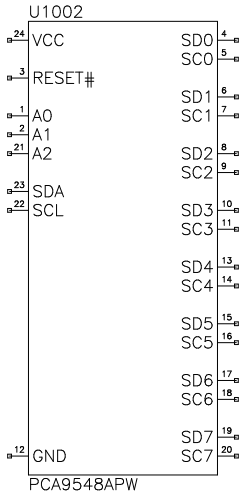


Sheet image_sensor	Number 8/11
Project Axiom micro rev3	Revision 0
Drawn by anuejn & vup	
License CERN-OHL-S V2	open source hardware
Date 20200324	

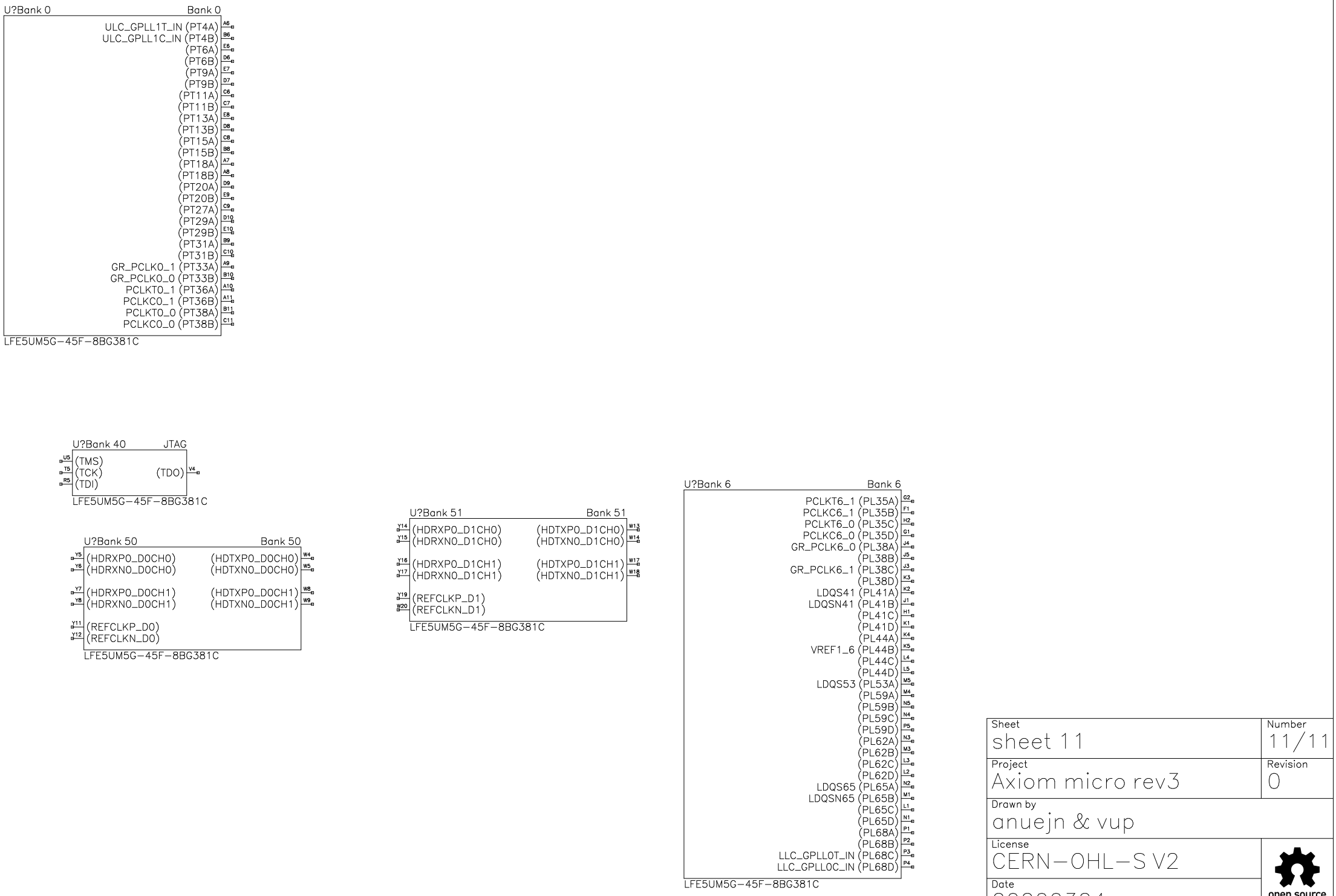
Sheet shield	Number 9/11
Project Axiom micro rev3	Revision 0
Drawn by anuejn & vup	
License CERN-OHL-S V2	open source hardware
Date 20200324	







Sheet misc	Number 10/11
Project Axiom micro rev3	Revision 0
Drawn by anuejn & vup	
License CERN-OHL-S V2	open source hardware
Date 20200324	


U?Bank 0
Bank 0
ULC_GPLL1T_IN (PT4A) A6
ULC_GPLL1C_IN (PT4B) B6
(PT6A) E6
(PT6B) D6
(PT9A) E7
(PT9B) D7
(PT11A) C6
(PT11B) C7
(PT13A) E8
(PT13B) D8
(PT15A) C8
(PT15B) B8
(PT18A) A7
(PT18B) A8
(PT20A) D9
(PT20B) E9
(PT27A) C9
(PT29A) D10
(PT29B) E10
(PT31A) B9
(PT31B) C10
GR_PCLK0_1 (PT33A) A9
GR_PCLK0_0 (PT33B) B10
PCLKT0_1 (PT36A) A10
PCLKC0_1 (PT36B) A11
PCLKT0_0 (PT38A) B11
PCLKC0_0 (PT38B) C11
LFE5UM5G-45F-8BG381C
U?Bank 40
JTAG
U5 (TMS)
T5 (TCK)
R5 (TDI)
(TDO) V4
LFE5UM5G-45F-8BG381C
U?Bank 50
Bank 50
Y5 (HDRXP0_D0CH0)
Y6 (HDRXN0_D0CH0)
(HDTXP0_D0CH0) W4
(HDTXN0_D0CH0) W5
Y7 (HDRXP0_D0CH1)
Y8 (HDRXN0_D0CH1)
(HDTXP0_D0CH1) W8
(HDTXN0_D0CH1) W9
Y11 (REFCLKP_D0)
Y12 (REFCLKN_D0)
LFE5UM5G-45F-8BG381C
U?Bank 51
Bank 51
Y14 (HDRXP0_D1CH0)
Y15 (HDRXN0_D1CH0)
(HDTXP0_D1CH0) W13
(HDTXN0_D1CH0) W14
Y16 (HDRXP0_D1CH1)
Y17 (HDRXN0_D1CH1)
(HDTXP0_D1CH1) W17
(HDTXN0_D1CH1) W18
Y19 (REFCLKP_D1)
W20 (REFCLKN_D1)
LFE5UM5G-45F-8BG381C
U?Bank 6
Bank 6
PCLKT6_1 (PL35A) G2
PCLKC6_1 (PL35B) F1
PCLKT6_0 (PL35C) H2
PCLKC6_0 (PL35D) G1
GR_PCLK6_0 (PL38A) J4
(PL38B) J5
GR_PCLK6_1 (PL38C) J3
(PL38D) K3
LDQS41 (PL41A) K2
LDQSN41 (PL41B) J1
(PL41C) H1
(PL41D) K1
(PL44A) K4
VREF1_6 (PL44B) K5
(PL44C) L4
(PL44D) L5
LDQS53 (PL53A) M5
(PL59A) M4
(PL59B) N5
(PL59C) N4
(PL59D) P5
(PL62A) N3
(PL62B) M3
(PL62C) L3
(PL62D) L2
LDQS65 (PL65A) N2
LDQSN65 (PL65B) M1
(PL65C) L1
(PL65D) N1
(PL68A) P1
(PL68B) P2
LLC_GPLL0T_IN (PL68C) P3
LLC_GPLL0C_IN (PL68D) P4
LFE5UM5G-45F-8BG381C
Sheet
sheet 11
Number
11/11
Project
Axiom micro rev3
Revision
0
Drawn by
anuejn & vup
License
CERN-OHL-S V2
Date
20200324
open source hardware