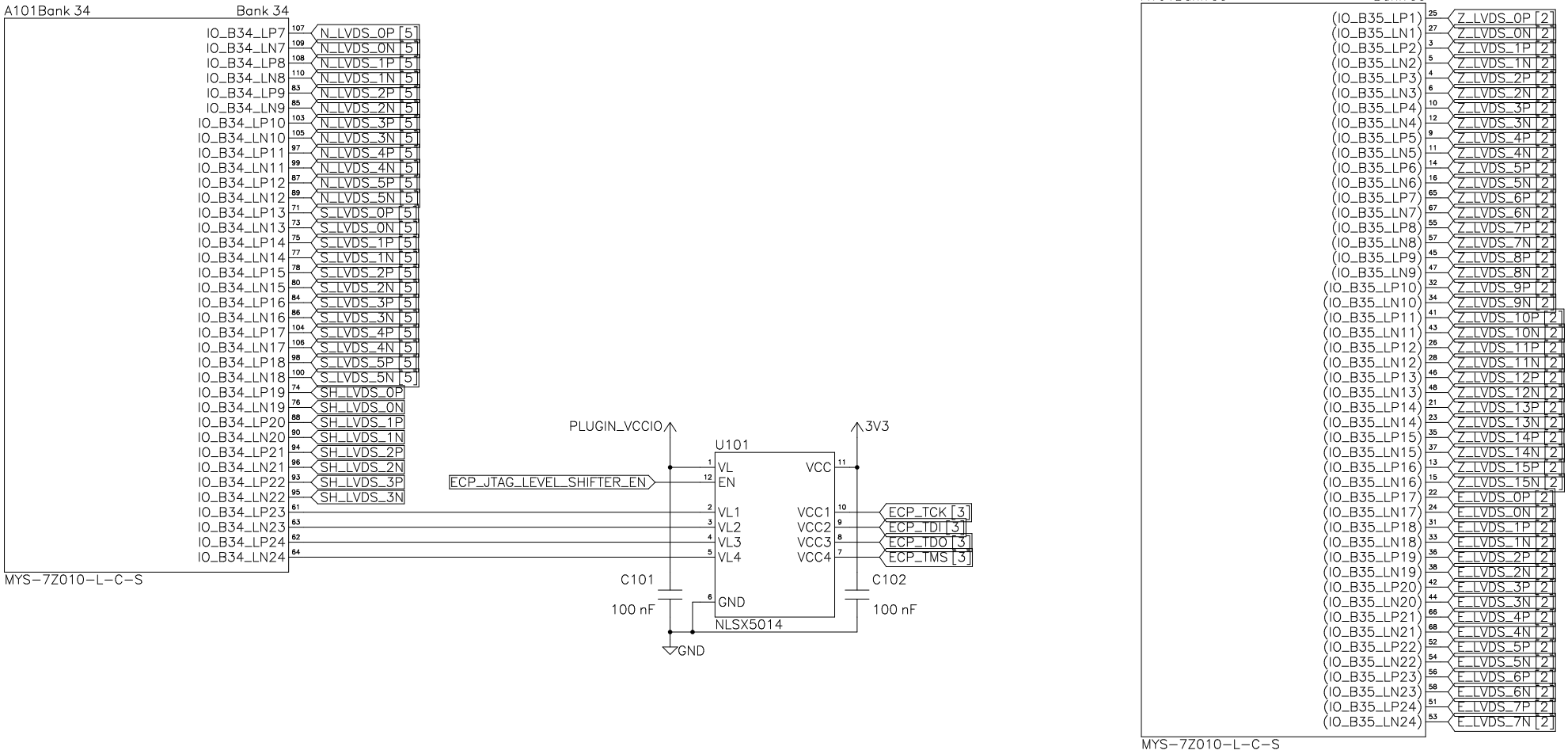
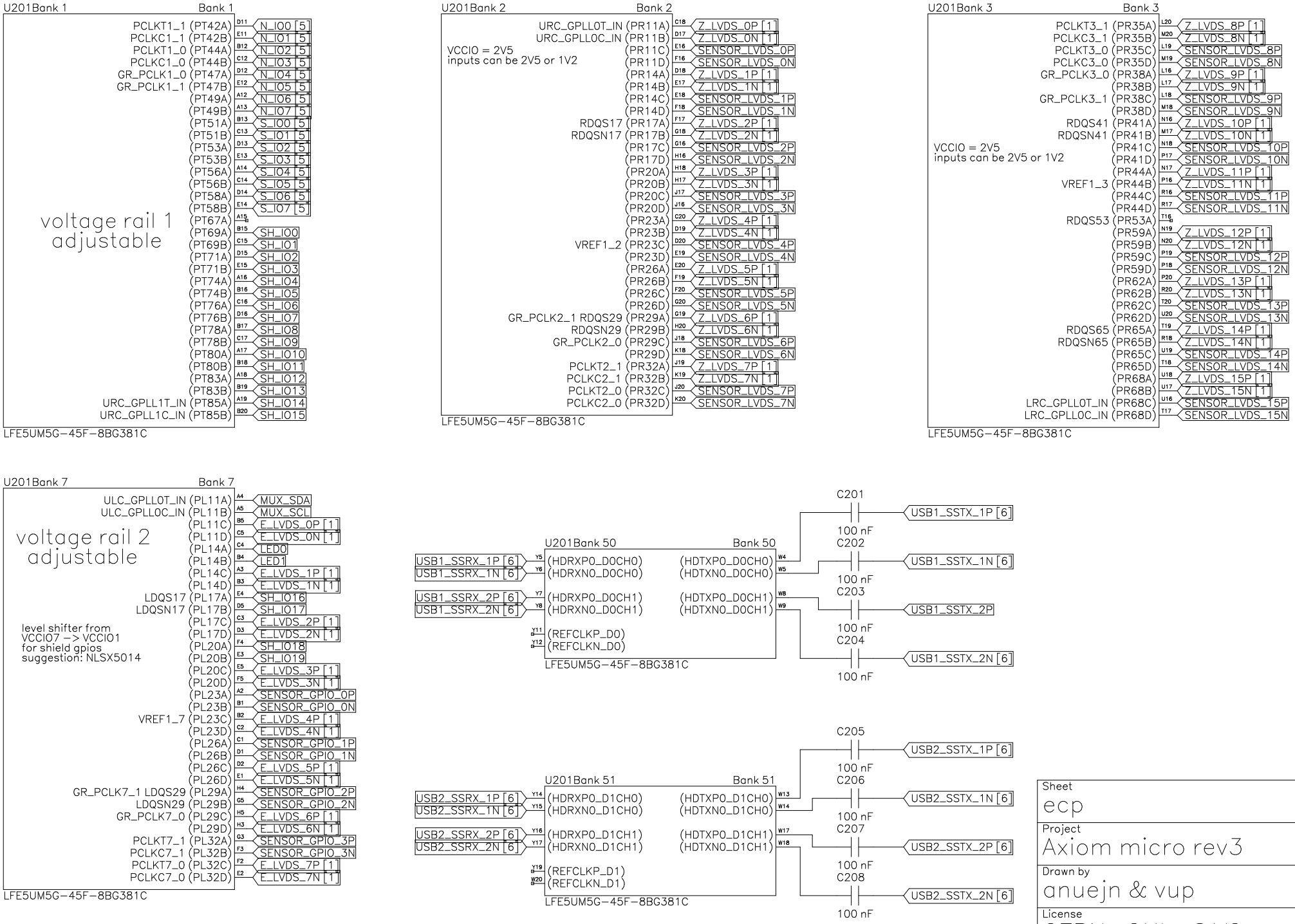


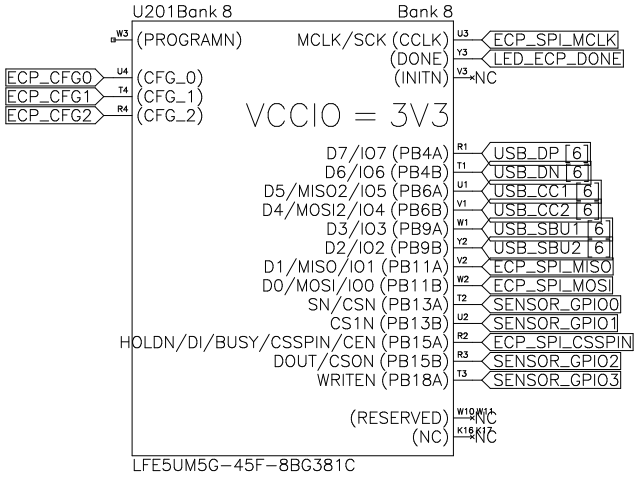
Sheet: zturn lite	Number: 1/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	
Date: 20200324	open source hardware

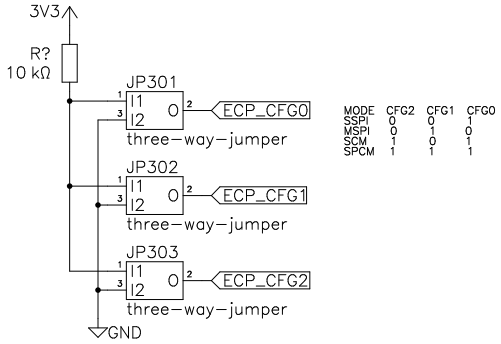

U201Bank 1
Bank 1
PCLKT1_1 (PT42A)
PCLKC1_1 (PT42B)
PCLKT1_0 (PT44A)
PCLKC1_0 (PT44B)
GR_PCLK1_0 (PT47A)
GR_PCLK1_1 (PT47B)
(PT49A)
(PT49B)
(PT51A)
(PT51B)
(PT53A)
(PT53B)
(PT56A)
(PT56B)
(PT58A)
(PT58B)
(PT67A)
(PT69A)
(PT69B)
(PT71A)
(PT71B)
(PT74A)
(PT74B)
(PT76A)
(PT76B)
(PT78A)
(PT78B)
(PT80A)
(PT80B)
(PT83A)
(PT83B)
URC_GPLL1T_IN (PT85A)
URC_GPLL1C_IN (PT85B)
N_IO0 [5]
N_IO1 [5]
N_IO2 [5]
N_IO3 [5]
N_IO4 [5]
N_IO5 [5]
N_IO6 [5]
N_IO7 [5]
S_IO0 [5]
S_IO1 [5]
S_IO2 [5]
S_IO3 [5]
S_IO4 [5]
S_IO5 [5]
S_IO6 [5]
S_IO7 [5]
SH_IO0
SH_IO1
SH_IO2
SH_IO3
SH_IO4
SH_IO5
SH_IO6
SH_IO7
SH_IO8
SH_IO9
SH_IO10
SH_IO11
SH_IO12
SH_IO13
SH_IO14
SH_IO15
voltage rail 1
adjustable
LFE5UM5G-45F-8BG381C
U201Bank 2
Bank 2
URC_GPLL0T_IN (PR11A)
URC_GPLL0C_IN (PR11B)
VCCIO = 2V5
inputs can be 2V5 or 1V2
(PR11C)
(PR11D)
(PR14A)
(PR14B)
(PR14C)
(PR14D)
RDQS17 (PR17A)
RDQSN17 (PR17B)
(PR17C)
(PR17D)
(PR20A)
(PR20B)
(PR20C)
(PR20D)
(PR23A)
(PR23B)
VREF1_2 (PR23C)
(PR23D)
(PR26A)
(PR26B)
(PR26C)
(PR26D)
GR_PCLK2_1 RDQS29 (PR29A)
RDQSN29 (PR29B)
GR_PCLK2_0 (PR29C)
(PR29D)
PCLKT2_1 (PR32A)
PCLKC2_1 (PR32B)
PCLKT2_0 (PR32C)
PCLKC2_0 (PR32D)
Z_LVDS_0P [1]
Z_LVDS_0N [1]
SENSOR_LVDS_0P
SENSOR_LVDS_0N
Z_LVDS_1P [1]
Z_LVDS_1N [1]
SENSOR_LVDS_1P
SENSOR_LVDS_1N
Z_LVDS_2P [1]
Z_LVDS_2N [1]
SENSOR_LVDS_2P
SENSOR_LVDS_2N
Z_LVDS_3P [1]
Z_LVDS_3N [1]
SENSOR_LVDS_3P
SENSOR_LVDS_3N
Z_LVDS_4P [1]
Z_LVDS_4N [1]
SENSOR_LVDS_4P
SENSOR_LVDS_4N
Z_LVDS_5P [1]
Z_LVDS_5N [1]
SENSOR_LVDS_5P
SENSOR_LVDS_5N
Z_LVDS_6P [1]
Z_LVDS_6N [1]
SENSOR_LVDS_6P
SENSOR_LVDS_6N
Z_LVDS_7P [1]
Z_LVDS_7N [1]
SENSOR_LVDS_7P
SENSOR_LVDS_7N
LFE5UM5G-45F-8BG381C
U201Bank 3
Bank 3
PCLKT3_1 (PR35A)
PCLKC3_1 (PR35B)
PCLKT3_0 (PR35C)
PCLKC3_0 (PR35D)
GR_PCLK3_0 (PR38A)
(PR38B)
GR_PCLK3_1 (PR38C)
(PR38D)
RDQS41 (PR41A)
RDQSN41 (PR41B)
VCCIO = 2V5
inputs can be 2V5 or 1V2
(PR41C)
(PR41D)
(PR44A)
VREF1_3 (PR44B)
(PR44C)
(PR44D)
RDQS53 (PR53A)
(PR59A)
(PR59B)
(PR59C)
(PR59D)
(PR62A)
(PR62B)
(PR62C)
(PR62D)
RDQS65 (PR65A)
RDQSN65 (PR65B)
(PR65C)
(PR65D)
(PR68A)
(PR68B)
LRC_GPLL0T_IN (PR68C)
LRC_GPLL0C_IN (PR68D)
Z_LVDS_8P [1]
Z_LVDS_8N [1]
SENSOR_LVDS_8P
SENSOR_LVDS_8N
Z_LVDS_9P [1]
Z_LVDS_9N [1]
SENSOR_LVDS_9P
SENSOR_LVDS_9N
Z_LVDS_10P [1]
Z_LVDS_10N [1]
SENSOR_LVDS_10P
SENSOR_LVDS_10N
Z_LVDS_11P [1]
Z_LVDS_11N [1]
SENSOR_LVDS_11P
SENSOR_LVDS_11N
Z_LVDS_12P [1]
Z_LVDS_12N [1]
SENSOR_LVDS_12P
SENSOR_LVDS_12N
Z_LVDS_13P [1]
Z_LVDS_13N [1]
SENSOR_LVDS_13P
SENSOR_LVDS_13N
Z_LVDS_14P [1]
Z_LVDS_14N [1]
SENSOR_LVDS_14P
SENSOR_LVDS_14N
Z_LVDS_15P [1]
Z_LVDS_15N [1]
SENSOR_LVDS_15P
SENSOR_LVDS_15N
LFE5UM5G-45F-8BG381C
U201Bank 7
Bank 7
ULC_GPLL0T_IN (PL11A)
ULC_GPLL0C_IN (PL11B)
(PL11C)
(PL11D)
(PL14A)
(PL14B)
(PL14C)
(PL14D)
LDQS17 (PL17A)
LDQSN17 (PL17B)
(PL17C)
(PL17D)
(PL20A)
(PL20B)
(PL20C)
(PL20D)
(PL23A)
(PL23B)
VREF1_7 (PL23C)
(PL23D)
(PL26A)
(PL26B)
(PL26C)
(PL26D)
GR_PCLK7_1 LDQS29 (PL29A)
LDQSN29 (PL29B)
GR_PCLK7_0 (PL29C)
(PL29D)
PCLKT7_1 (PL32A)
PCLKC7_1 (PL32B)
PCLKT7_0 (PL32C)
PCLKC7_0 (PL32D)
MUX_SDA
MUX_SCL
E_LVDS_0P [1]
E_LVDS_0N [1]
LED0
LED1
E_LVDS_1P [1]
E_LVDS_1N [1]
SH_IO16
SH_IO17
E_LVDS_2P [1]
E_LVDS_2N [1]
SH_IO18
SH_IO19
E_LVDS_3P [1]
E_LVDS_3N [1]
SENSOR_GPIO_0P
SENSOR_GPIO_0N
E_LVDS_4P [1]
E_LVDS_4N [1]
SENSOR_GPIO_1P
SENSOR_GPIO_1N
E_LVDS_5P [1]
E_LVDS_5N [1]
SENSOR_GPIO_2P
SENSOR_GPIO_2N
E_LVDS_6P [1]
E_LVDS_6N [1]
SENSOR_GPIO_3P
SENSOR_GPIO_3N
E_LVDS_7P [1]
E_LVDS_7N [1]
voltage rail 2
adjustable
level shifter from
VCCIO7 -> VCCIO1
for shield gpios
suggestion: NLSX5014
LFE5UM5G-45F-8BG381C
U201Bank 50
Bank 50
USB1_SSRX_1P [6]
USB1_SSRX_1N [6]
USB1_SSRX_2P [6]
USB1_SSRX_2N [6]
(HDRXP0_D0CH0)
(HDRXN0_D0CH0)
(HDRXP0_D0CH1)
(HDRXN0_D0CH1)
(REFCLKP_D0)
(REFCLKN_D0)
(HDTXP0_D0CH0)
(HDTXN0_D0CH0)
(HDTXP0_D0CH1)
(HDTXN0_D0CH1)
C201
C202
C203
C204
100 nF
USB1_SSTX_1P [6]
USB1_SSTX_1N [6]
USB1_SSTX_2P
USB1_SSTX_2N [6]
LFE5UM5G-45F-8BG381C
U201Bank 51
Bank 51
USB2_SSRX_1P [6]
USB2_SSRX_1N [6]
USB2_SSRX_2P [6]
USB2_SSRX_2N [6]
(HDRXP0_D1CH0)
(HDRXN0_D1CH0)
(HDRXP0_D1CH1)
(HDRXN0_D1CH1)
(REFCLKP_D1)
(REFCLKN_D1)
(HDTXP0_D1CH0)
(HDTXN0_D1CH0)
(HDTXP0_D1CH1)
(HDTXN0_D1CH1)
C205
C206
C207
C208
100 nF
USB2_SSTX_1P [6]
USB2_SSTX_1N [6]
USB2_SSTX_2P [6]
USB2_SSTX_2N [6]
LFE5UM5G-45F-8BG381C
Sheet
ecp
Number
2/12
Project
Axiom micro rev3
Revision
0
Drawn by
anuejn & vup
License
CERN-OHL-S V2
Date
20200324
open source
hardware

PROGRAMN

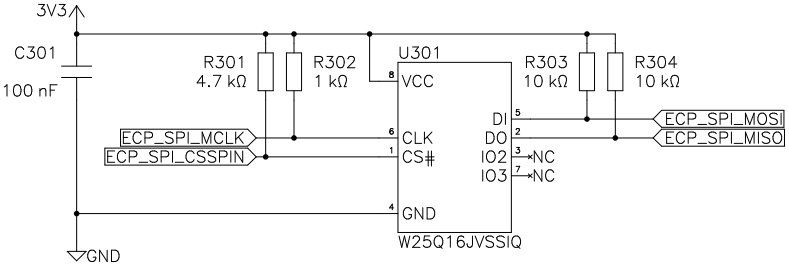
Maybe button for reset,
or somehow connect to trigger reset?

Also has internal pullup during configuration, but maybe we want a external pullup to prevent floating?



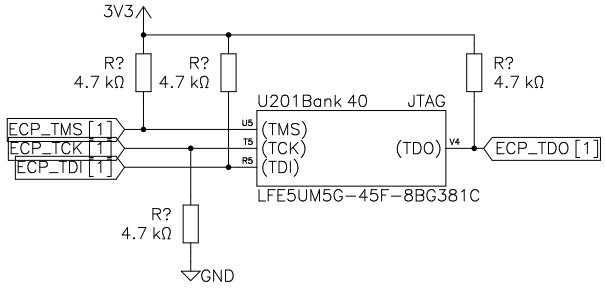


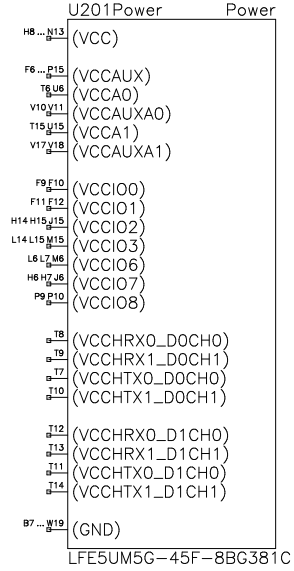
MODE	CFG2	CFG1	CFG0
SSPI	0	0	1
MSPI	0	1	0
SCM	1	0	1
SPCM	1	1	1



The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI operation. When the QE bit is set to a 0 state (factory default for part numbers with ordering options **TIM**), the /WP pin and /HOLD are enabled. When the QE bit is set to a 1(factory default for Quad Enabled part numbers with ordering option **TIQ**), the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled

/CS must track VCC
during VCC Ramp Up/Down

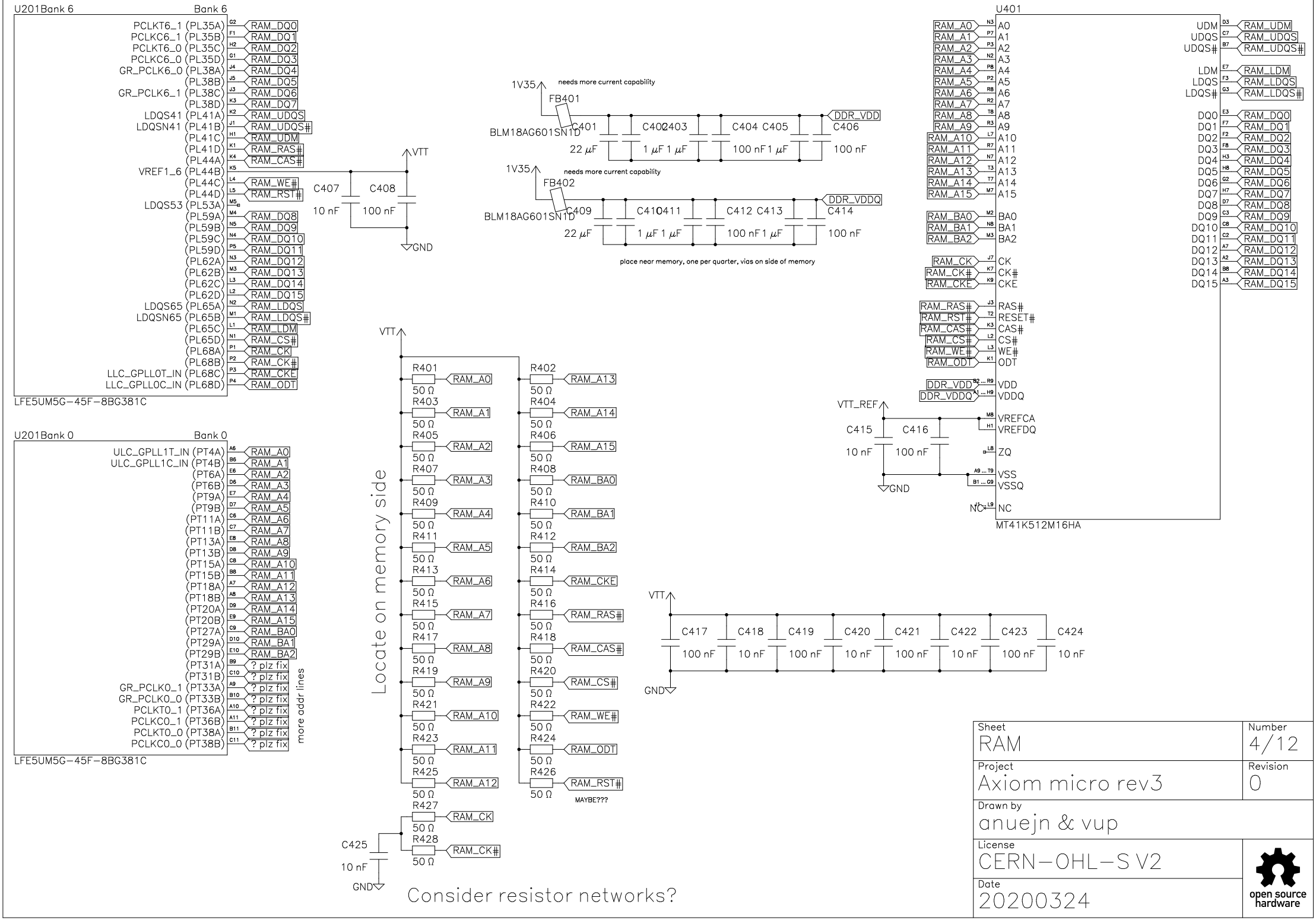




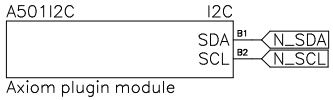
WARNING
ECP5 family datasheet
p.48: Power Supply Ramp rates
for all supplies 0.01-10V/ms

for decoupling see tn1068

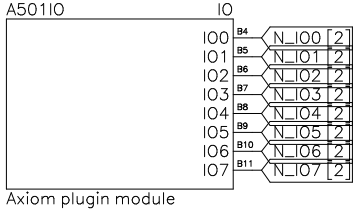
Sheet: ecp config / power	Number: 3/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	
Date: 20200324	open source hardware


U201Bank 6
Bank 6
PCLKT6_1 (PL35A) G2 RAM_DQ0
PCLKC6_1 (PL35B) F1 RAM_DQ1
PCLKT6_0 (PL35C) H2 RAM_DQ2
PCLKC6_0 (PL35D) G1 RAM_DQ3
GR_PCLK6_0 (PL38A) J4 RAM_DQ4
(PL38B) J5 RAM_DQ5
GR_PCLK6_1 (PL38C) J3 RAM_DQ6
(PL38D) K3 RAM_DQ7
LDQS41 (PL41A) K2 RAM_UDQS
LDQSN41 (PL41B) J1 RAM_UDQS#
(PL41C) H1 RAM_UDM
(PL41D) K1 RAM_RAS#
(PL44A) K4 RAM_CAS#
VREF1_6 (PL44B) K5
(PL44C) L4 RAM_WE#
(PL44D) L5 RAM_RST#
LDQS53 (PL53A) M5
(PL59A) M4 RAM_DQ8
(PL59B) N5 RAM_DQ9
(PL59C) N4 RAM_DQ10
(PL59D) P5 RAM_DQ11
(PL62A) N3 RAM_DQ12
(PL62B) M3 RAM_DQ13
(PL62C) L3 RAM_DQ14
(PL62D) L2 RAM_DQ15
LDQS65 (PL65A) N2 RAM_LDQS
LDQSN65 (PL65B) M1 RAM_LDQS#
(PL65C) L1 RAM_LDM
(PL65D) N1 RAM_CS#
(PL68A) P1 RAM_CK
(PL68B) P2 RAM_CK#
LLC_GPLL0T_IN (PL68C) P3 RAM_CKE
LLC_GPLL0C_IN (PL68D) P4 RAM_ODT
LFE5UM5G-45F-8BG381C
VTT
C407 10 nF
C408 100 nF
GND
U201Bank 0
Bank 0
ULC_GPLL1T_IN (PT4A) A6 RAM_A0
ULC_GPLL1C_IN (PT4B) B6 RAM_A1
(PT6A) E6 RAM_A2
(PT6B) D6 RAM_A3
(PT9A) E7 RAM_A4
(PT9B) D7 RAM_A5
(PT11A) C6 RAM_A6
(PT11B) C7 RAM_A7
(PT13A) E8 RAM_A8
(PT13B) D8 RAM_A9
(PT15A) C8 RAM_A10
(PT15B) B8 RAM_A11
(PT18A) A7 RAM_A12
(PT18B) A8 RAM_A13
(PT20A) D9 RAM_A14
(PT20B) E9 RAM_A15
(PT27A) C9 RAM_BA0
(PT29A) D10 RAM_BA1
(PT29B) E10 RAM_BA2
(PT31A) B9 ? plz fix
(PT31B) C10 ? plz fix
GR_PCLK0_1 (PT33A) A9 ? plz fix
GR_PCLK0_0 (PT33B) B10 ? plz fix
PCLKT0_1 (PT36A) A10 ? plz fix
PCLKC0_1 (PT36B) A11 ? plz fix
PCLKT0_0 (PT38A) B11 ? plz fix
PCLKC0_0 (PT38B) C11 ? plz fix
more addr lines
LFE5UM5G-45F-8BG381C
1V35
needs more current capability
FB401
BLM18AG601SN1D
C401 22 µF
C402 C403 1 µF 1 µF
C404 C405 100 nF 1 µF
C406 100 nF
DDR_VDD
1V35
needs more current capability
FB402
BLM18AG601SN1D
C409 22 µF
C410 C411 1 µF 1 µF
C412 C413 100 nF 1 µF
C414 100 nF
DDR_VDDQ
place near memory, one per quarter, vias on side of memory
U401
RAM_A0 N3 A0
RAM_A1 P7 A1
RAM_A2 P3 A2
RAM_A3 N2 A3
RAM_A4 P8 A4
RAM_A5 P2 A5
RAM_A6 R8 A6
RAM_A7 R2 A7
RAM_A8 T8 A8
RAM_A9 R3 A9
RAM_A10 L7 A10
RAM_A11 R7 A11
RAM_A12 N7 A12
RAM_A13 T3 A13
RAM_A14 T7 A14
RAM_A15 M7 A15
RAM_BA0 M2 BA0
RAM_BA1 N8 BA1
RAM_BA2 M3 BA2
RAM_CK J7 CK
RAM_CK# K7 CK#
RAM_CKE K9 CKE
RAM_RAS# J3 RAS#
RAM_RST# T2 RESET#
RAM_CAS# K3 CAS#
RAM_CS# L2 CS#
RAM_WE# L3 WE#
RAM_ODT K1 ODT
DDR_VDD B2 ... R9 VDD
DDR_VDDQ A1 ... H9 VDDQ
M8 VREFCA
H1 VREFDQ
L8 ZQ
A9 ... T9 VSS
B1 ... G9 VSSQ
NC L9 NC
UDM D3 RAM_UDM
UDQS C7 RAM_UDQS
UDQS# B7 RAM_UDQS#
LDM E7 RAM_LDM
LDQS F3 RAM_LDQS
LDQS# G3 RAM_LDQS#
DQ0 E3 RAM_DQ0
DQ1 F7 RAM_DQ1
DQ2 F2 RAM_DQ2
DQ3 F8 RAM_DQ3
DQ4 H3 RAM_DQ4
DQ5 H8 RAM_DQ5
DQ6 G2 RAM_DQ6
DQ7 H7 RAM_DQ7
DQ8 D7 RAM_DQ8
DQ9 C3 RAM_DQ9
DQ10 C8 RAM_DQ10
DQ11 C2 RAM_DQ11
DQ12 A7 RAM_DQ12
DQ13 A2 RAM_DQ13
DQ14 B8 RAM_DQ14
DQ15 A3 RAM_DQ15
MT41K512M16HA
VTT_REF
C415 10 nF
C416 100 nF
GND
VTT
R401 RAM_A0 50 Ω
R403 RAM_A1 50 Ω
R405 RAM_A2 50 Ω
R407 RAM_A3 50 Ω
R409 RAM_A4 50 Ω
R411 RAM_A5 50 Ω
R413 RAM_A6 50 Ω
R415 RAM_A7 50 Ω
R417 RAM_A8 50 Ω
R419 RAM_A9 50 Ω
R421 RAM_A10 50 Ω
R423 RAM_A11 50 Ω
R425 RAM_A12 50 Ω
R427 RAM_CK 50 Ω
R428 RAM_CK# 50 Ω
C425 10 nF
GND
R402 RAM_A13 50 Ω
R404 RAM_A14 50 Ω
R406 RAM_A15 50 Ω
R408 RAM_BA0 50 Ω
R410 RAM_BA1 50 Ω
R412 RAM_BA2 50 Ω
R414 RAM_CKE 50 Ω
R416 RAM_RAS# 50 Ω
R418 RAM_CAS# 50 Ω
R420 RAM_CS# 50 Ω
R422 RAM_WE# 50 Ω
R424 RAM_ODT 50 Ω
R426 RAM_RST# 50 Ω
MAYBE???
Locate on memory side
Consider resistor networks?
VTT
C417 100 nF
C418 10 nF
C419 100 nF
C420 10 nF
C421 100 nF
C422 10 nF
C423 100 nF
C424 10 nF
GND
Sheet
RAM
Number
4/12
Project
Axiom micro rev3
Revision
0
Drawn by
anuejn & vup
License
CERN-OHL-S V2
Date
20200324
open source hardware

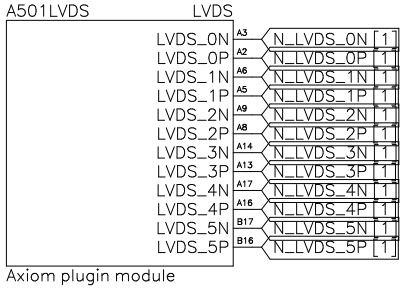
plugin north



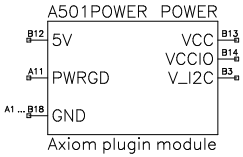
Axiom plugin module



Axiom plugin module

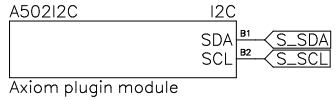


Axiom plugin module

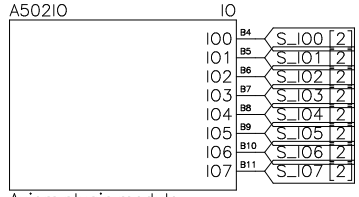


Axiom plugin module

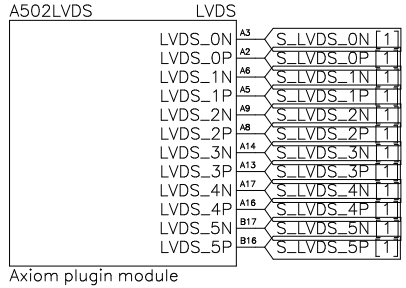
plugin south



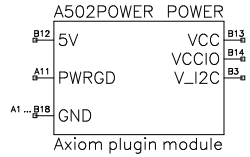
Axiom plugin module



Axiom plugin module



Axiom plugin module



Axiom plugin module

Sheet plugin	Number 5/12
Project Axiom micro rev3	Revision 0
Drawn by anuejn & vup	
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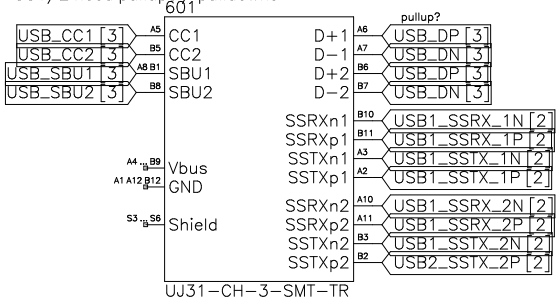
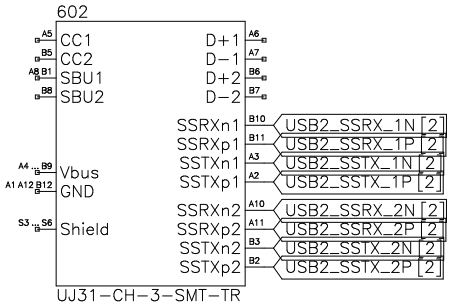
We probably want to be a upwards facing port?
CC1/2 need pullups / pulldowns





Sheet USB	Number 6/12
Project Axiom micro rev3	Revision 0
Drawn by anuejn & vup	
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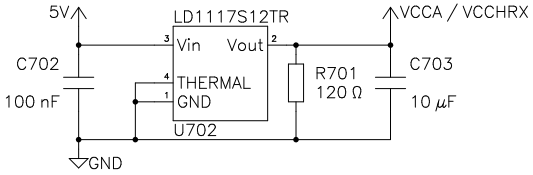
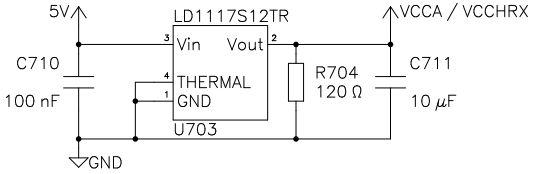
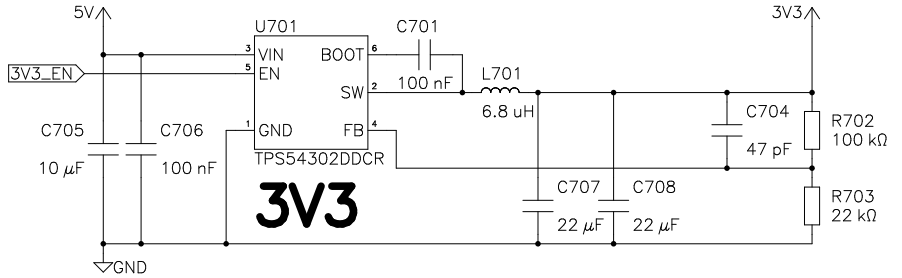
Date 20200324	

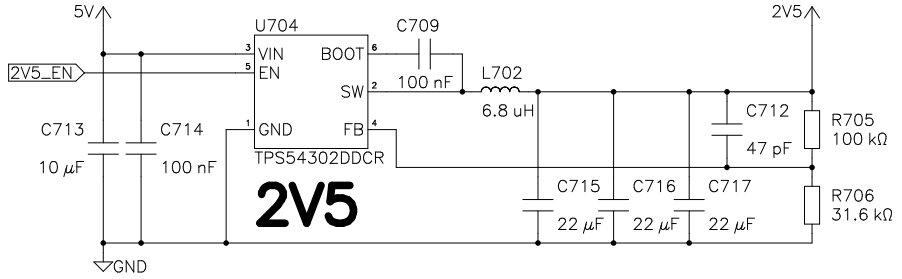


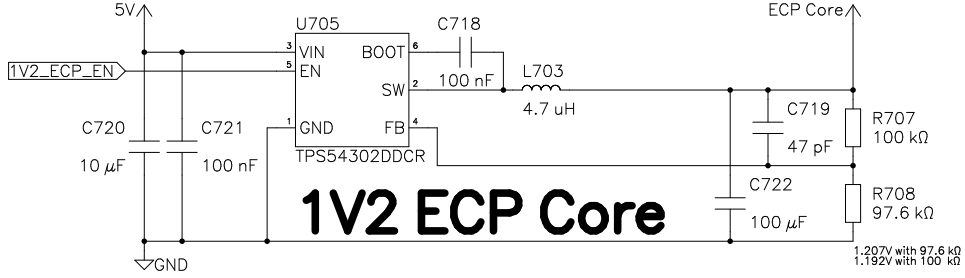
1V2 VCCA / VCCHRX

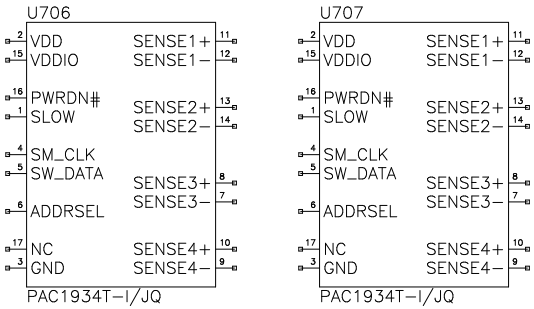


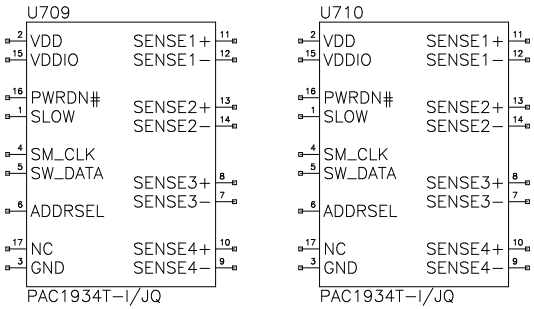
1V2 VCCHTX

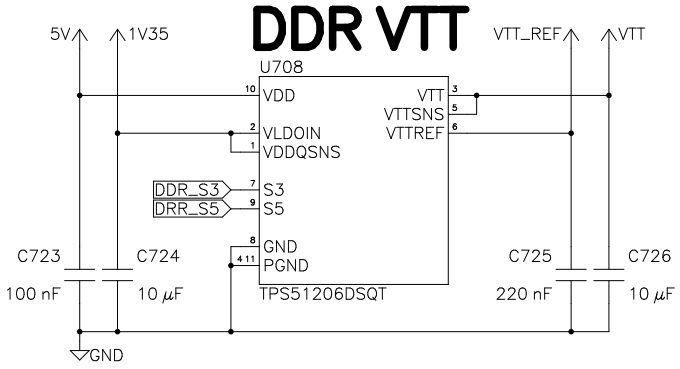












positive terminal of the VTT pin output capacitor(s) as a separate trace from the high−current path from VTT. Consider adding a low−pass R−C filter at the VTTSNS pin in case the ESR of the VTT output capacitor(s) is larger than 2 mΩ. The R−C filter time constant should be approximately the same or slightly lower than the time constant of the VTT output capacitance and ESR.

Sheet: power fixed	Number: 7/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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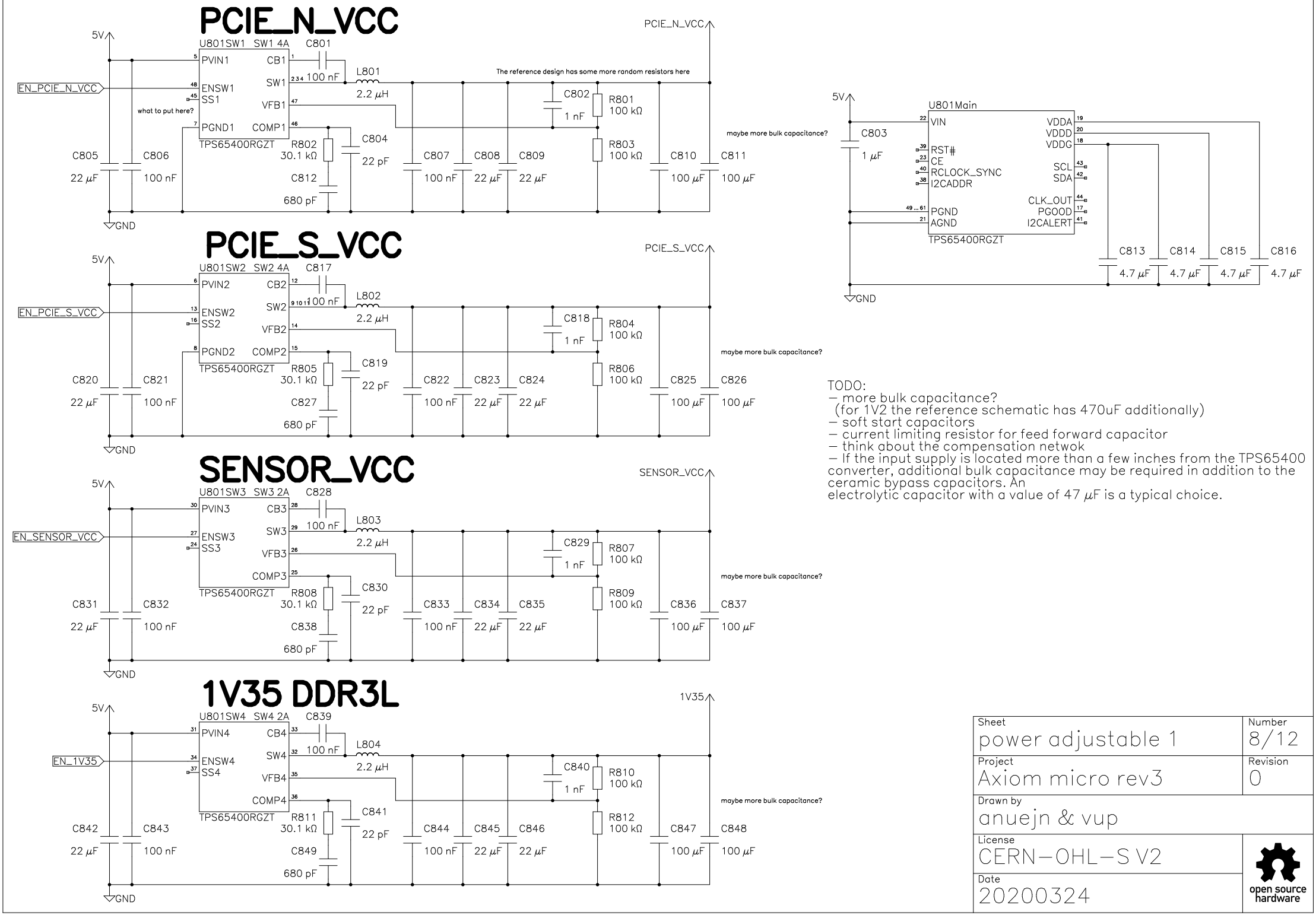
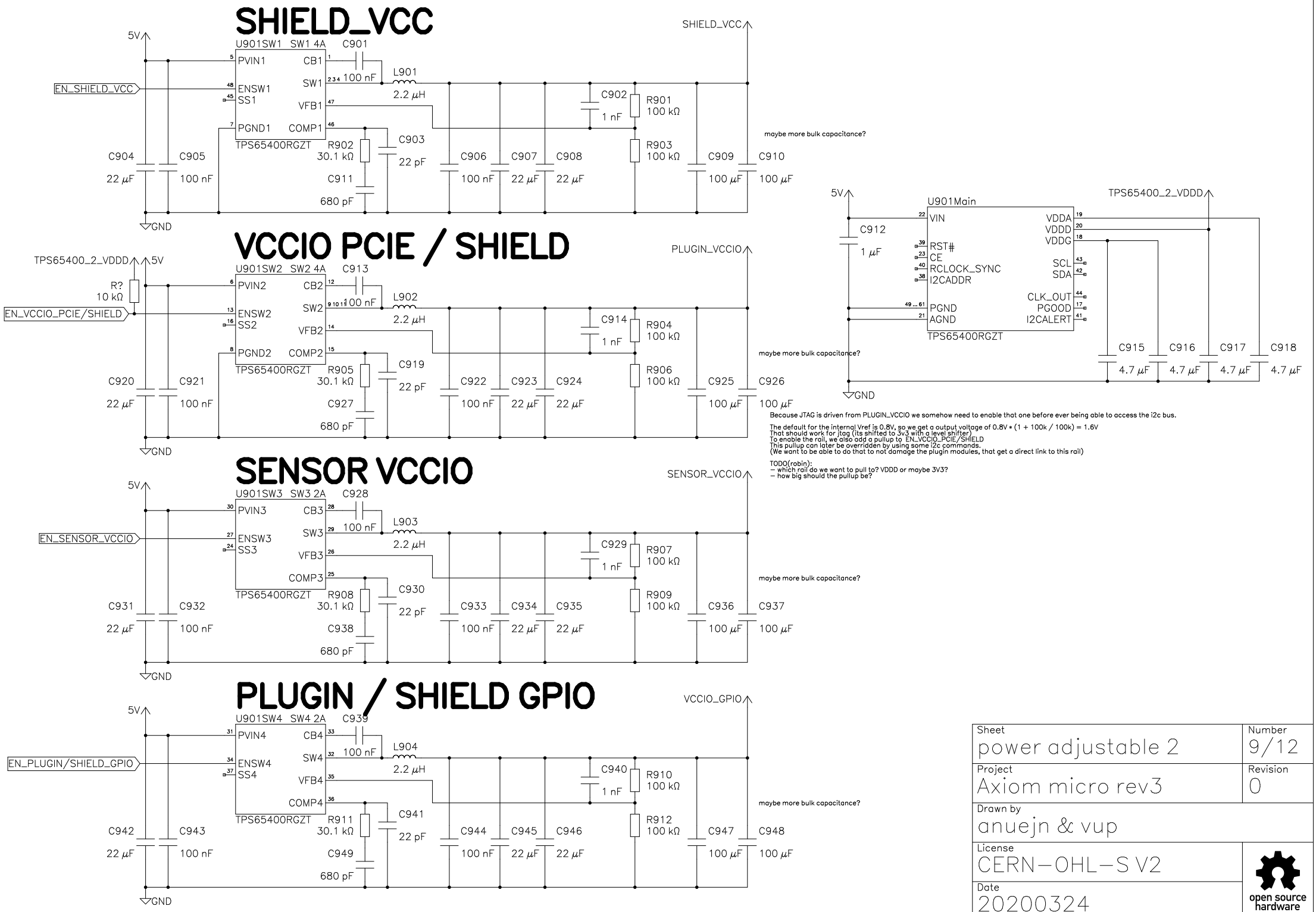
Date: 20200324	


PCIE_N_VCC
5V
U801SW1 SW1 4A
C801
PVIN1
CB1
100 nF
L801
2.2 µH
EN_PCIE_N_VCC
ENSW1
SW1
SS1
VFB1
what to put here?
PGND1
COMP1
TPS65400RGZT
R802
30.1 kΩ
C804
22 pF
C812
680 pF
C802
1 nF
R801
100 kΩ
R803
100 kΩ
The reference design has some more random resistors here
maybe more bulk capacitance?
C805
22 µF
C806
100 nF
C807
100 nF
C808
22 µF
C809
22 µF
C810
100 µF
C811
100 µF
PCIE_N_VCC
GND
PCIE_S_VCC
U801SW2 SW2 4A
C817
PVIN2
CB2
100 nF
L802
2.2 µH
EN_PCIE_S_VCC
ENSW2
SW2
SS2
VFB2
PGND2
COMP2
TPS65400RGZT
R805
30.1 kΩ
C819
22 pF
C827
680 pF
C818
1 nF
R804
100 kΩ
R806
100 kΩ
maybe more bulk capacitance?
C820
22 µF
C821
100 nF
C822
100 nF
C823
22 µF
C824
22 µF
C825
100 µF
C826
100 µF
PCIE_S_VCC
GND
SENSOR_VCC
U801SW3 SW3 2A
C828
PVIN3
CB3
100 nF
L803
2.2 µH
EN_SENSOR_VCC
ENSW3
SW3
SS3
VFB3
COMP3
TPS65400RGZT
R808
30.1 kΩ
C830
22 pF
C838
680 pF
C829
1 nF
R807
100 kΩ
R809
100 kΩ
maybe more bulk capacitance?
C831
22 µF
C832
100 nF
C833
100 nF
C834
22 µF
C835
22 µF
C836
100 µF
C837
100 µF
SENSOR_VCC
GND
1V35 DDR3L
5V
U801SW4 SW4 2A
C839
PVIN4
CB4
100 nF
L804
2.2 µH
EN_1V35
ENSW4
SW4
SS4
VFB4
COMP4
TPS65400RGZT
R811
30.1 kΩ
C841
22 pF
C849
680 pF
C840
1 nF
R810
100 kΩ
R812
100 kΩ
maybe more bulk capacitance?
C842
22 µF
C843
100 nF
C844
100 nF
C845
22 µF
C846
22 µF
C847
100 µF
C848
100 µF
1V35
GND
5V
U801Main
C803
1 µF
VIN
RST#
CE
RCLOCK_SYNC
I2CADDR
PGND
AGND
VDDA
VDDD
VDDG
SCL
SDA
CLK_OUT
PGOOD
I2CALERT
TPS65400RGZT
C813
4.7 µF
C814
4.7 µF
C815
4.7 µF
C816
4.7 µF
GND
TODO:
– more bulk capacitance?
(for 1V2 the reference schematic has 470uF additionally)
– soft start capacitors
– current limiting resistor for feed forward capacitor
– think about the compensation netwok
– If the input supply is located more than a few inches from the TPS65400 converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An
electrolytic capacitor with a value of 47 µF is a typical choice.
Sheet
power adjustable 1
Number
8/12
Project
Axiom micro rev3
Revision
0
Drawn by
anuejn & vup
License
CERN–OHL–S V2
Date
20200324
open source hardware



Because JTAG is driven from PLUGIN_VCCIO we somehow need to enable that one before ever being able to access the i2c bus.

The default for the internal Vref is 0.8V, so we get a output voltage of 0.8V * (1 + 100k / 100k) = 1.6V
That should work for jtag (its shifted to 3v3 with a level shifter)
To enable the rail, we also add a pullup to EN_VCCIO_PCIE/SHIELD
This pullup can later be overridden by using some i2c commands.
(We want to be able to do that to not damage the plugin modules, that get a direct link to this rail)

TODO(robin):
– which rail do we want to pull to? VDDD or maybe 3V3?
– how big should the pullup be?

Sheet: power adjustable 2	Number: 9/12
Project: Axiom micro rev3	Revision: 0
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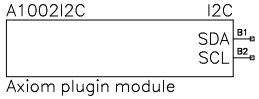

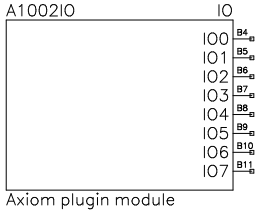

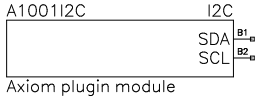

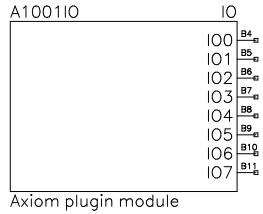

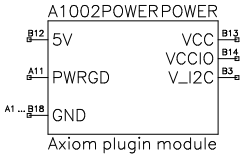

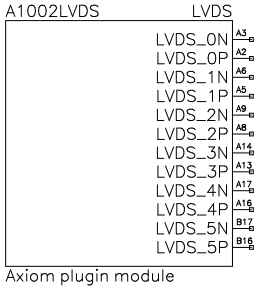

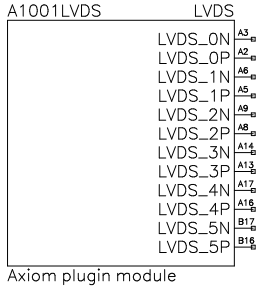

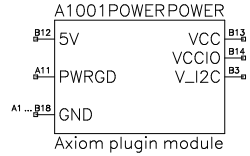

Sheet: image_sensor	Number: 10/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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Sheet shield	Number 11/12
Project Axiom micro rev3	Revision 0
Drawn by anuejn & vup	
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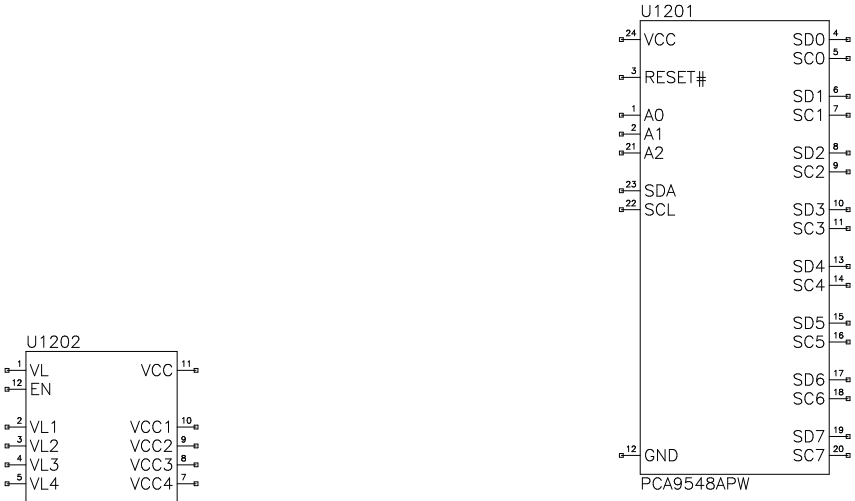

Stuff we want to hang of the i2c mux:
plugin modules
pmic
probably gpio expander for power stuff
????

Sheet: misc	Number: 12/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	open source hardware
Date: 20200324	