
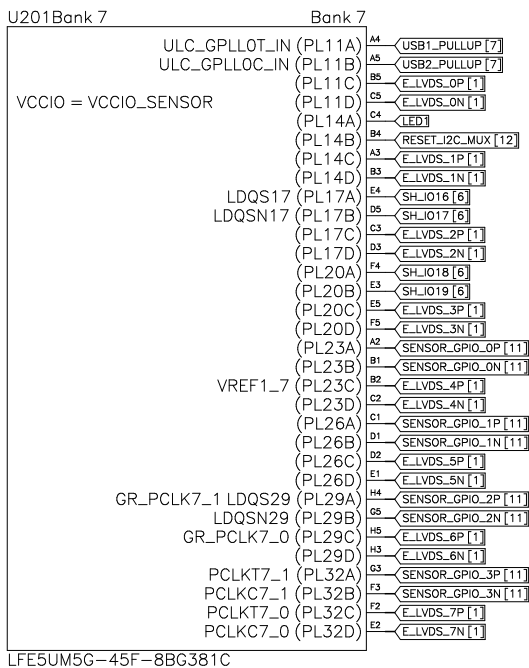
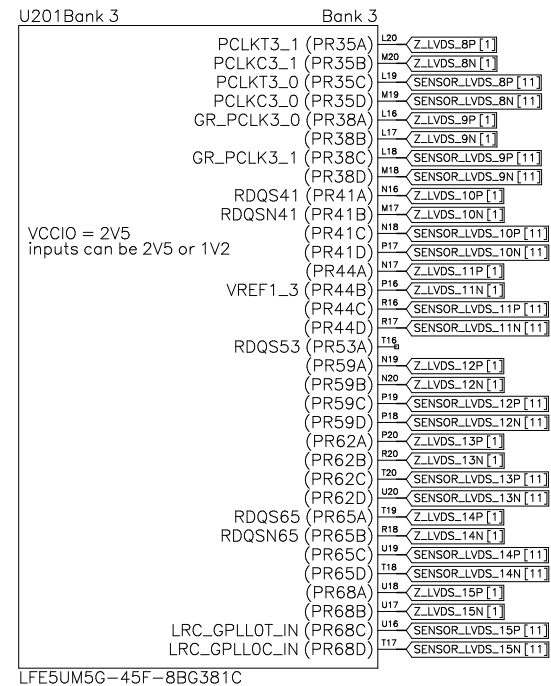
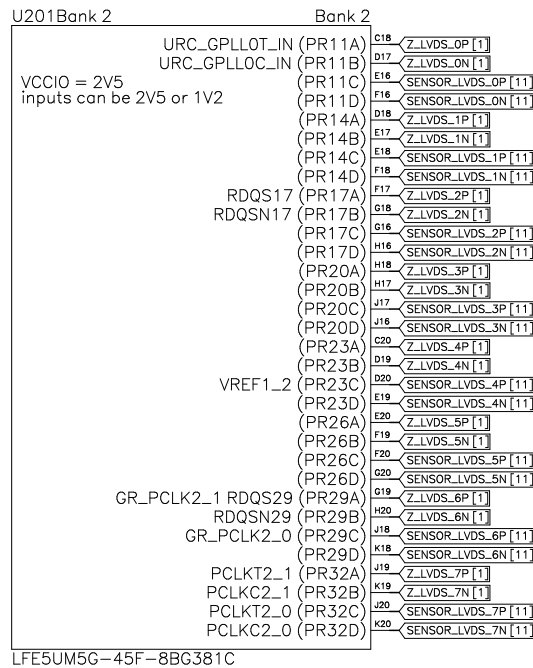
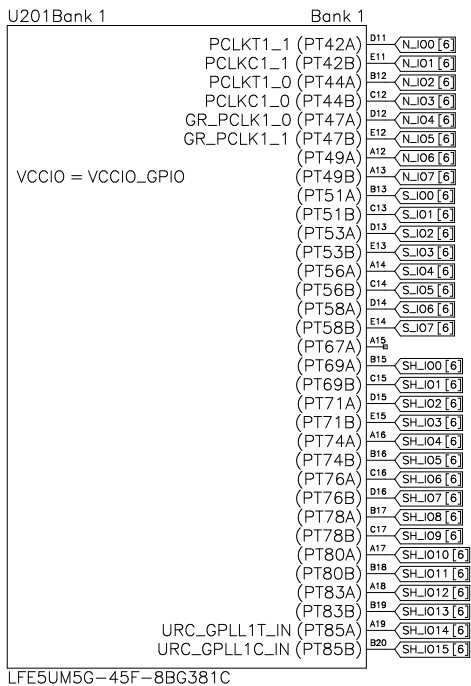
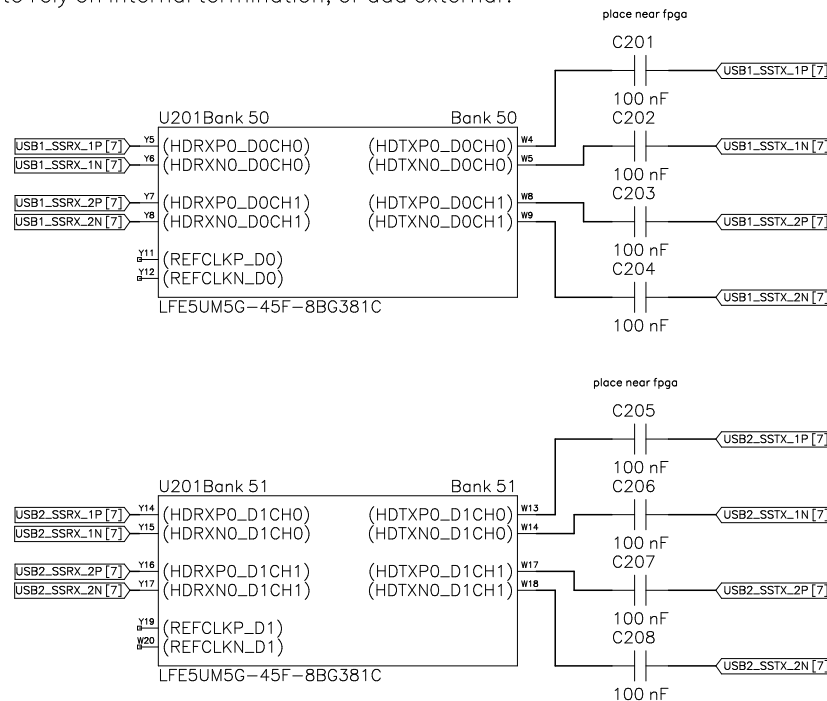


Sheet	zturn lite	Number	1/12
Project	Axiom micro rev3	Revision	0
Drawn by	anuejn & vup		
License	CERN-OHL-S V2		
Date	20200324		
			 open source hardware




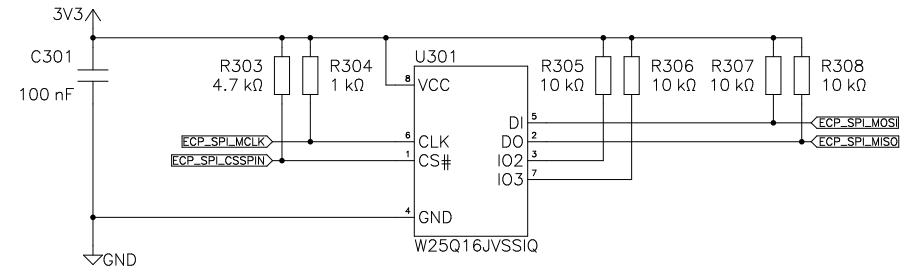
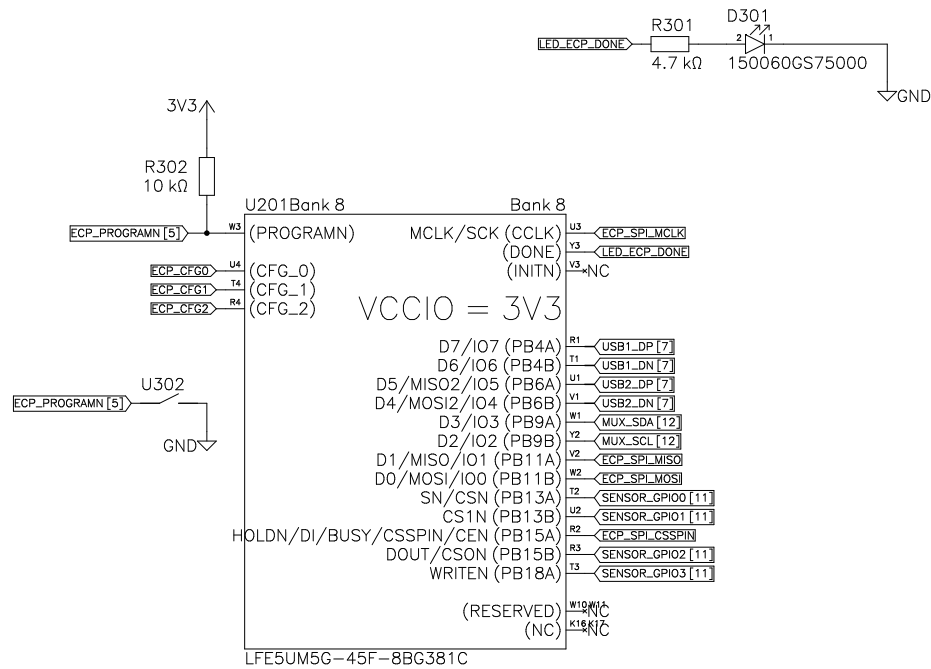
Do we want to rely on internal termination, or add external?



Z\_LVDS goes from ECP to ZYNQ  
E\_LVDS goes from ZYNQ to ECP  
SENSOR\_LVDS goes from sensor board to ECP

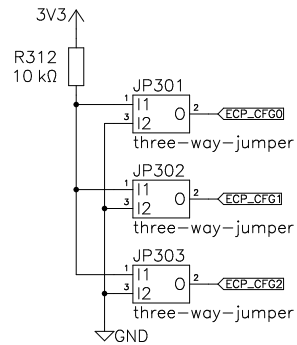


Sheet	Number
ecp	2/12
Project	Revision
Axiom micro rev3	0
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20200324	
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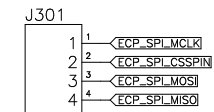
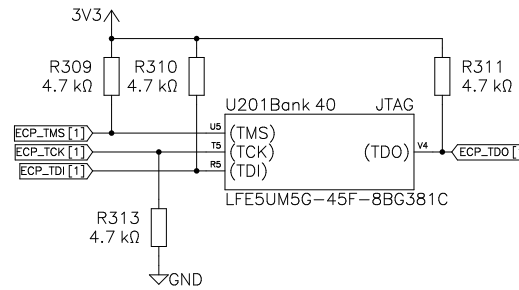


The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI operation. When the QE bit is set to a 0 state (factory default for part numbers with ordering options **TIMT**), the /WP pin and /HOLD are enabled. When the QE bit is set to a 1 (factory default for Quad Enabled part numbers with ordering option **TIOY**), the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled.

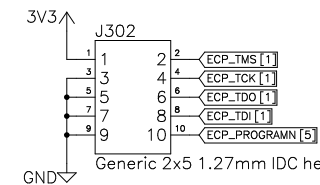
/CS must track VCC during VCC Ramp Up/Down



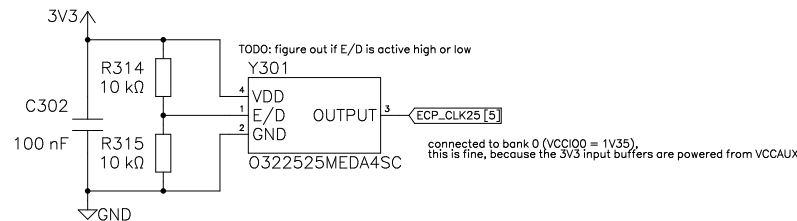
MODE	CFG2	CFG1	CFG0
SSPI	0	0	0
MSPI	0	1	0
SCM	1	0	1
SPCM	1	1	1



Generic Pin header 1x4, 2.54mm pitch, vertical



Generic 2x5 1.27mm IDC header



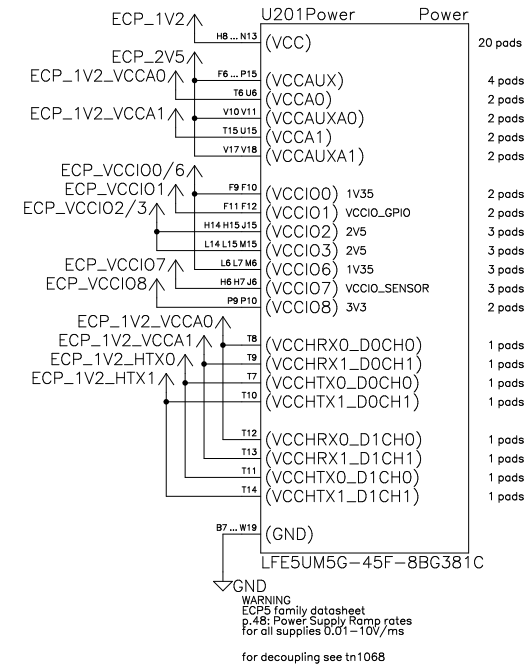
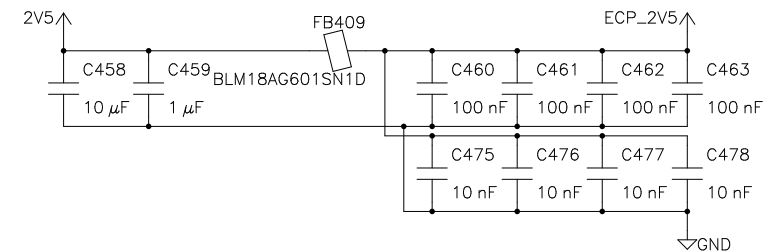
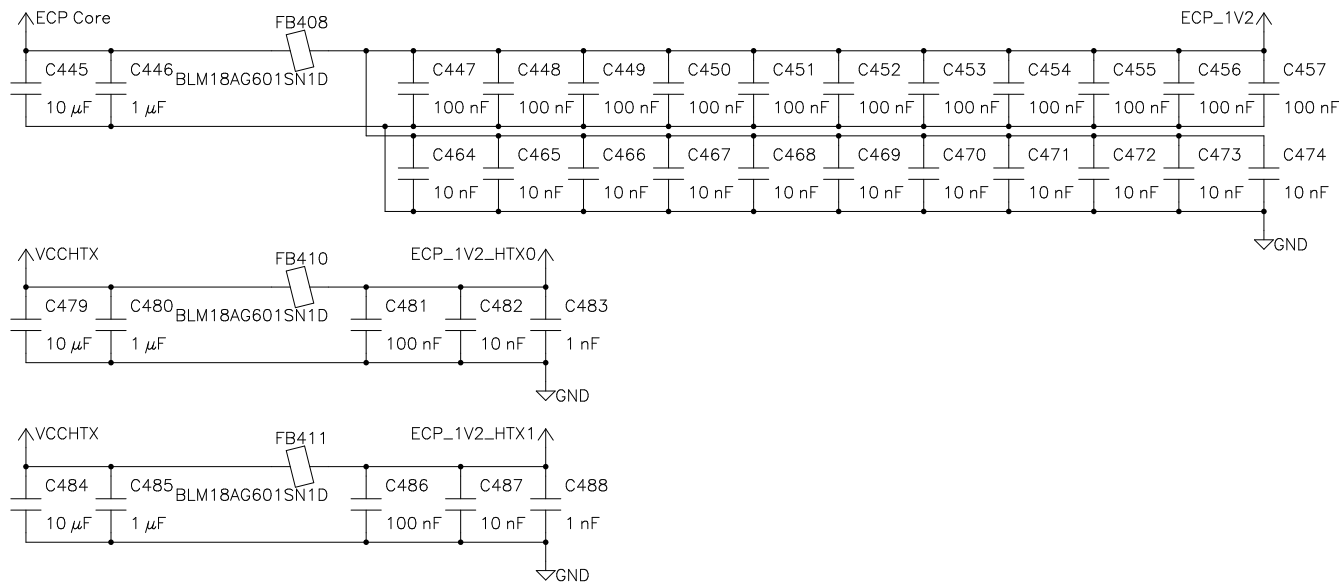
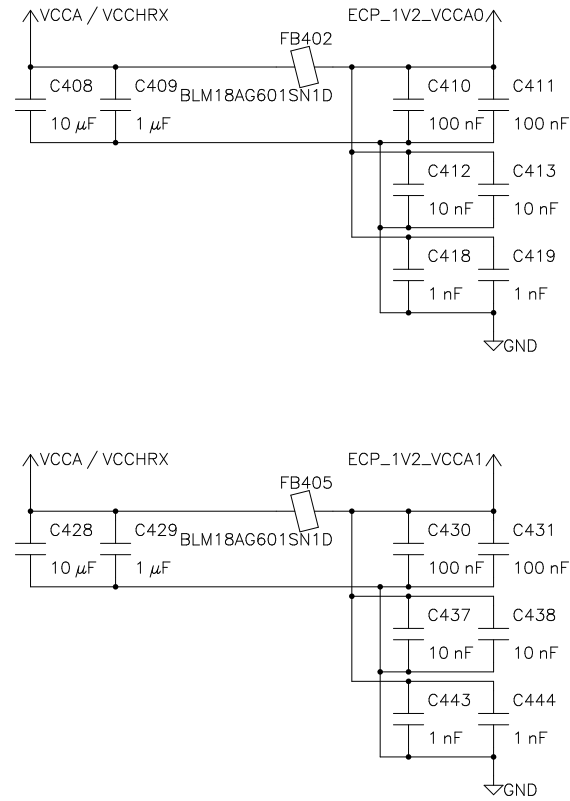
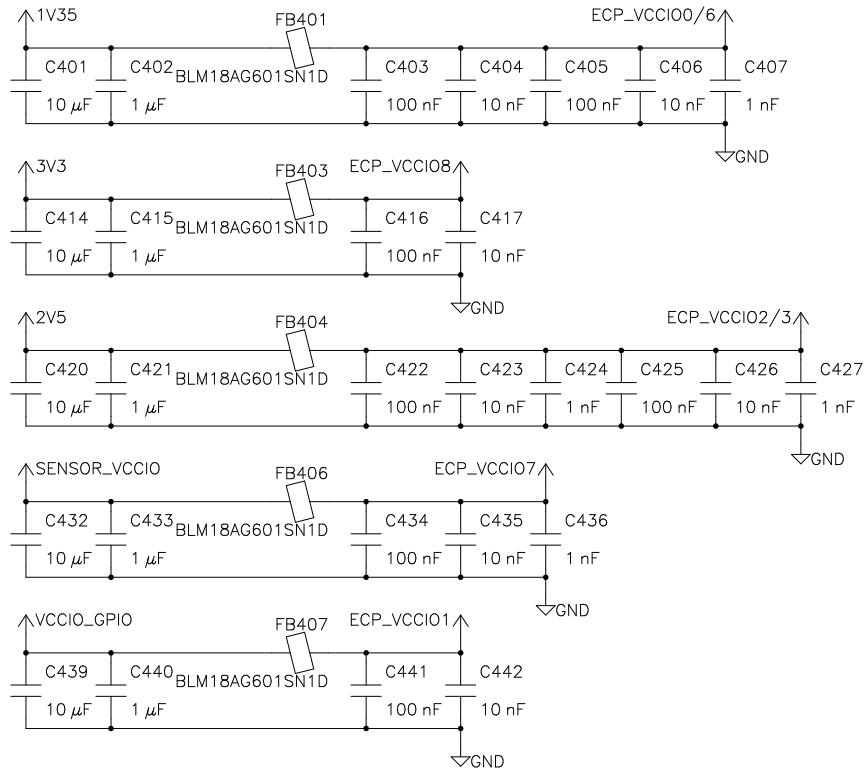
TODD: figure out if E/D is active high or low

connected to bank 0 (VCCIO0 = 1V35), this is fine, because the 3V3 input buffers are powered from VCCAUX

Sheet	Number
ecp config	3/12
Project	Revision
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Place decoupling near FPGA, alternate 100n and 10n per pad per rail

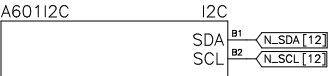


Sheet	Number
ecp power	4/12
Project	Revision
Axiom micro rev3	0
Drawn by	
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Date	
20200324	

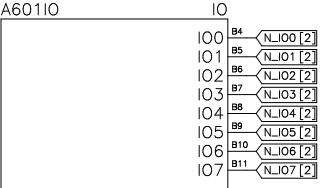




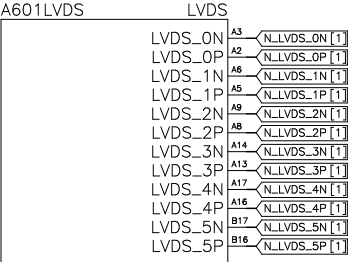
plugin north



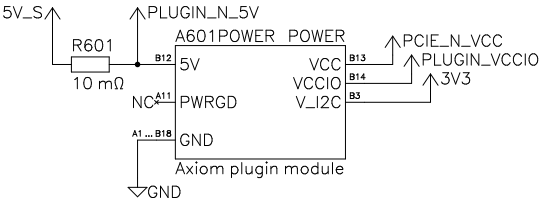
Axiom plugin module



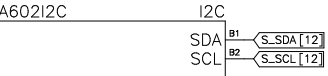
Axiom plugin module



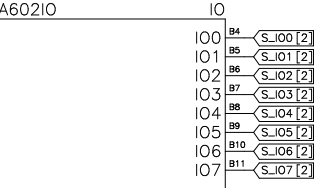
Axiom plugin module



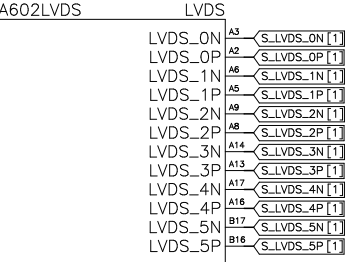
plugin south



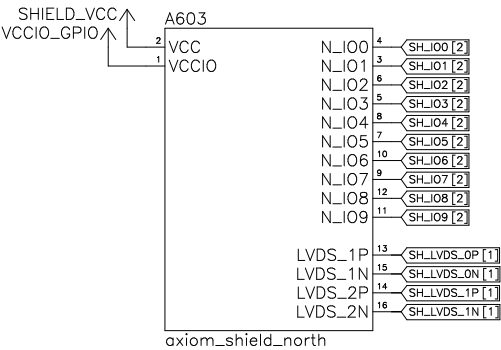
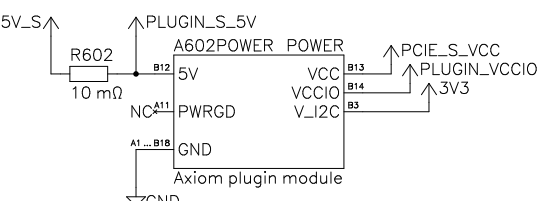
Axiom plugin module



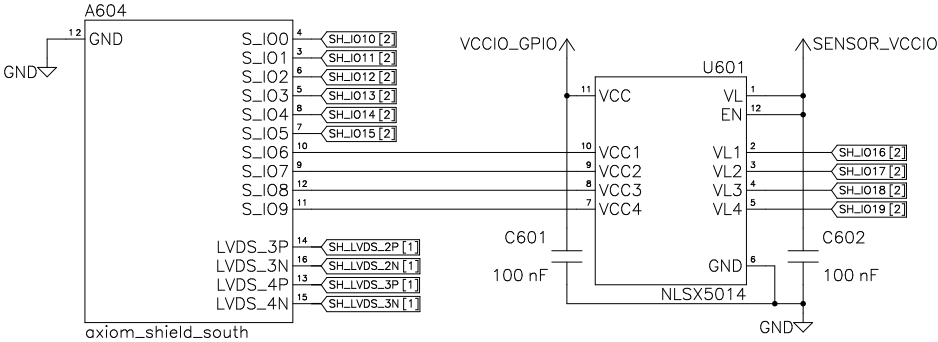
Axiom plugin module




Axiom plugin module

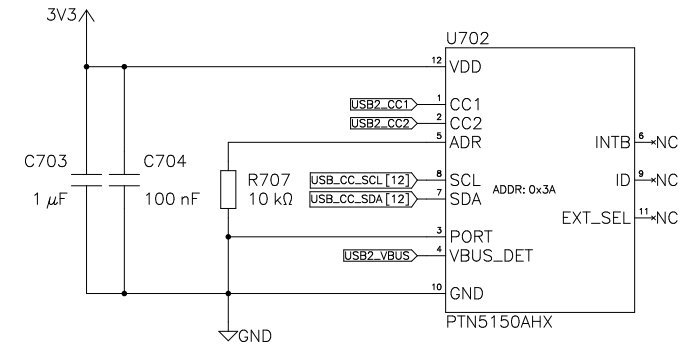
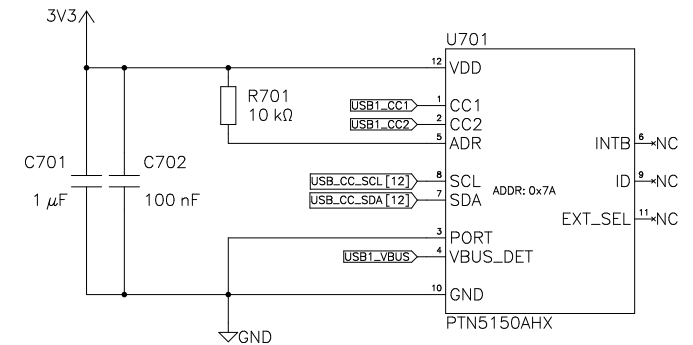
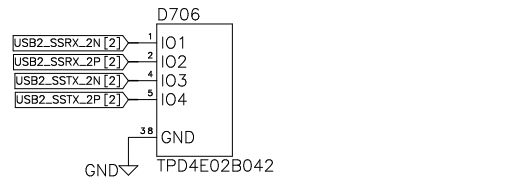
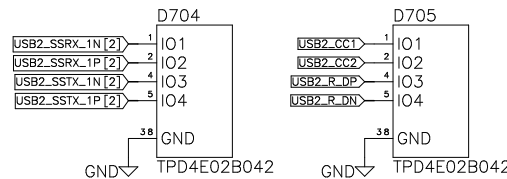
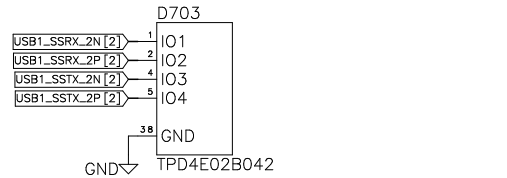
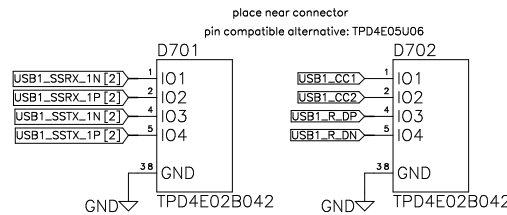
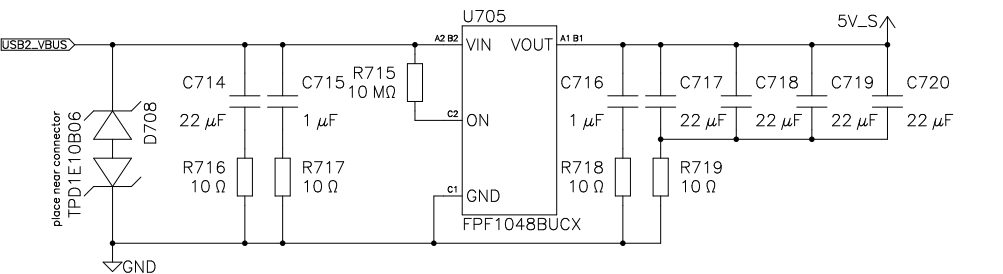
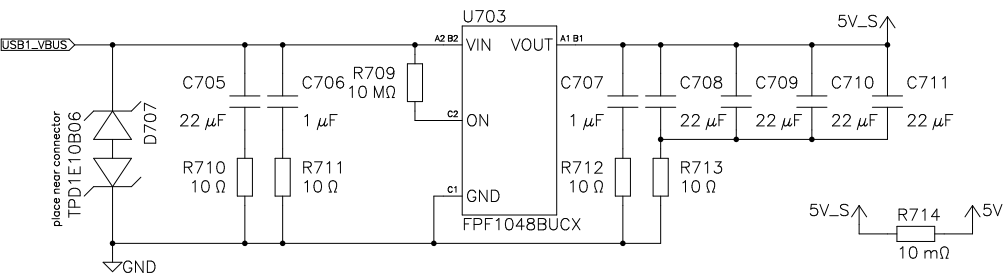
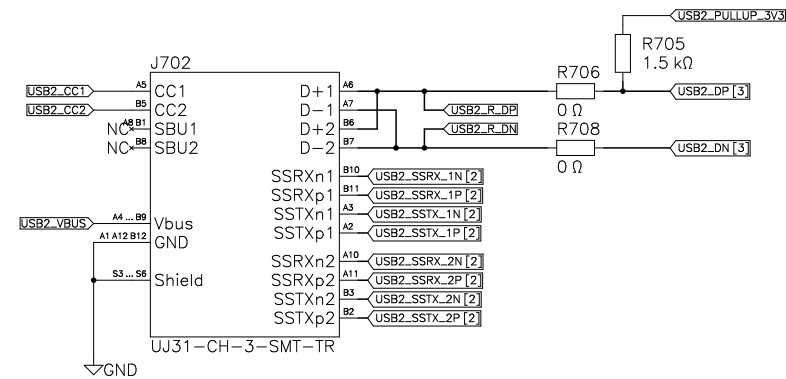
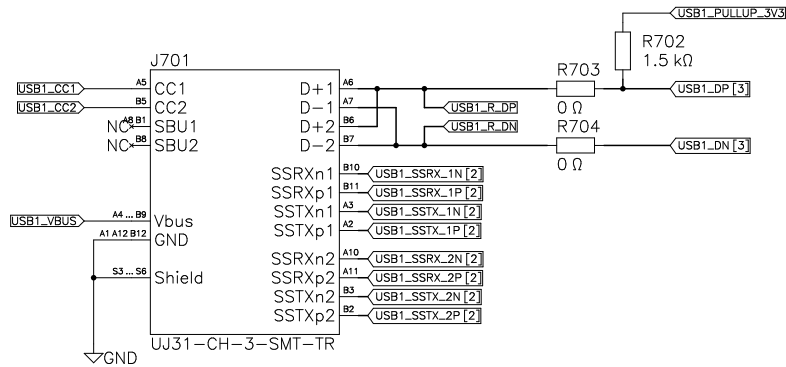


axiom\_shield\_north



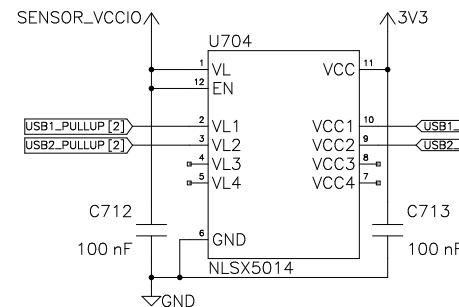
axiom\_shield\_south

Sheet	plugins / shield	Number	6/12
Project	Axiom micro rev3	Revision	0
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PORT= VDD: DFP mode (Rp = 80uA power default for non-I2C mode).  
 PORT= Mid (or floating): DRP mode  
 PORT= GND: UFP mode

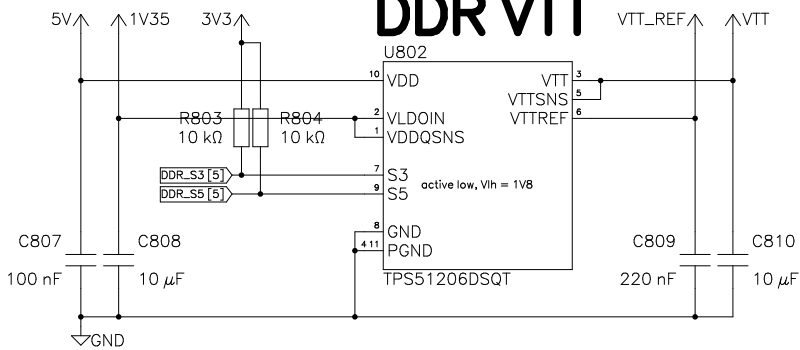
Trinary GPIO input ADDR pin run from VDD  
 - ADDR pull up to VDD with 10 kΩ resistor (I2C Enabled with ADDR bit 6 equal to 1, I2C Address 0x7A)  
 - ADDR pull down to GND with 10 kΩ resistor. (I2C Enabled with ADDR bit 6 equal to 0, I2C Address 0x3A)  
 - ADDR = Mid or floating (Pin 6/7/8) configured as OUT1/2/3 in non-I2C mode



Sheet USB	Number 7/12
Project Axiom micro rev3	Revision 0
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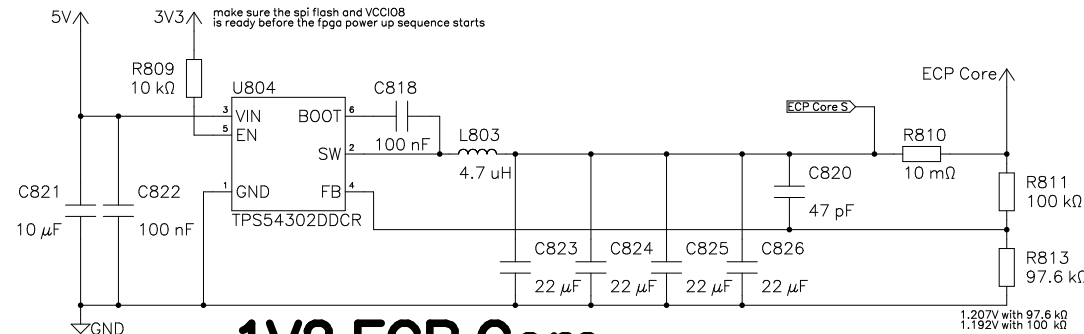
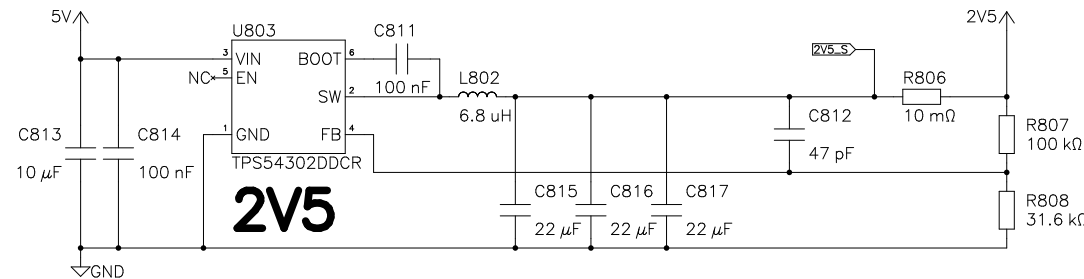
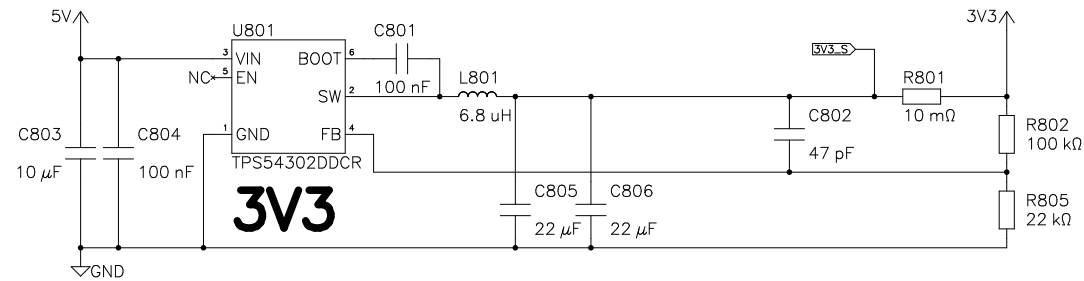
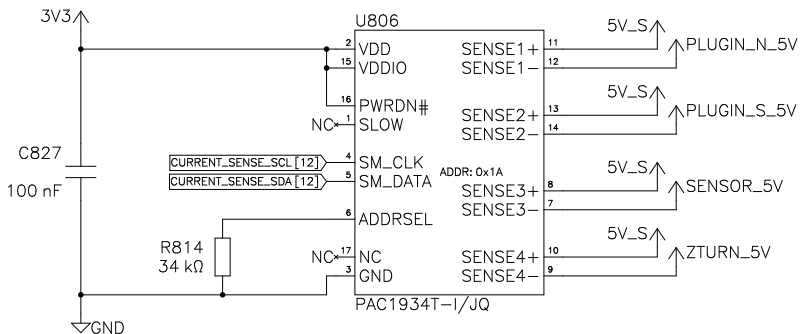
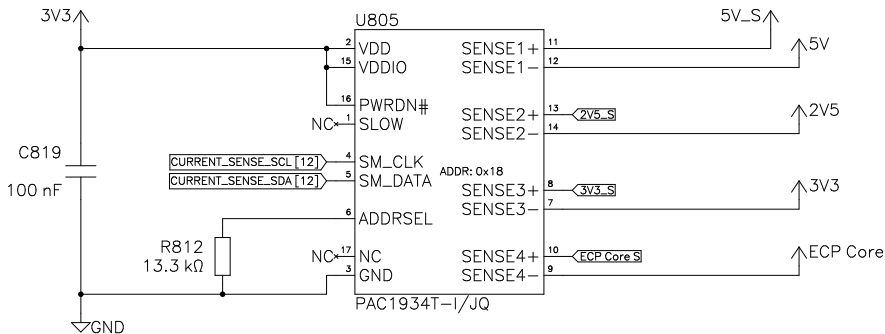


# DDR VTT



positive terminal of the VTT pin output capacitor(s) as a separate trace from the high-current path from VTT. Consider adding a low-pass R-C filter at the VTTSENS pin in case the ESR of the VTT output capacitor(s) is larger than 2 mΩ. The R-C filter time constant should be approximately the same or slightly lower than the time constant of the VTT output capacitance and ESR.

current sense resistors: O805W8F100MT5E or CS05W8F100MT5E

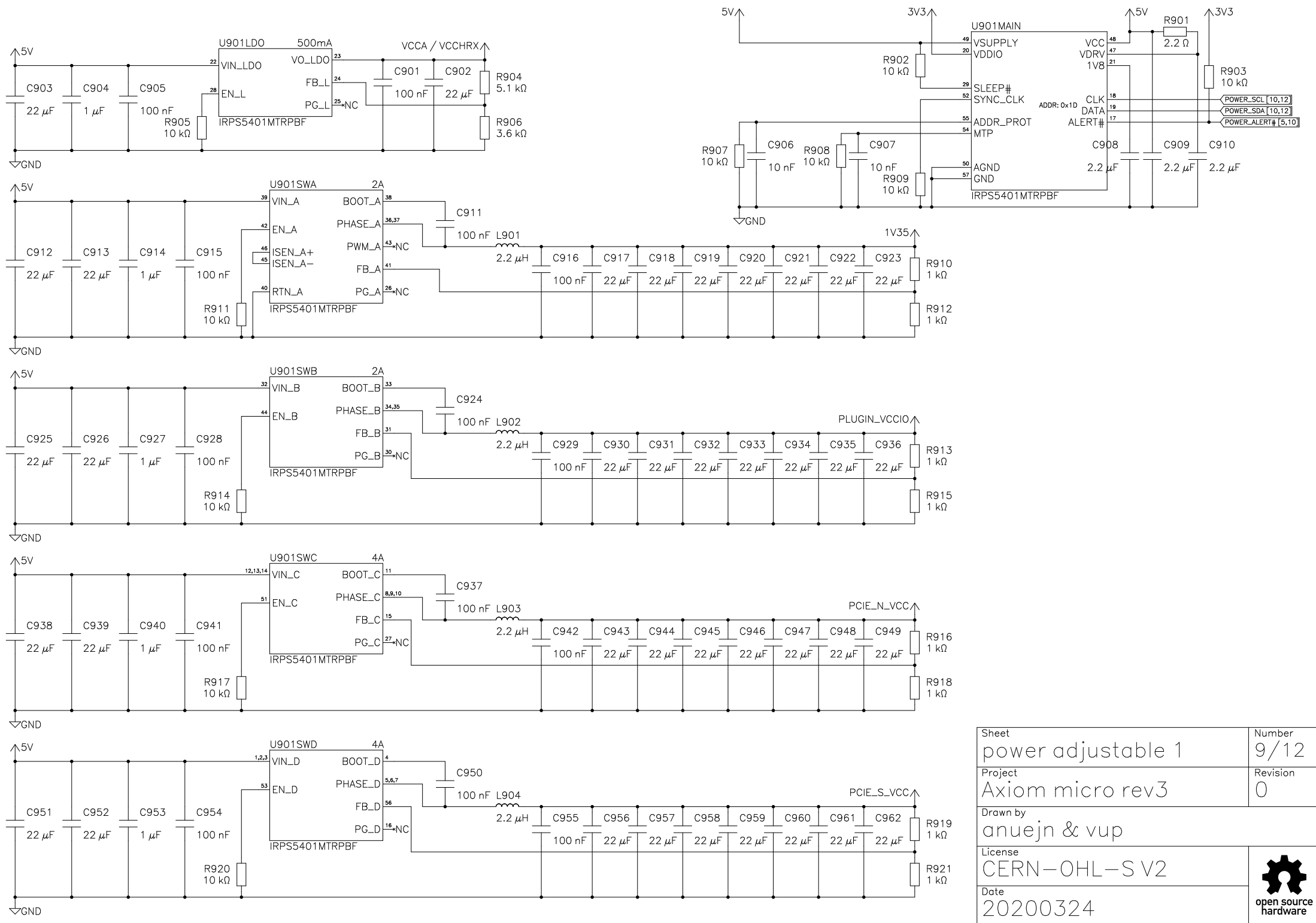


## 1V2 ECP Core

Sheet	Number
power fixed / current sense	8/12
Project	Revision
Axiom micro rev3	0
Drawn by	
anuejn & vup	
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CERN-OHL-S V2	
Date	
20200324	



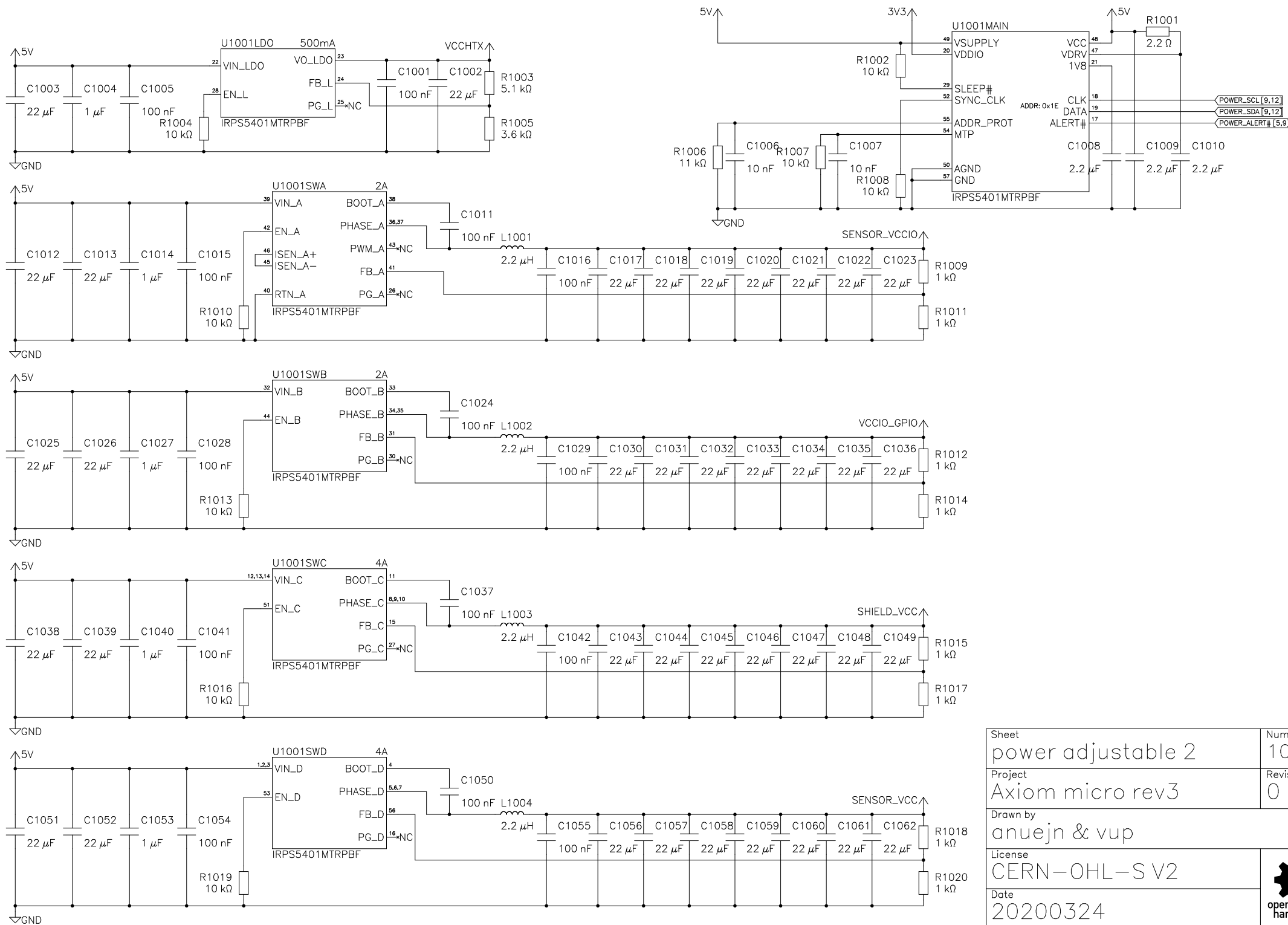




Sheet	power adjustable 1	Number	9/12
Project	Axiom micro rev3	Revision	0
Drawn by	anuejn & vup		
License	CERN-OHL-S V2		
Date	20200324		



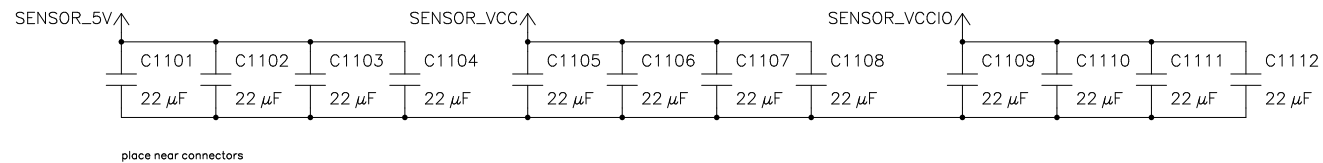
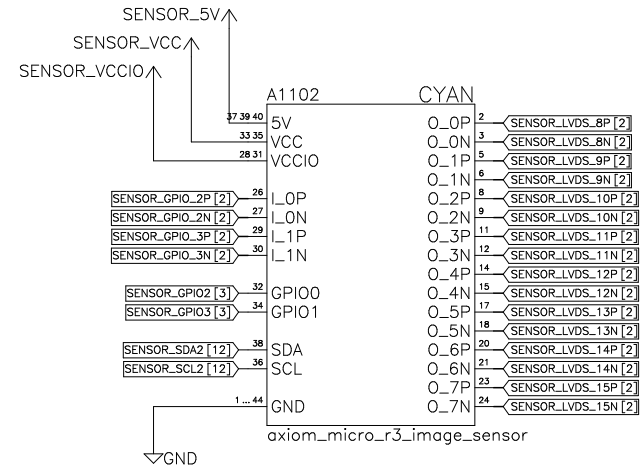
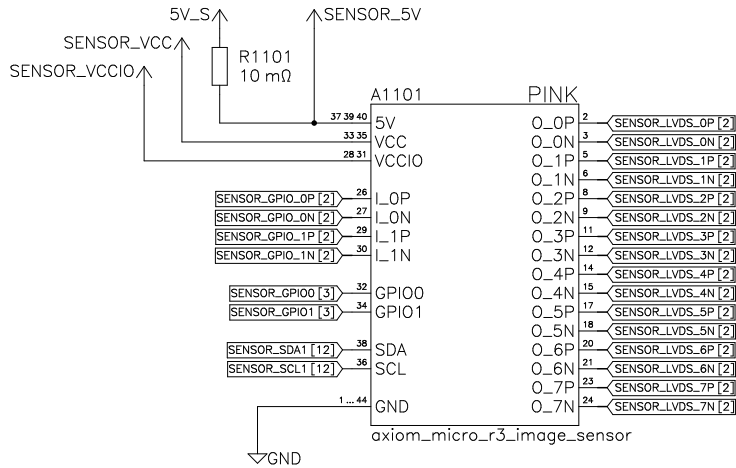
open source hardware



Sheet	power adjustable 2	Number	10/12
Project	Axiom micro rev3	Revision	0
Drawn by	anuejn & vup		
License	CERN-OHL-S V2		
Date	20200324		



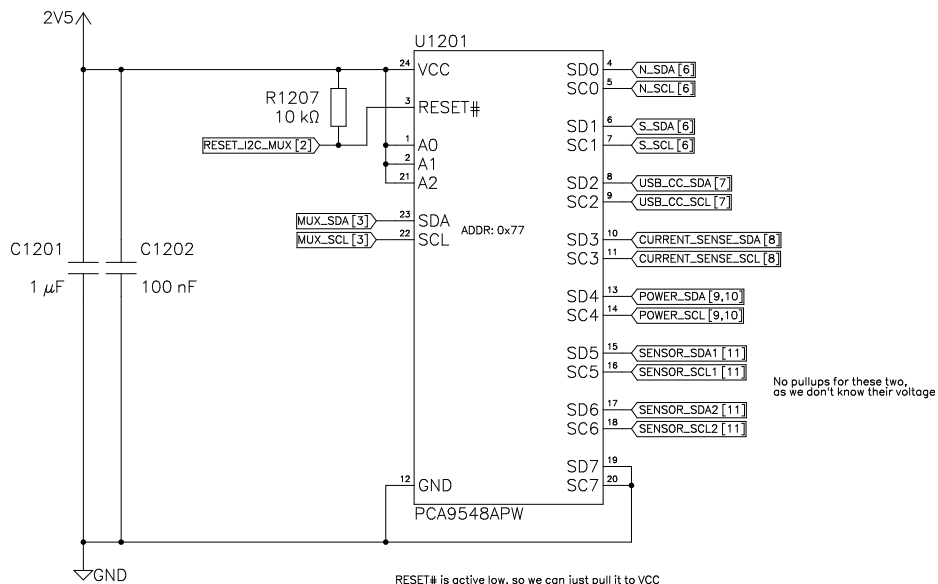
open source  
hardware



Sheet	Number
image sensor	11/12
Project	Revision
Axiom micro rev3	0
Drawn by	
anuejn & vup	
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CERN-OHL-S V2	
Date	
20200324	



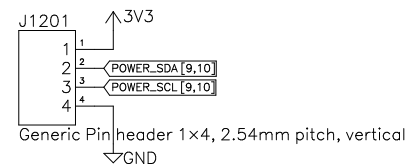
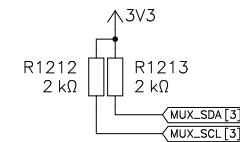
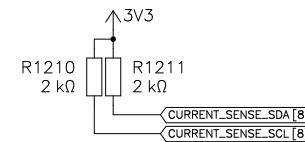
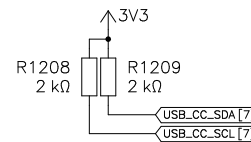
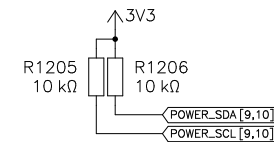
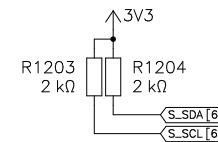
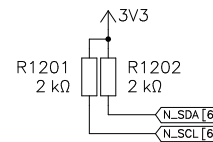
open source  
hardware



RESET# is active low, so we can just pull it to VCC  
and then pull it to GND using any VCCIO from the ECP,  
attention has to be paid to not make RESET# get over VCC,  
as otherwise current flows from the RESET pin to the VCC pin,  
this should be accomplishable by just making the fpga output Hi-Z  
if it is not pulien low

2V5 VCC means about 1V8 voltage clamping by the pass through transistors  
That should work for most applications, we just need to be careful with nothing with 1V2 is on the bus

Unused channels have to be tied to GND or VCC



Sheet	Number
i2c mux	12/12
Project	Revision
Axiom micro rev3	0
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20200324	

