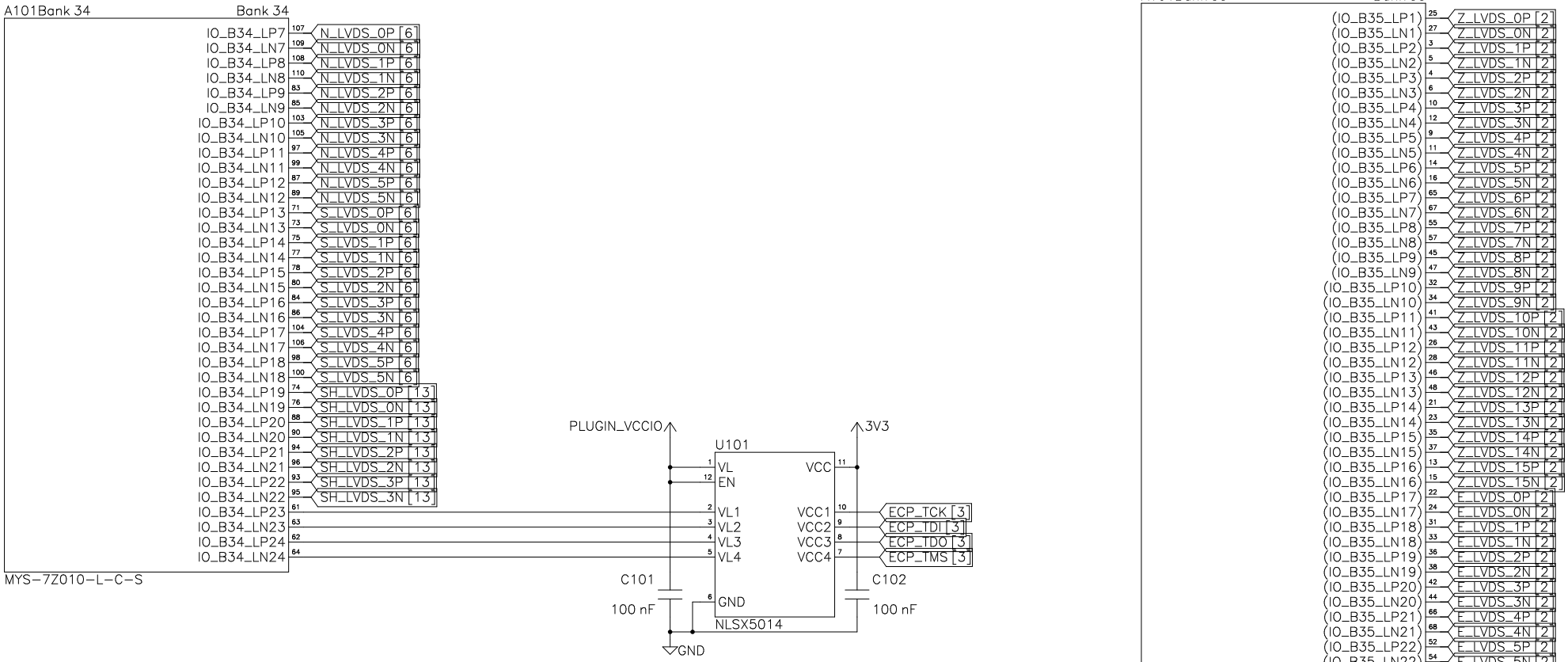
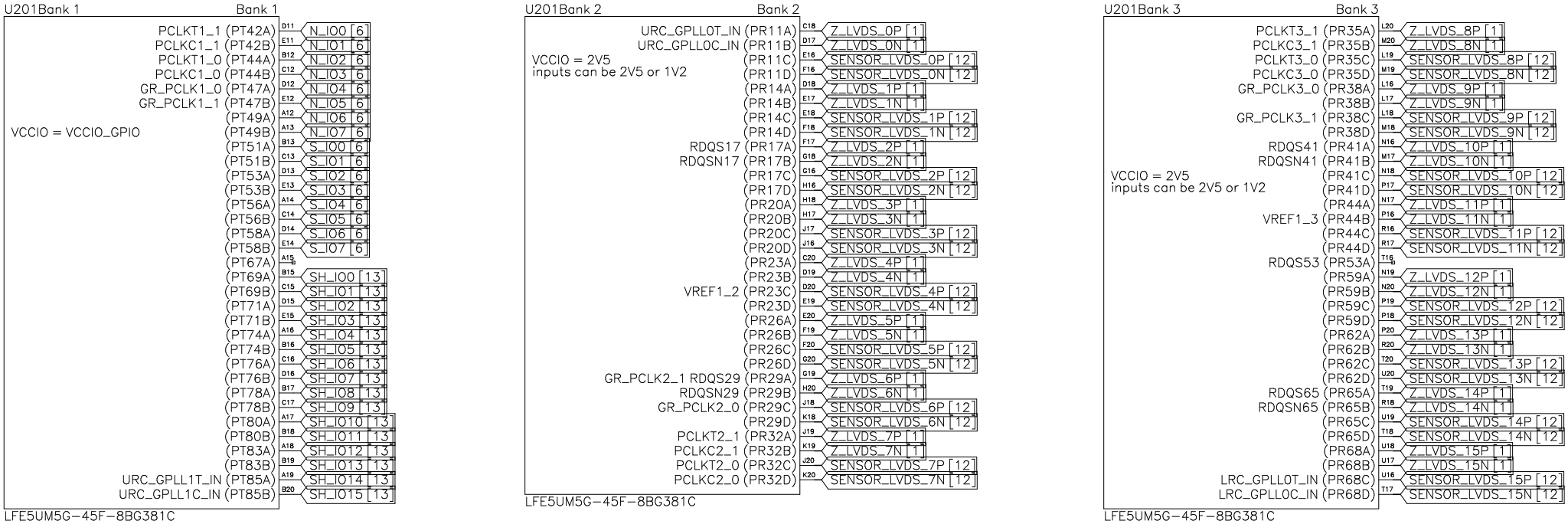
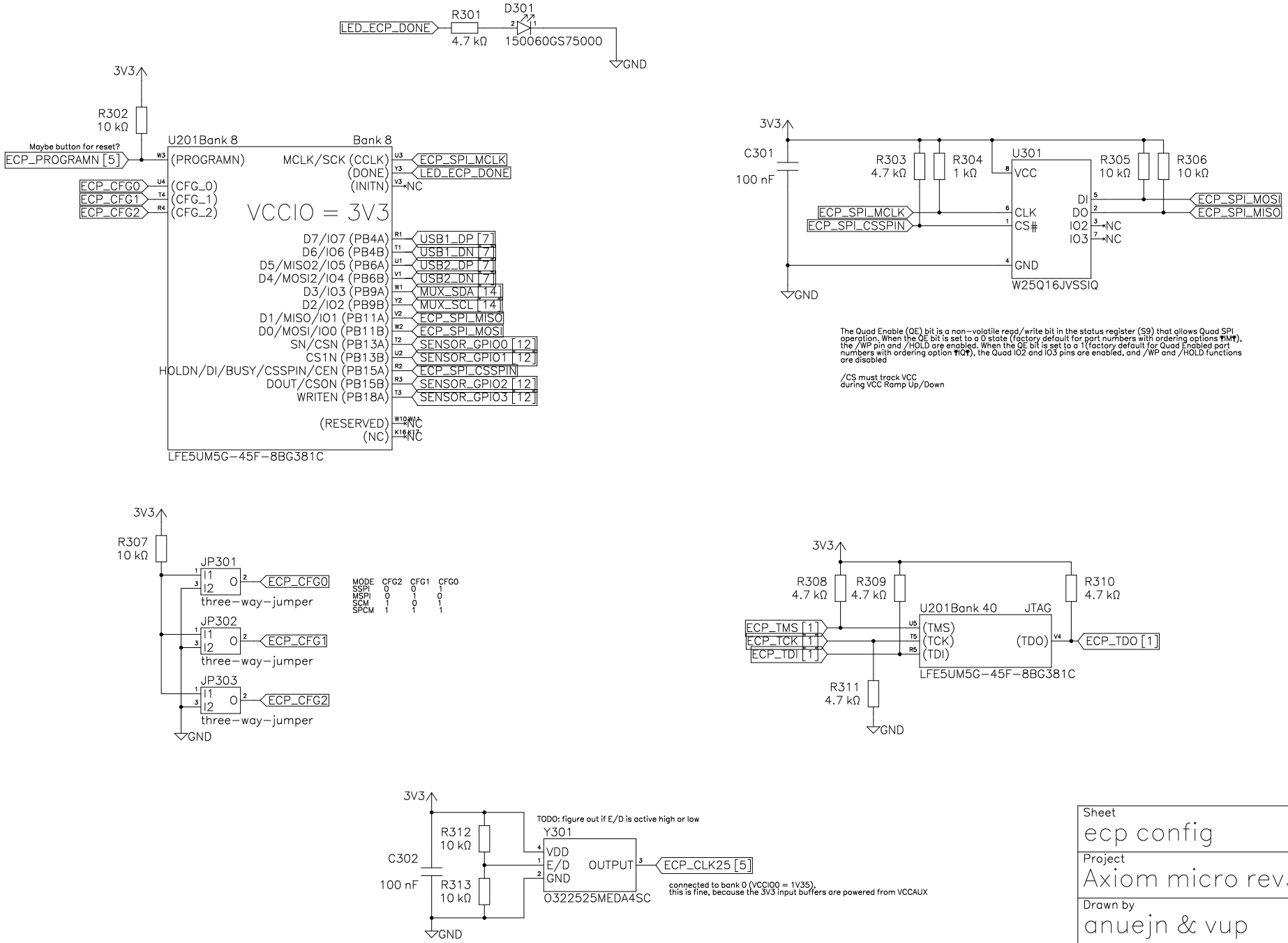


Sheet: zturn lite	Number: 1/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	
Date: 20200324	

open source hardware

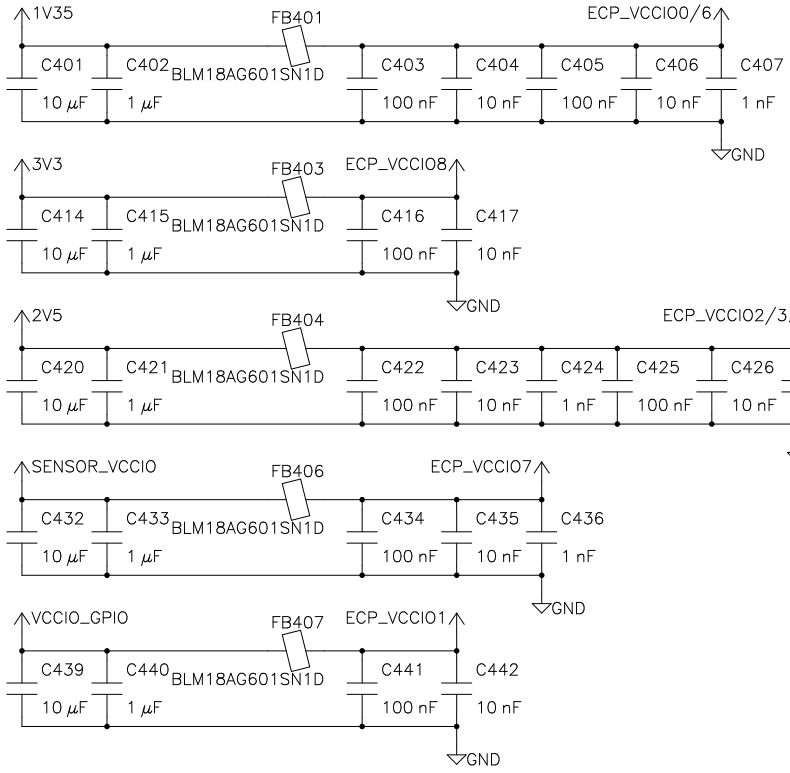


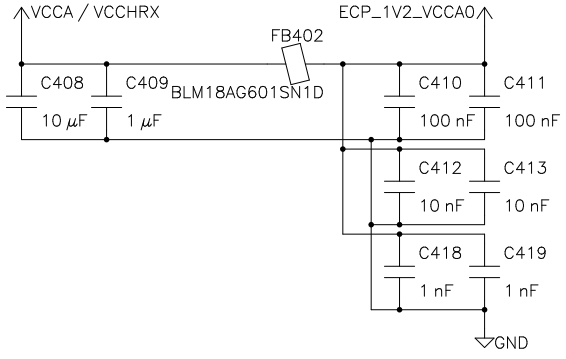
Sheet: ecp	Number: 2/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	
Date: 20200324	open source hardware

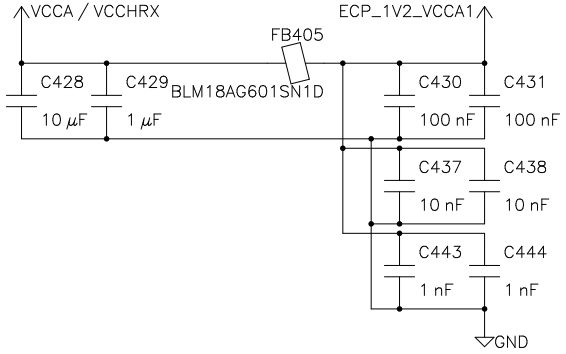


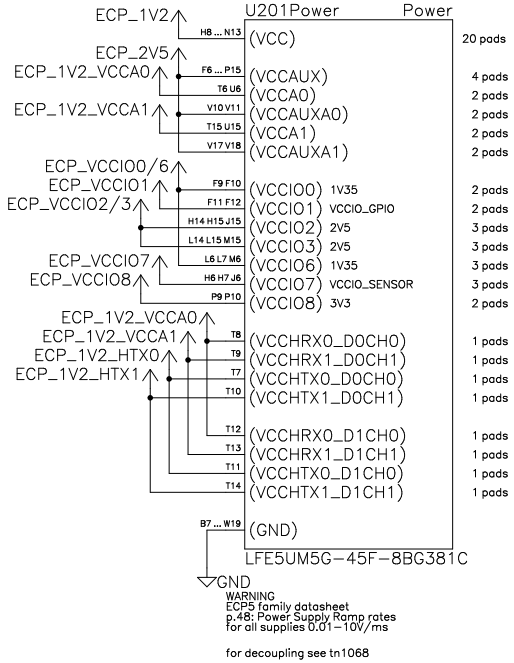
Sheet: ecp config	Number: 3/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	
Date: 20200324	open source hardware

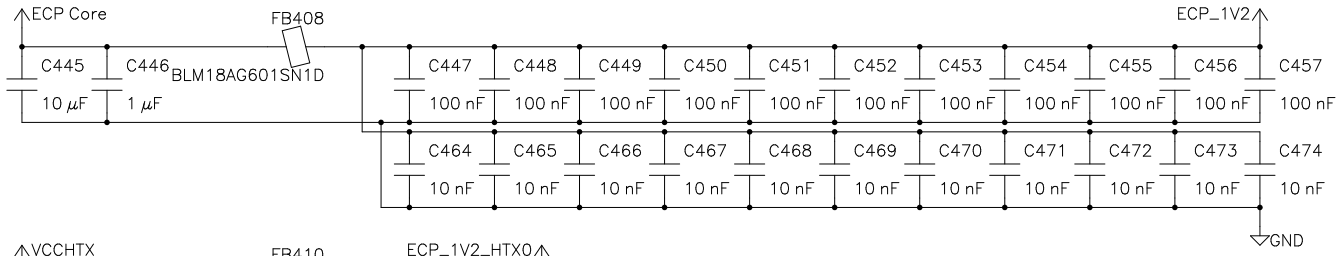
Place decoupling near FPGA, alternate 100n and 10n per pad per rail

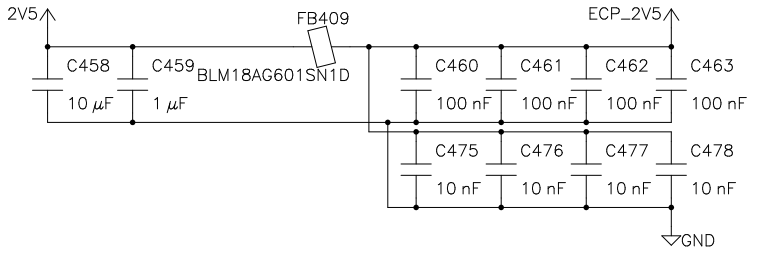


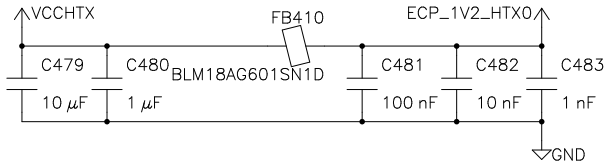


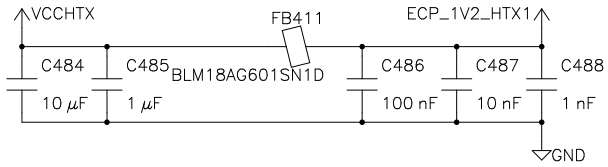




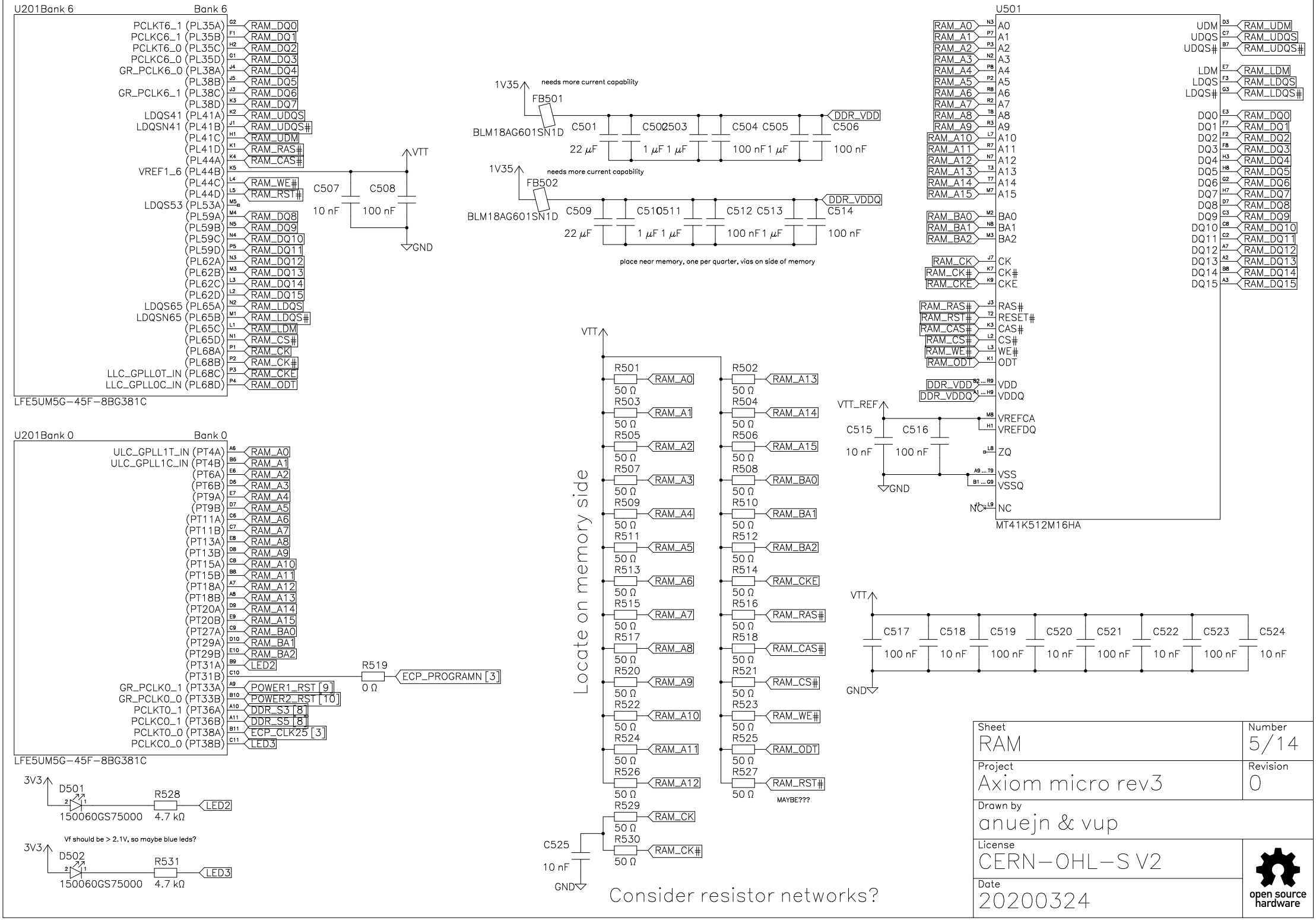








Sheet: ecp power	Number: 4/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	open source hardware
Date: 20200324	


U201Bank 6
Bank 6
PCLKT6_1 (PL35A) G2 RAM_DQ0
PCLKC6_1 (PL35B) F1 RAM_DQ1
PCLKT6_0 (PL35C) H2 RAM_DQ2
PCLKC6_0 (PL35D) G1 RAM_DQ3
GR_PCLK6_0 (PL38A) J4 RAM_DQ4
(PL38B) J5 RAM_DQ5
GR_PCLK6_1 (PL38C) J3 RAM_DQ6
(PL38D) K3 RAM_DQ7
LDQS41 (PL41A) K2 RAM_UDQS
LDQSN41 (PL41B) J1 RAM_UDQS#
(PL41C) H1 RAM_UDM
(PL41D) K1 RAM_RAS#
(PL44A) K4 RAM_CAS#
VREF1_6 (PL44B) K5
(PL44C) L4 RAM_WE#
(PL44D) L5 RAM_RST#
LDQS53 (PL53A) M5
(PL59A) M4 RAM_DQ8
(PL59B) N5 RAM_DQ9
(PL59C) N4 RAM_DQ10
(PL59D) P5 RAM_DQ11
(PL62A) N3 RAM_DQ12
(PL62B) M3 RAM_DQ13
(PL62C) L3 RAM_DQ14
(PL62D) L2 RAM_DQ15
LDQS65 (PL65A) N2 RAM_LDQS
LDQSN65 (PL65B) M1 RAM_LDQS#
(PL65C) L1 RAM_LDM
(PL65D) N1 RAM_CS#
(PL68A) P1 RAM_CK
(PL68B) P2 RAM_CK#
LLC_GPLL0T_IN (PL68C) P3 RAM_CKE
LLC_GPLL0C_IN (PL68D) P4 RAM_ODT
LFE5UM5G-45F-8BG381C
VTT
C507 10 nF
C508 100 nF
GND
U201Bank 0
Bank 0
ULC_GPLL1T_IN (PT4A) A6 RAM_A0
ULC_GPLL1C_IN (PT4B) B6 RAM_A1
(PT6A) E6 RAM_A2
(PT6B) D6 RAM_A3
(PT9A) E7 RAM_A4
(PT9B) D7 RAM_A5
(PT11A) C6 RAM_A6
(PT11B) C7 RAM_A7
(PT13A) E8 RAM_A8
(PT13B) D8 RAM_A9
(PT15A) C8 RAM_A10
(PT15B) B8 RAM_A11
(PT18A) A7 RAM_A12
(PT18B) A8 RAM_A13
(PT20A) D9 RAM_A14
(PT20B) E9 RAM_A15
(PT27A) C9 RAM_BA0
(PT29A) D10 RAM_BA1
(PT29B) E10 RAM_BA2
(PT31A) B9 LED2
(PT31B) C10
R519 0 Ω
ECP_PROGRAMN [3]
GR_PCLK0_1 (PT33A) A9 POWER1_RST [9]
GR_PCLK0_0 (PT33B) B10 POWER2_RST [10]
PCLKT0_1 (PT36A) A10 DDR_S3 [8]
PCLKC0_1 (PT36B) A11 DDR_S5 [8]
PCLKT0_0 (PT38A) B11 ECP_CLK25 [3]
PCLKC0_0 (PT38B) C11 LED3
LFE5UM5G-45F-8BG381C
3V3
D501
R528
150060GS75000
4.7 kΩ
LED2
Vf should be > 2.1V, so maybe blue leds?
3V3
D502
R531
150060GS75000
4.7 kΩ
LED3
1V35
needs more current capability
FB501
BLM18AG601SN1D
C501 22 µF
C502 1 µF
C503 1 µF
C504 100 nF
C505 1 µF
C506 100 nF
DDR_VDD
1V35
needs more current capability
FB502
BLM18AG601SN1D
C509 22 µF
C510 1 µF
C511 1 µF
C512 100 nF
C513 1 µF
C514 100 nF
DDR_VDDQ
place near memory, one per quarter, vias on side of memory
U501
RAM_A0 N3 A0
RAM_A1 P7 A1
RAM_A2 P3 A2
RAM_A3 N2 A3
RAM_A4 P8 A4
RAM_A5 P2 A5
RAM_A6 R8 A6
RAM_A7 R2 A7
RAM_A8 T8 A8
RAM_A9 R3 A9
RAM_A10 L7 A10
RAM_A11 R7 A11
RAM_A12 N7 A12
RAM_A13 T3 A13
RAM_A14 T7 A14
RAM_A15 M7 A15
RAM_BA0 M2 BA0
RAM_BA1 N8 BA1
RAM_BA2 M3 BA2
RAM_CK J7 CK
RAM_CK# K7 CK#
RAM_CKE K9 CKE
RAM_RAS# J3 RAS#
RAM_RST# T2 RESET#
RAM_CAS# K3 CAS#
RAM_CS# L2 CS#
RAM_WE# L3 WE#
RAM_ODT K1 ODT
DDR_VDD B2 ... R9 VDD
DDR_VDDQ A1 ... H9 VDDQ
M8 VREFCA
H1 VREFDQ
L8 ZQ
A9 ... T9 VSS
B1 ... G9 VSSQ
NC L9 NC
UDM D3 RAM_UDM
UDQS C7 RAM_UDQS
UDQS# B7 RAM_UDQS#
LDM E7 RAM_LDM
LDQS F3 RAM_LDQS
LDQS# G3 RAM_LDQS#
DQ0 E3 RAM_DQ0
DQ1 F7 RAM_DQ1
DQ2 F2 RAM_DQ2
DQ3 F8 RAM_DQ3
DQ4 H3 RAM_DQ4
DQ5 H8 RAM_DQ5
DQ6 G2 RAM_DQ6
DQ7 H7 RAM_DQ7
DQ8 D7 RAM_DQ8
DQ9 C3 RAM_DQ9
DQ10 C8 RAM_DQ10
DQ11 C2 RAM_DQ11
DQ12 A7 RAM_DQ12
DQ13 A2 RAM_DQ13
DQ14 B8 RAM_DQ14
DQ15 A3 RAM_DQ15
MT41K512M16HA
VTT_REF
C515 10 nF
C516 100 nF
GND
VTT
Locate on memory side
R501 50 Ω RAM_A0
R502 50 Ω RAM_A13
R503 50 Ω RAM_A1
R504 50 Ω RAM_A14
R505 50 Ω RAM_A2
R506 50 Ω RAM_A15
R507 50 Ω RAM_A3
R508 50 Ω RAM_BA0
R509 50 Ω RAM_A4
R510 50 Ω RAM_BA1
R511 50 Ω RAM_A5
R512 50 Ω RAM_BA2
R513 50 Ω RAM_A6
R514 50 Ω RAM_CKE
R515 50 Ω RAM_A7
R516 50 Ω RAM_RAS#
R517 50 Ω RAM_A8
R518 50 Ω RAM_CAS#
R520 50 Ω RAM_A9
R521 50 Ω RAM_CS#
R522 50 Ω RAM_A10
R523 50 Ω RAM_WE#
R524 50 Ω RAM_A11
R525 50 Ω RAM_ODT
R526 50 Ω RAM_A12
R527 50 Ω RAM_RST#
MAYBE???
R529 50 Ω RAM_CK
R530 50 Ω RAM_CK#
C525 10 nF
GND
Consider resistor networks?
VTT
C517 100 nF
C518 10 nF
C519 100 nF
C520 10 nF
C521 100 nF
C522 10 nF
C523 100 nF
C524 10 nF
GND
Sheet
RAM
Number
5/14
Project
Axiom micro rev3
Revision
0
Drawn by
anuejn & vup
License
CERN-OHL-S V2
Date
20200324
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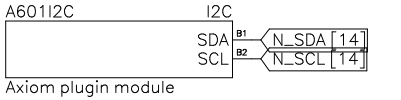
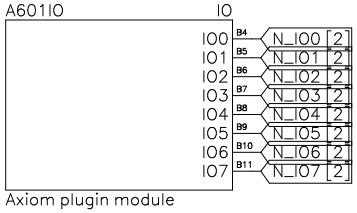
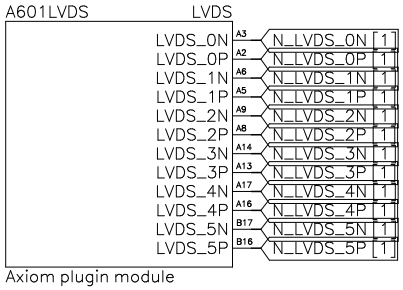
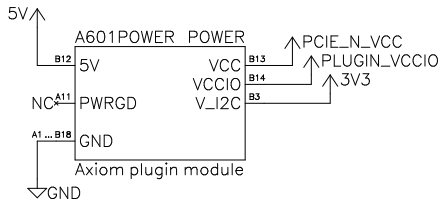
plugin north

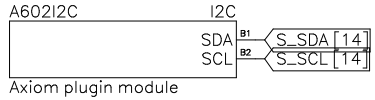


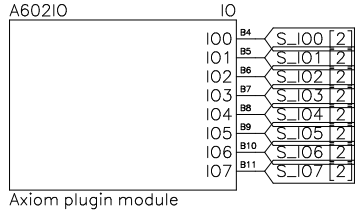


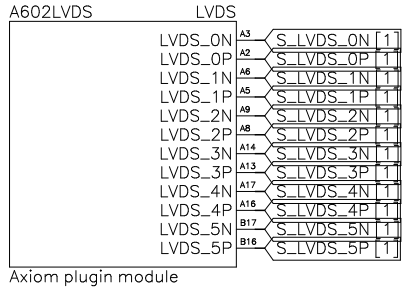


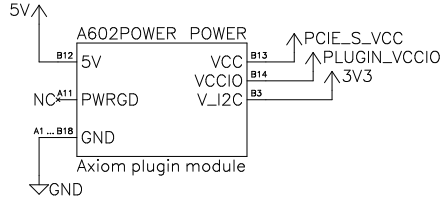


plugin south









Sheet plugin	Number 6/14
Project Axiom micro rev3	Revision 0
Drawn by anuejn & vup	
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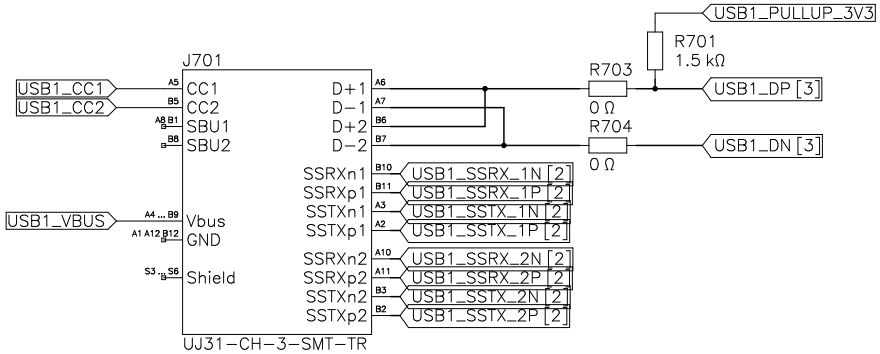
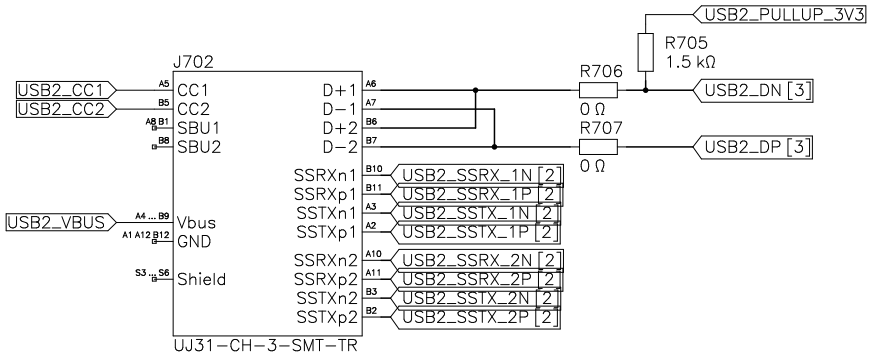
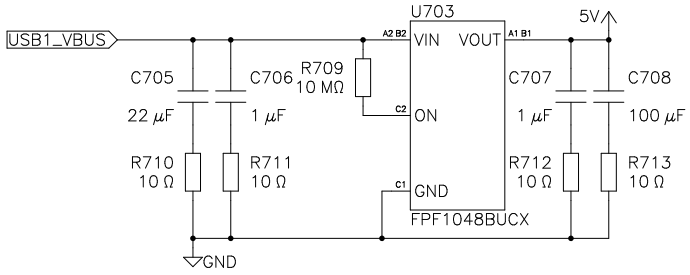
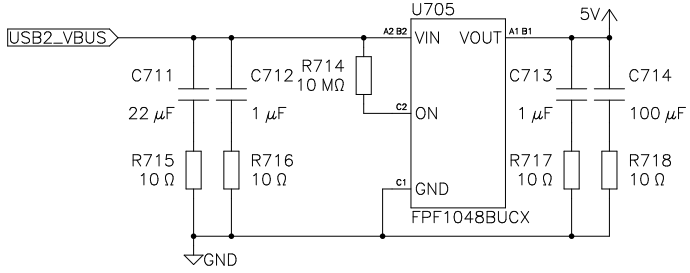
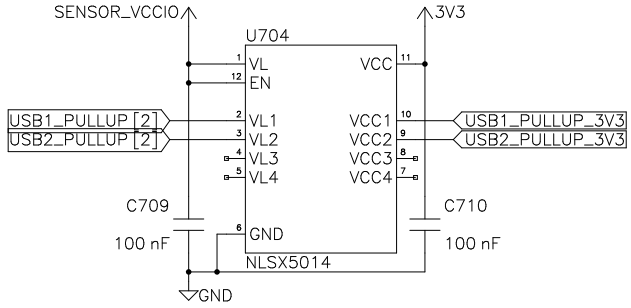
Date 20200324	

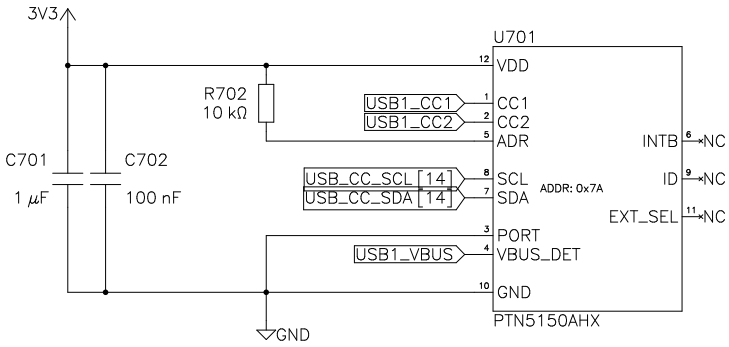


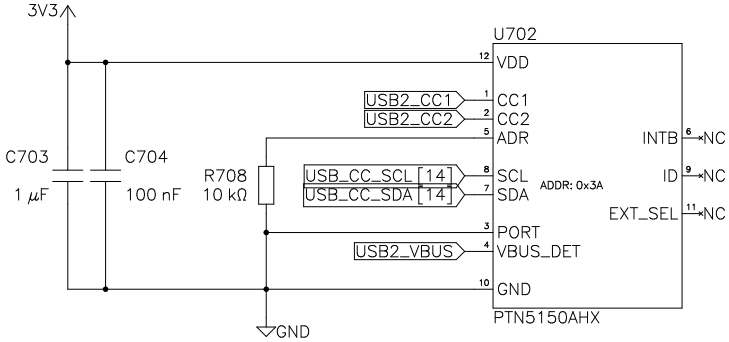












PORT= VDD: DFP mode (R_D = 80uA power default for non−I2C mode).
PORT = Mid (or floating): DRP mode
PORT=GND: UFP mode

Trinary GPIO Input ADR pin run from VDD
– ADR pull up to VDD with 10 kΩ resistor (I2C Enabled with ADDR bit 6 equal to 1, I2C Address 0x7A)
– ADR pull down to GND with 10 kΩ resistor. (I2C Enabled with ADDR bit 6 equal to 0, I2C Address 0x3A)
– ADR = Mid or floating (Pin 6/7/8) configured as OUT1/2/3 in non−I2C mode

Sheet: USB	Number: 7/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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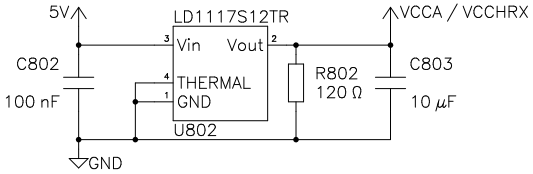
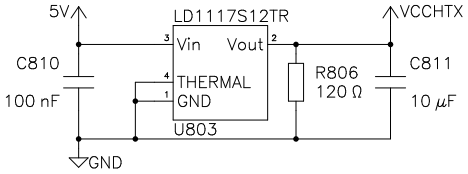
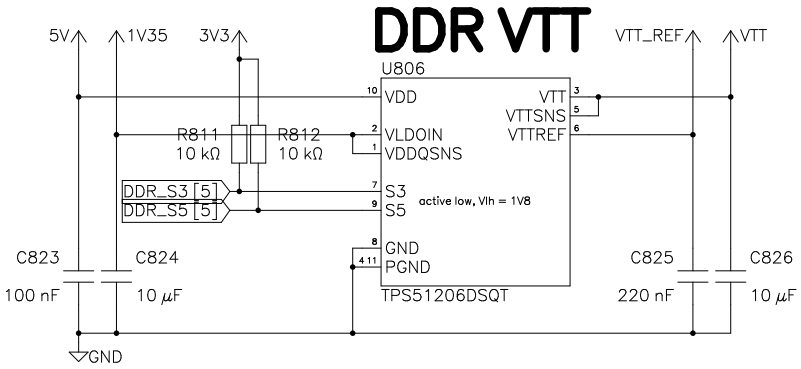
Date: 20200324	open source hardware



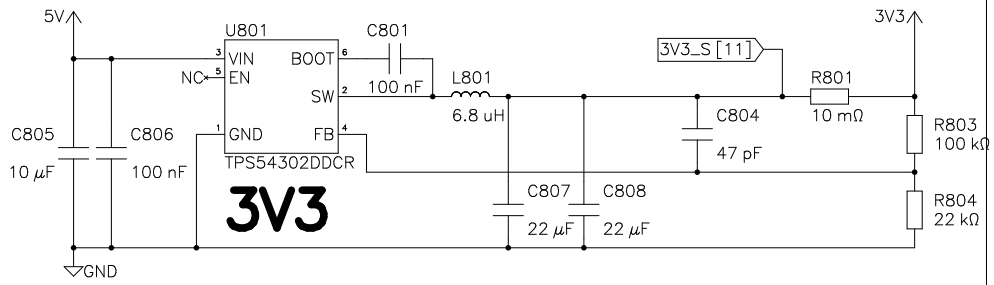
1V2 VCCA / VCCHRX

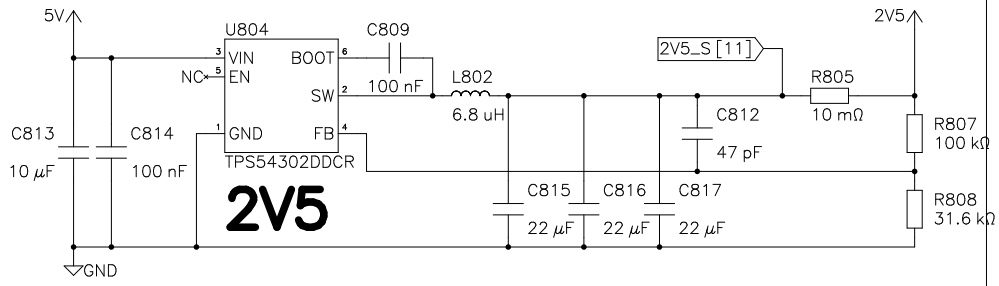


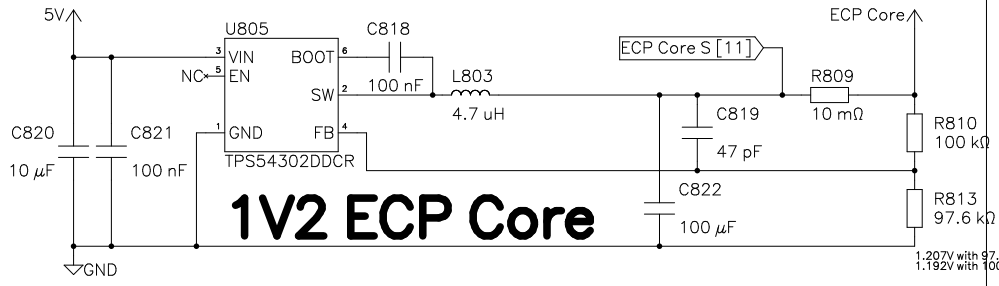
1V2 VCCHTX



positive terminal of the VTT pin output capacitor(s) as a separate trace from the high–current path from VTT. Consider adding a low–pass R–C filter at the VTTSNS pin in case the ESR of the VTT output capacitor(s) is larger than 2 mΩ. The R–C filter time constant should be approximately the same or slightly lower than the time constant of the VTT output capacitance and ESR.







1.207V with 97.6
1.192V with 100

Sheet: power fixed	Number: 8/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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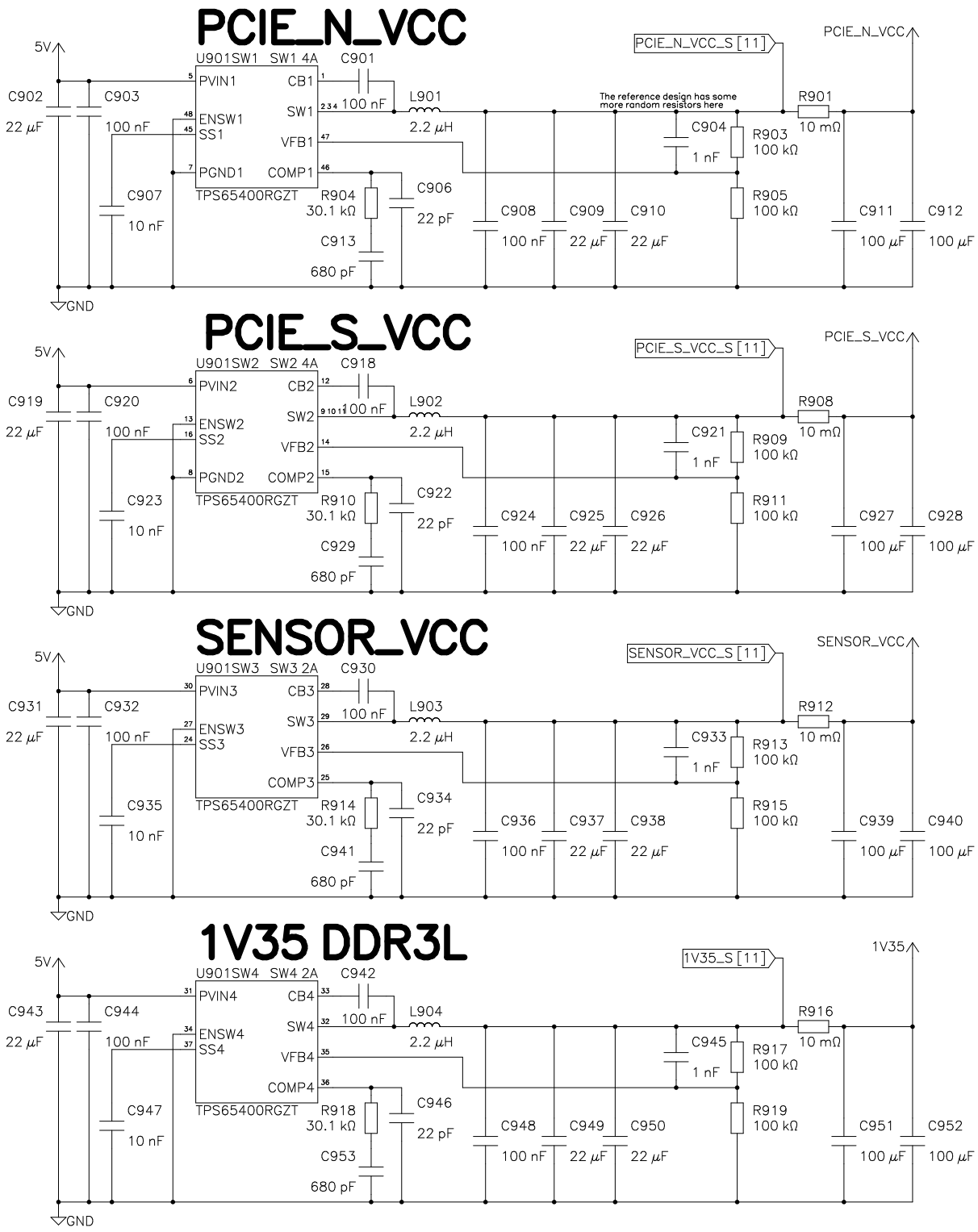
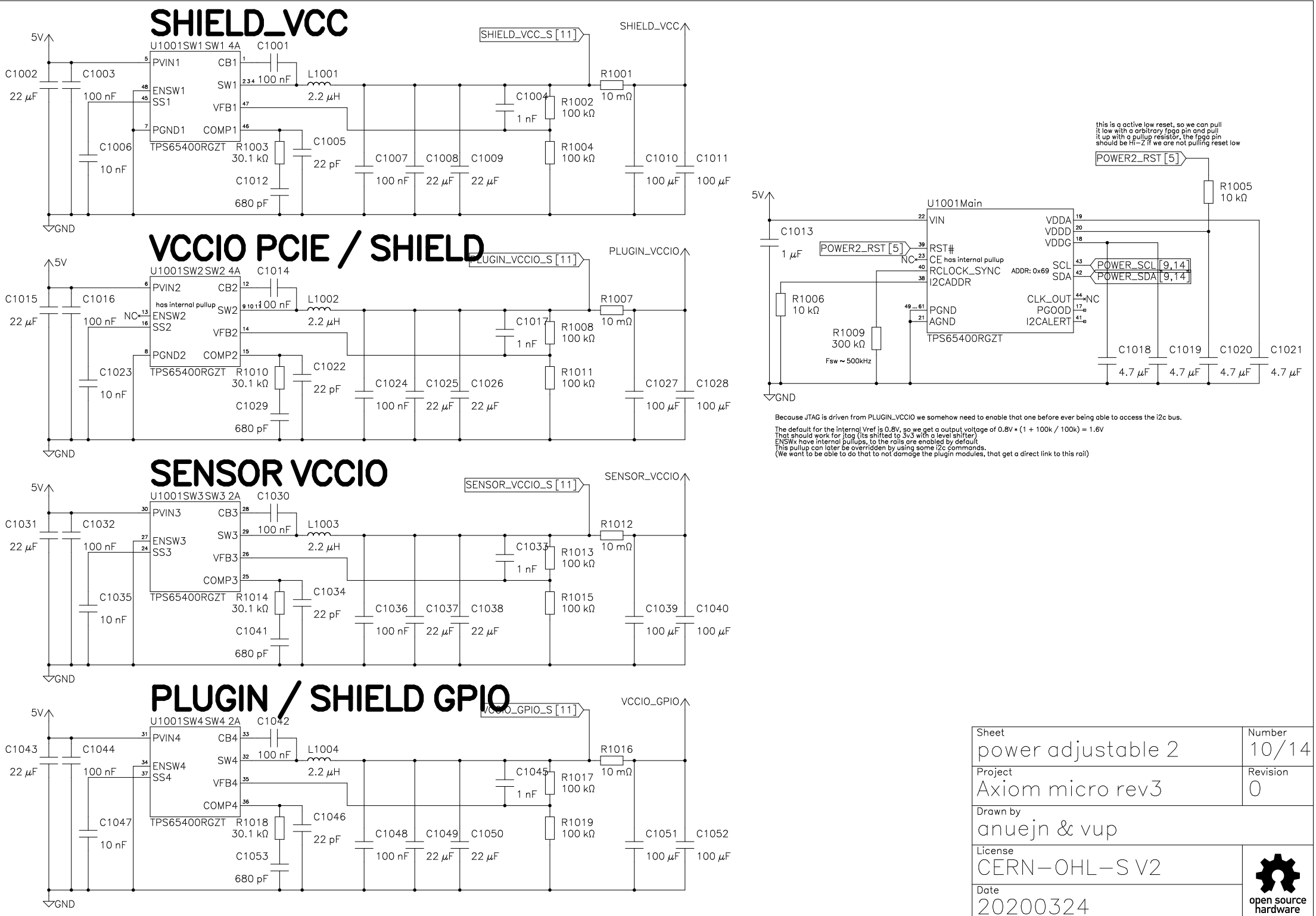
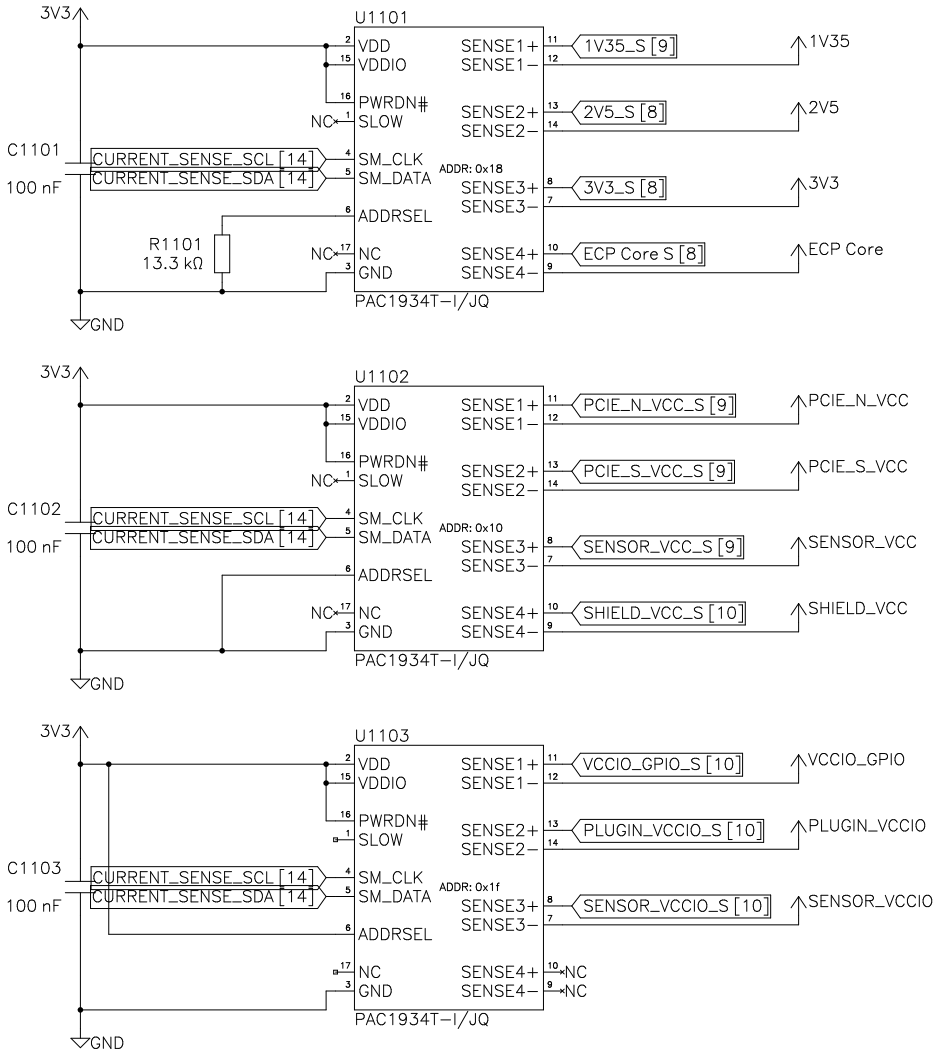
Date: 20200324	



Sheet: power adjustable 1	Number: 9/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	
Date: 20200324	open source hardware


SHIELD_VCC
5V
U1001SW1 SW1 4A
PVIN1
ENSW1
SS1
PGND1
TPS65400RGZT
CB1
SW1
VFB1
COMP1
C1001
100 nF
L1001
2.2 µH
SHIELD_VCC_S [11]
SHIELD_VCC
R1001
10 mΩ
C1002
22 µF
C1003
100 nF
C1004
1 nF
R1002
100 kΩ
C1005
22 pF
C1006
10 nF
R1003
30.1 kΩ
C1012
680 pF
R1004
100 kΩ
C1007
100 nF
C1008
22 µF
C1009
22 µF
C1010
100 µF
C1011
100 µF
GND
VCCIO PCIE / SHIELD
U1001SW2 SW2 4A
PVIN2
has internal pullup
NC
ENSW2
SS2
PGND2
CB2
SW2
VFB2
COMP2
C1014
L1002
PLUGIN_VCCIO_S [11]
PLUGIN_VCCIO
R1007
C1015
C1016
C1017
R1008
C1023
R1010
C1022
C1029
R1011
C1024
C1025
C1026
C1027
C1028
SENSOR VCCIO
U1001SW3 SW3 2A
PVIN3
ENSW3
SS3
CB3
SW3
VFB3
COMP3
C1030
L1003
SENSOR_VCCIO_S [11]
SENSOR_VCCIO
R1012
C1031
C1032
C1033
R1013
C1035
R1014
C1034
C1041
R1015
C1036
C1037
C1038
C1039
C1040
PLUGIN / SHIELD GPIO
U1001SW4 SW4 2A
PVIN4
ENSW4
SS4
CB4
SW4
VFB4
COMP4
C1042
L1004
VCCIO_GPIO_S [11]
VCCIO_GPIO
R1016
C1043
C1044
C1045
R1017
C1047
R1018
C1046
C1053
R1019
C1048
C1049
C1050
C1051
C1052
this is a active low reset, so we can pull it low with a arbitrary fpga pin and pull it up with a pullup resistor, the fpga pin should be Hi-Z if we are not pulling reset low
POWER2_RST [5]
R1005
10 kΩ
U1001Main
VIN
RST#
CE has internal pullup
RCLOCK_SYNC
I2CADDR
ADDR: 0x69
PGND
AGND
VDDA
VDDD
VDDG
SCL
SDA
CLK_OUT
PGOOD
I2CALERT
POWER_SCL [9,14]
POWER_SDA [9,14]
C1013
1 µF
R1006
10 kΩ
R1009
300 kΩ
Fsw ~ 500kHz
C1018
C1019
C1020
C1021
4.7 µF
Because JTAG is driven from PLUGIN_VCCIO we somehow need to enable that one before ever being able to access the i2c bus.
The default for the internal Vref is 0.8V, so we get a output voltage of 0.8V * (1 + 100k / 100k) = 1.6V
That should work for jtag (its shifted to 3v3 with a level shifter)
ENSWx have internal pullups, to the rails are enabled by default
This pullup can later be overridden by using some i2c commands.
(We want to be able to do that to not damage the plugin modules, that get a direct link to this rail)
Sheet
power adjustable 2
Number
10/14
Project
Axiom micro rev3
Revision
0
Drawn by
anuejn & vup
License
CERN-OHL-S V2
Date
20200324
open source hardware

current sense resistors: 0805W8F100MT5E or CS05W8F100MT5E



Sheet: current sense	Number: 11/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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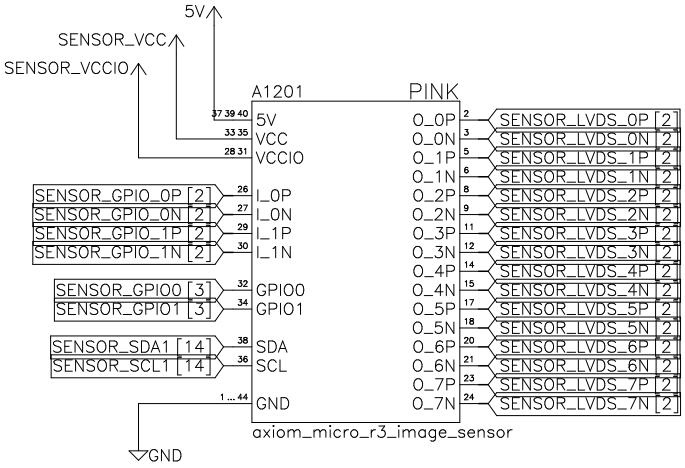

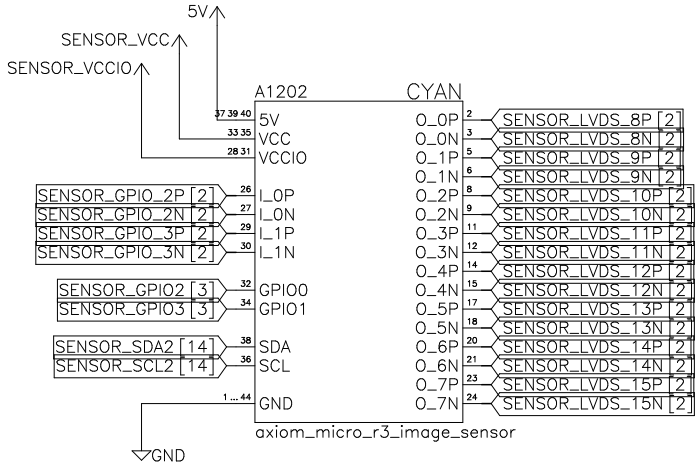

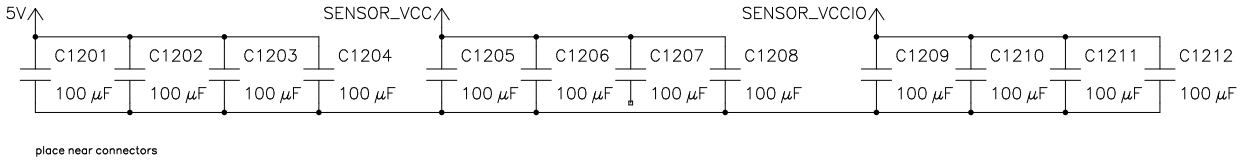

Sheet: image sensor	Number: 12/14
Project: Axiom micro rev3	Revision: 0
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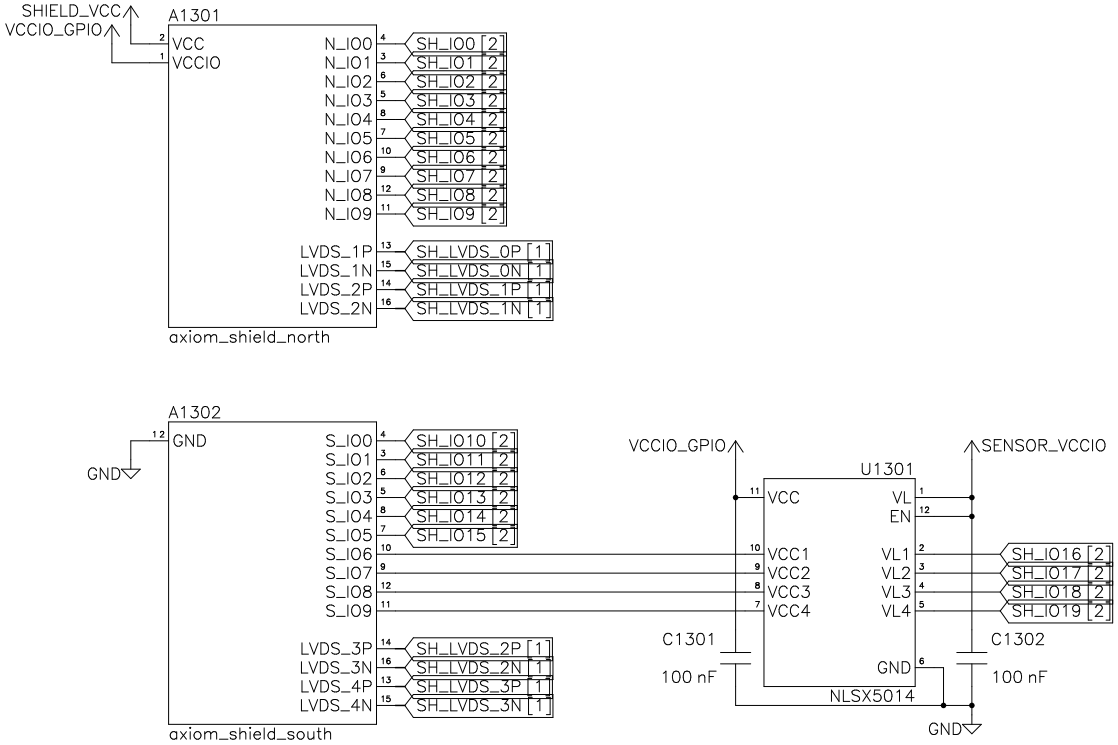

Sheet: shield	Number: 13/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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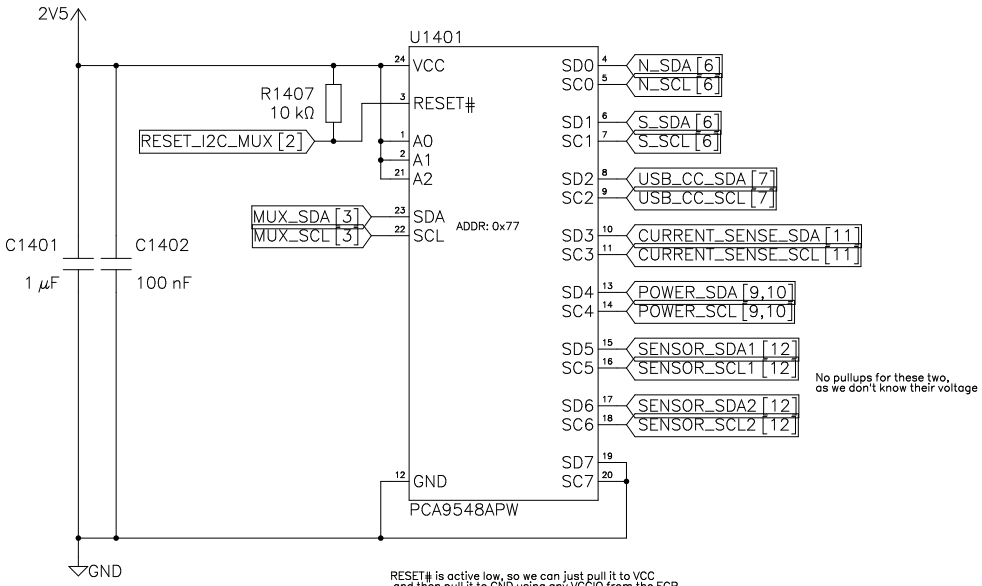
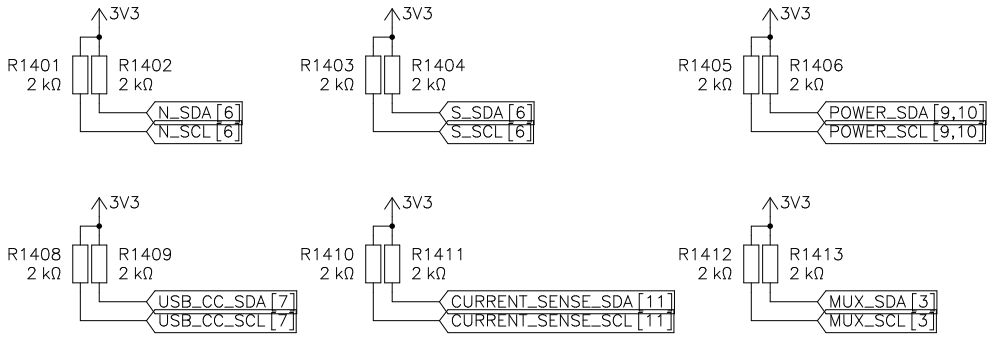
Date: 20200324	

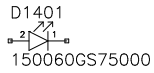


RESET# is active low, so we can just pull it to VCC
and then pull it to GND using any VCCIO from the ECP,
attention has to be paid to not make RESET# get over VCC,
as otherwise current flows from the RESET pin to the VCC pin,
this should be accomplishable by just making the fpga output Hi-Z
if it is not pullen low

2V5 VCC means about 1V8 voltage clamping by the pass through transistors
That sholud work for most applications, we just need to be careful with nothing with 1V2 is on the bus

Unused channels have to be tied to GND or VCC





Sheet: i2c mux	Number: 14/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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Date: 20200324	