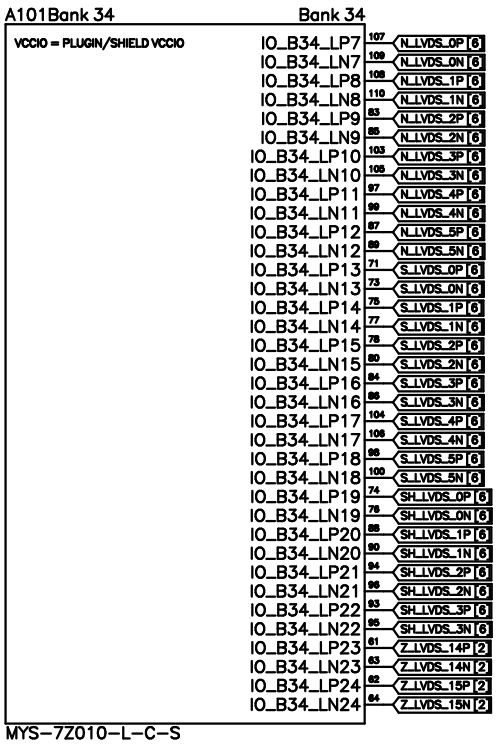
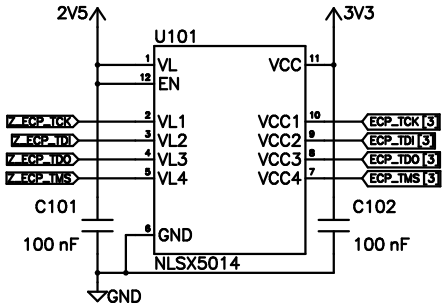
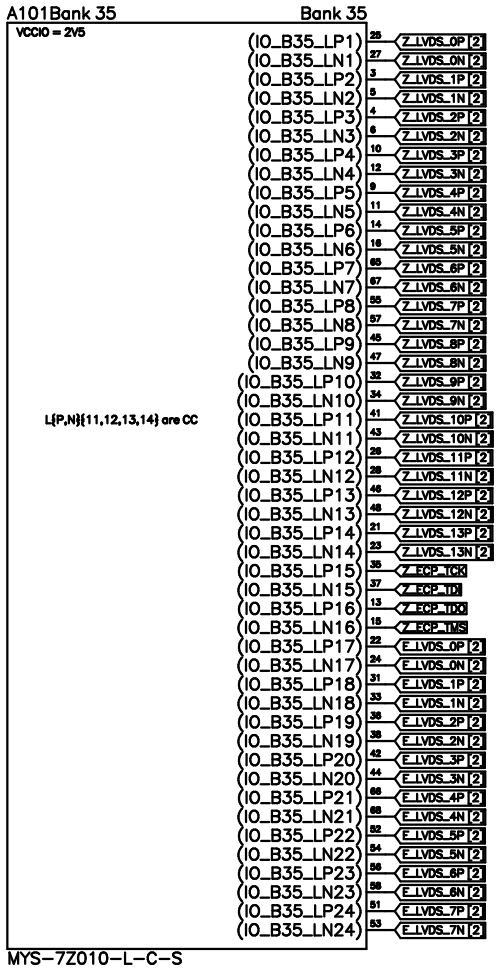
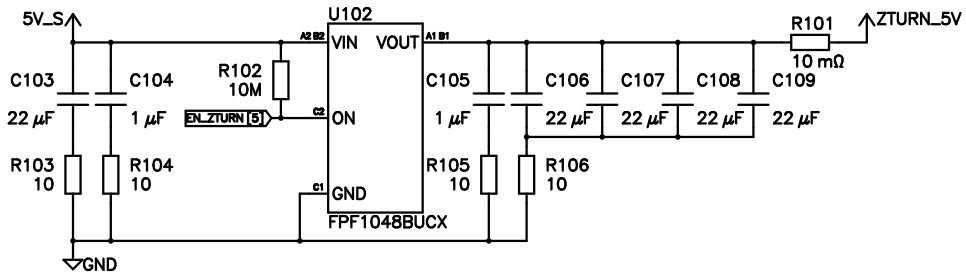
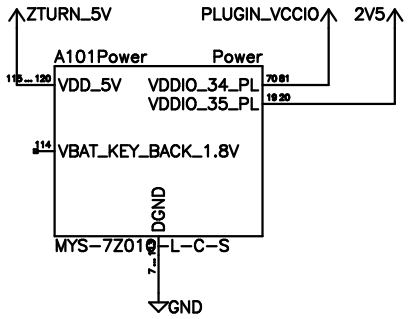
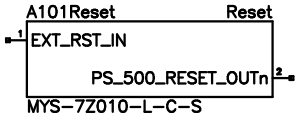




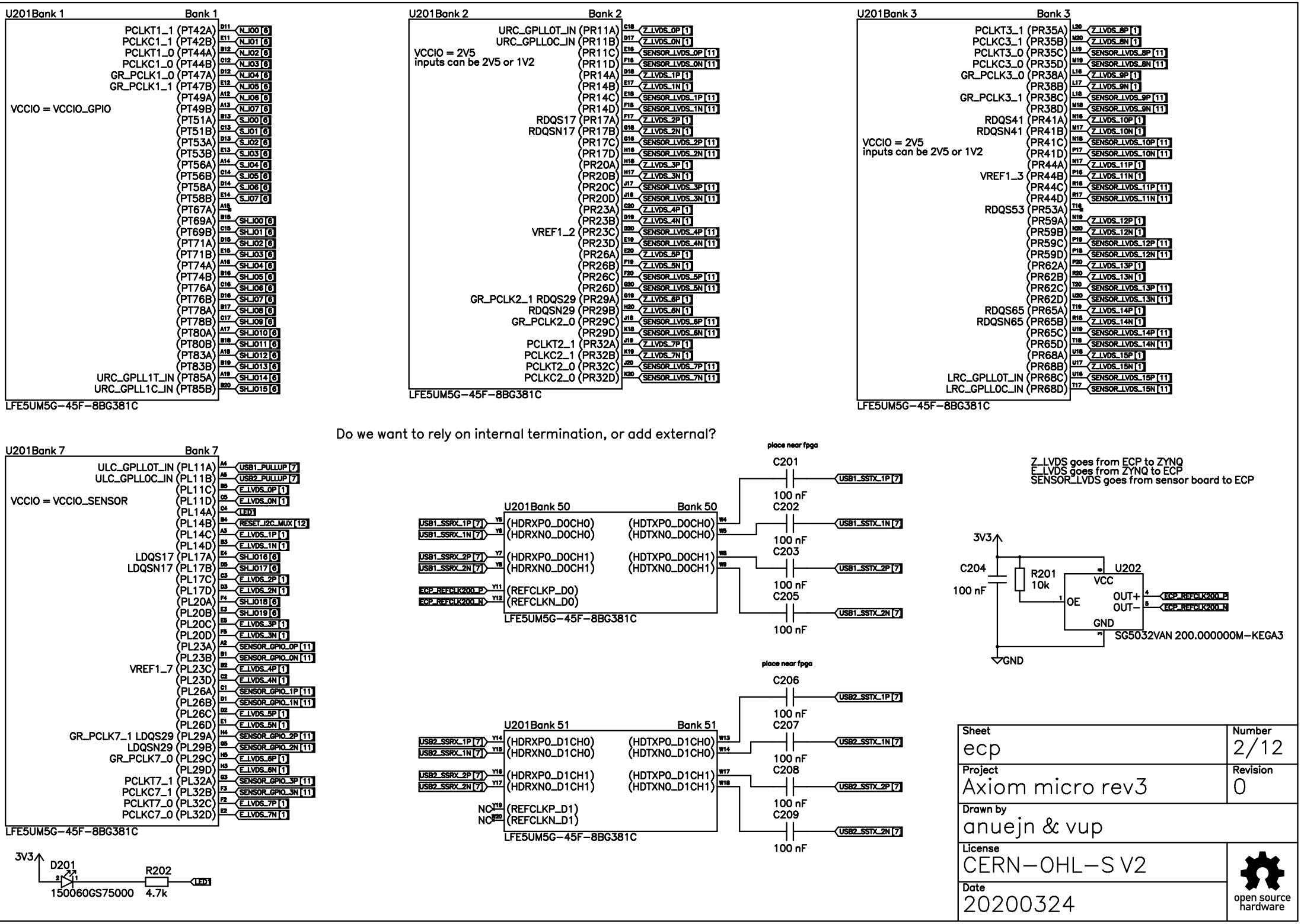


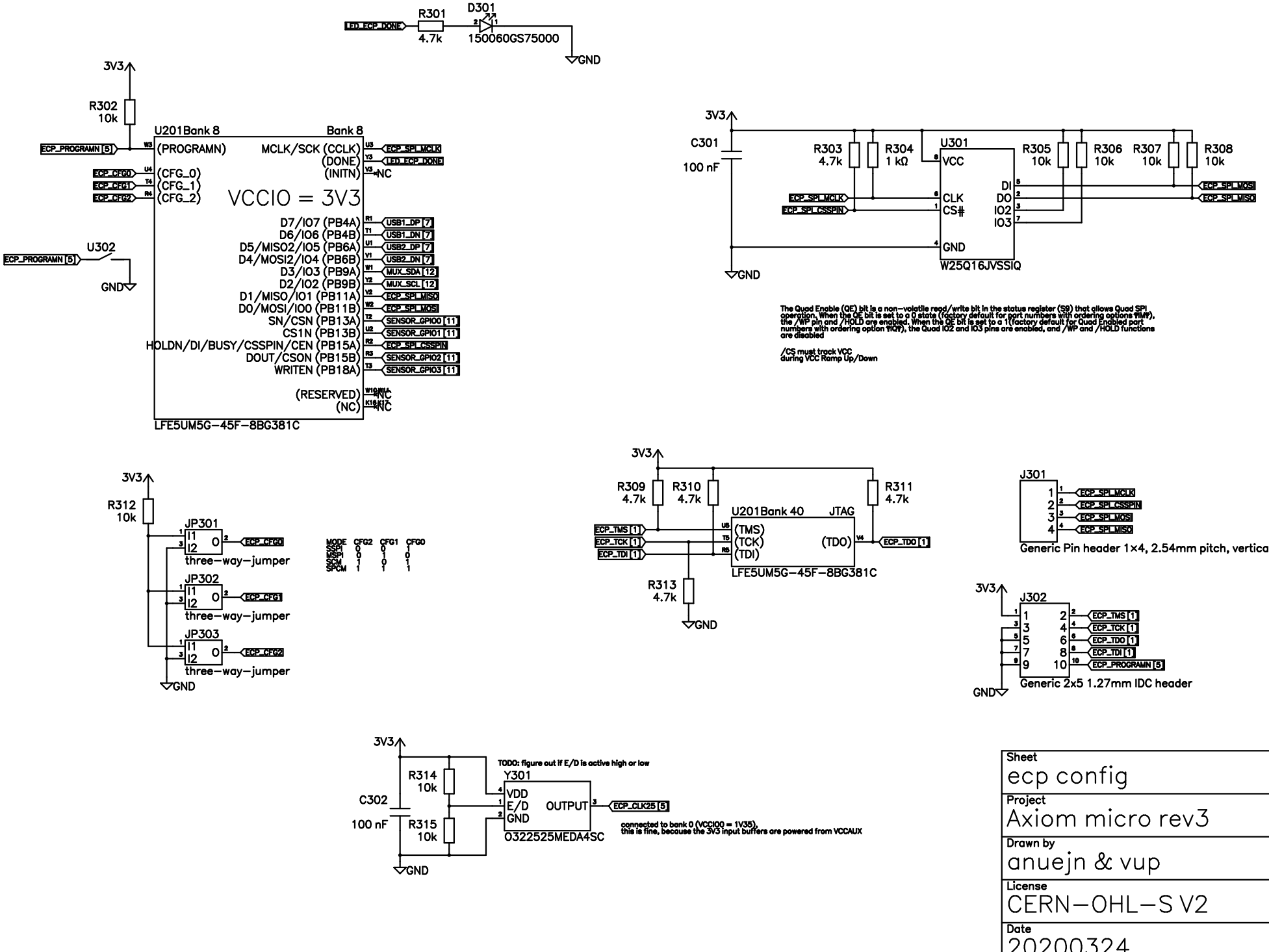






Sheet: zturn lite	Number: 1/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	open source hardware
Date: 20200324	


U201Bank 1
Bank 1
PCLKT1_1 (PT42A)
PCLKC1_1 (PT42B)
PCLKT1_0 (PT44A)
PCLKC1_0 (PT44B)
GR_PCLK1_0 (PT47A)
GR_PCLK1_1 (PT47B)
(PT49A)
VCCIO = VCCIO_GPIO
(PT49B)
(PT51A)
(PT51B)
(PT53A)
(PT53B)
(PT56A)
(PT56B)
(PT58A)
(PT58B)
(PT67A)
(PT69A)
(PT69B)
(PT71A)
(PT71B)
(PT74A)
(PT74B)
(PT76A)
(PT76B)
(PT78A)
(PT78B)
(PT80A)
(PT80B)
(PT83A)
(PT83B)
URC_GPLL1T_IN (PT85A)
URC_GPLL1C_IN (PT85B)
LFE5UM5G-45F-8BG381C
U201Bank 2
Bank 2
URC_GPLL0T_IN (PR11A)
URC_GPLL0C_IN (PR11B)
VCCIO = 2V5
inputs can be 2V5 or 1V2
(PR11C)
(PR11D)
(PR14A)
(PR14B)
(PR14C)
(PR14D)
RDQS17 (PR17A)
RDQSN17 (PR17B)
(PR17C)
(PR17D)
(PR20A)
(PR20B)
(PR20C)
(PR20D)
(PR23A)
(PR23B)
VREF1_2 (PR23C)
(PR23D)
(PR26A)
(PR26B)
(PR26C)
(PR26D)
GR_PCLK2_1 RDQS29 (PR29A)
RDQSN29 (PR29B)
GR_PCLK2_0 (PR29C)
(PR29D)
PCLKT2_1 (PR32A)
PCLKC2_1 (PR32B)
PCLKT2_0 (PR32C)
PCLKC2_0 (PR32D)
LFE5UM5G-45F-8BG381C
U201Bank 3
Bank 3
PCLKT3_1 (PR35A)
PCLKC3_1 (PR35B)
PCLKT3_0 (PR35C)
PCLKC3_0 (PR35D)
GR_PCLK3_0 (PR38A)
(PR38B)
GR_PCLK3_1 (PR38C)
(PR38D)
RDQS41 (PR41A)
RDQSN41 (PR41B)
VCCIO = 2V5
inputs can be 2V5 or 1V2
(PR41C)
(PR41D)
(PR44A)
VREF1_3 (PR44B)
(PR44C)
(PR44D)
RDQS53 (PR53A)
(PR59A)
(PR59B)
(PR59C)
(PR59D)
(PR62A)
(PR62B)
(PR62C)
(PR62D)
RDQS65 (PR65A)
RDQSN65 (PR65B)
(PR65C)
(PR65D)
(PR68A)
(PR68B)
LRC_GPLL0T_IN (PR68C)
LRC_GPLL0C_IN (PR68D)
LFE5UM5G-45F-8BG381C
Do we want to rely on internal termination, or add external?
U201Bank 7
Bank 7
ULC_GPLL0T_IN (PL11A)
ULC_GPLL0C_IN (PL11B)
(PL11C)
VCCIO = VCCIO_SENSOR
(PL11D)
(PL14A)
(PL14B)
(PL14C)
(PL14D)
LDQS17 (PL17A)
LDQSN17 (PL17B)
(PL17C)
(PL17D)
(PL20A)
(PL20B)
(PL20C)
(PL20D)
(PL23A)
(PL23B)
VREF1_7 (PL23C)
(PL23D)
(PL26A)
(PL26B)
(PL26C)
(PL26D)
GR_PCLK7_1 LDQS29 (PL29A)
LDQSN29 (PL29B)
GR_PCLK7_0 (PL29C)
(PL29D)
PCLKT7_1 (PL32A)
PCLKC7_1 (PL32B)
PCLKT7_0 (PL32C)
PCLKC7_0 (PL32D)
LFE5UM5G-45F-8BG381C
3V3
D201
150060GS75000
R202
4.7k
LED1
place near fpga
C201
C202
C203
C205
100 nF
U201Bank 50
Bank 50
(HDRXP0_D0CH0)
(HDRXN0_D0CH0)
(HDRXP0_D0CH1)
(HDRXN0_D0CH1)
(REFCLKP_D0)
(REFCLKN_D0)
(HDTXP0_D0CH0)
(HDTXN0_D0CH0)
(HDTXP0_D0CH1)
(HDTXN0_D0CH1)
LFE5UM5G-45F-8BG381C
place near fpga
C206
C207
C208
C209
100 nF
U201Bank 51
Bank 51
(HDRXP0_D1CH0)
(HDRXN0_D1CH0)
(HDRXP0_D1CH1)
(HDRXN0_D1CH1)
NC
NC
(REFCLKP_D1)
(REFCLKN_D1)
(HDTXP0_D1CH0)
(HDTXN0_D1CH0)
(HDTXP0_D1CH1)
(HDTXN0_D1CH1)
LFE5UM5G-45F-8BG381C
Z_LVDS goes from ECP to ZYNQ
E_LVDS goes from ZYNQ to ECP
SENSOR_LVDS goes from sensor board to ECP
3V3
C204
100 nF
R201
10k
U202
VCC
OE
GND
OUT+
OUT-
SG5032VAN 200.000000M-KEGA3
GND
Sheet
ecp
Number
2/12
Project
Axiom micro rev3
Revision
0
Drawn by
anuejn & vup
License
CERN-OHL-S V2
Date
20200324
open source hardware



Sheet: ecp config	Number: 3/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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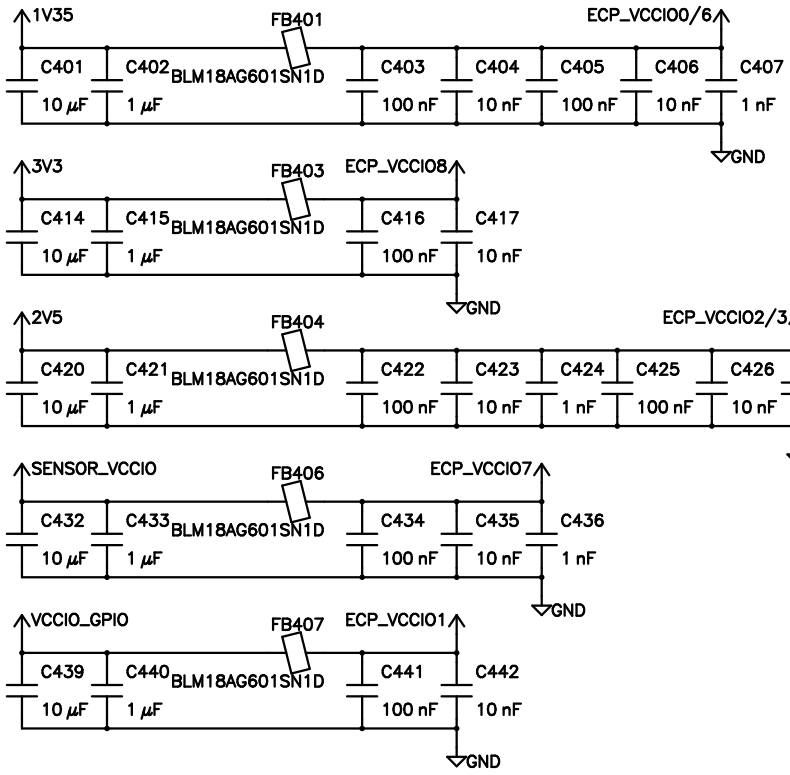
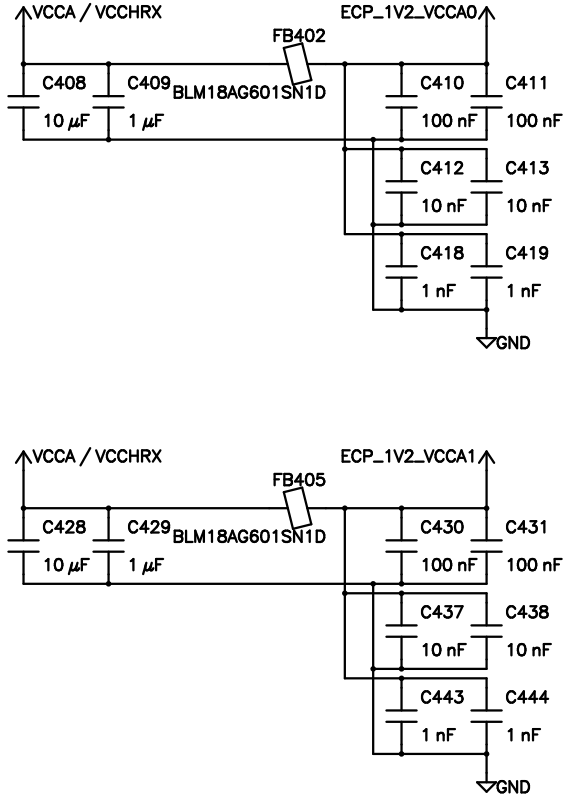
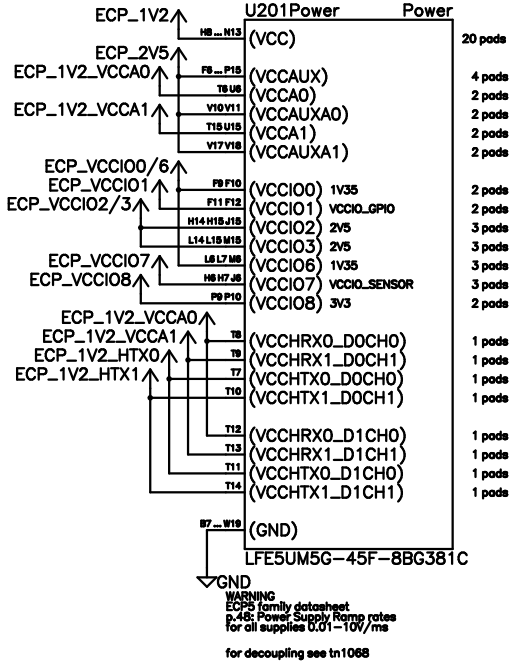
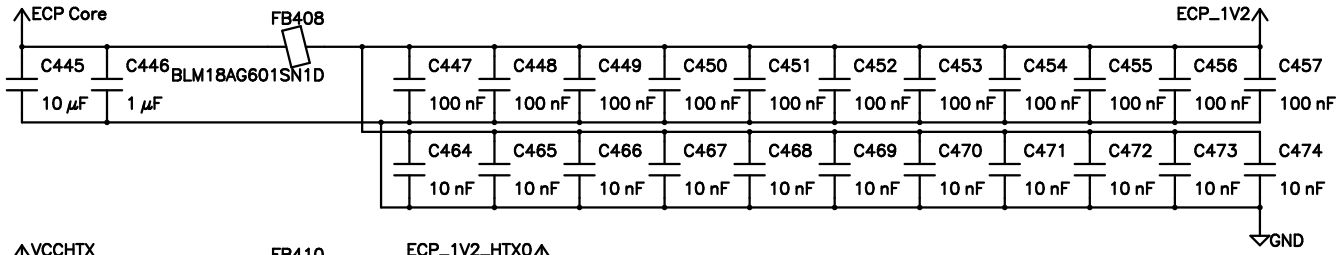
Date: 20200324	

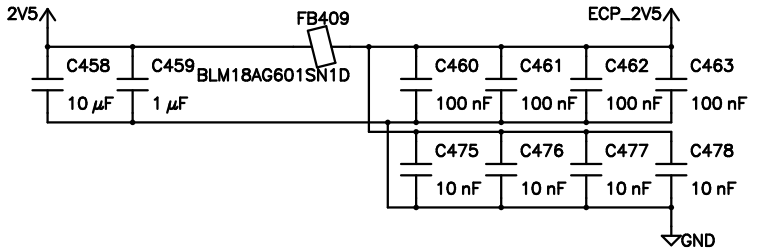
Place decoupling near FPGA, alternate 100n and 10n per pad per rail

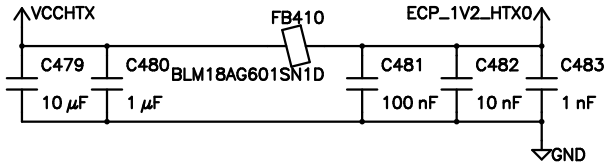


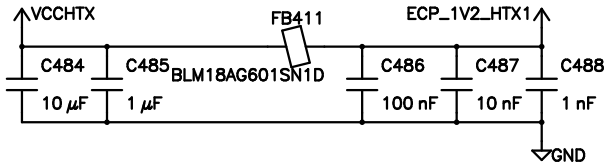




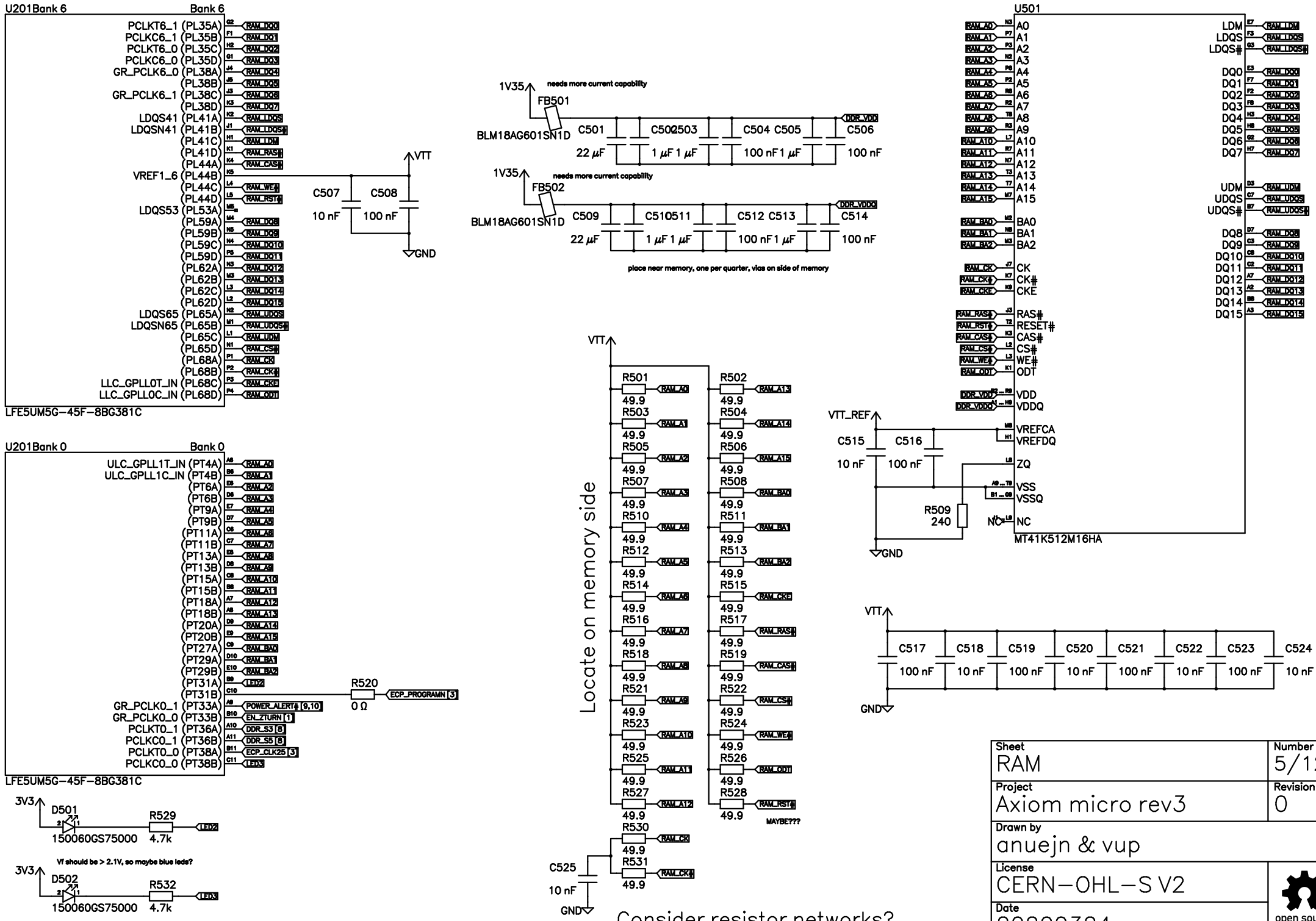




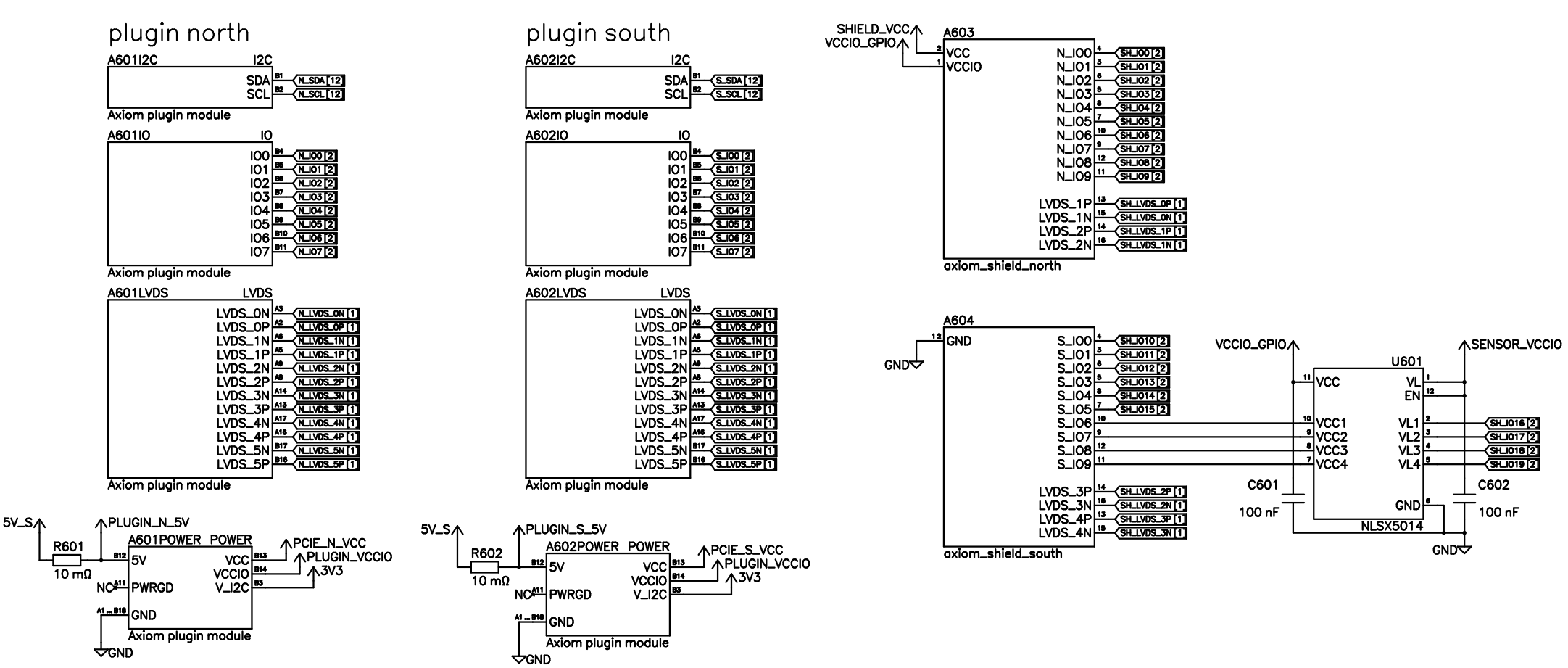




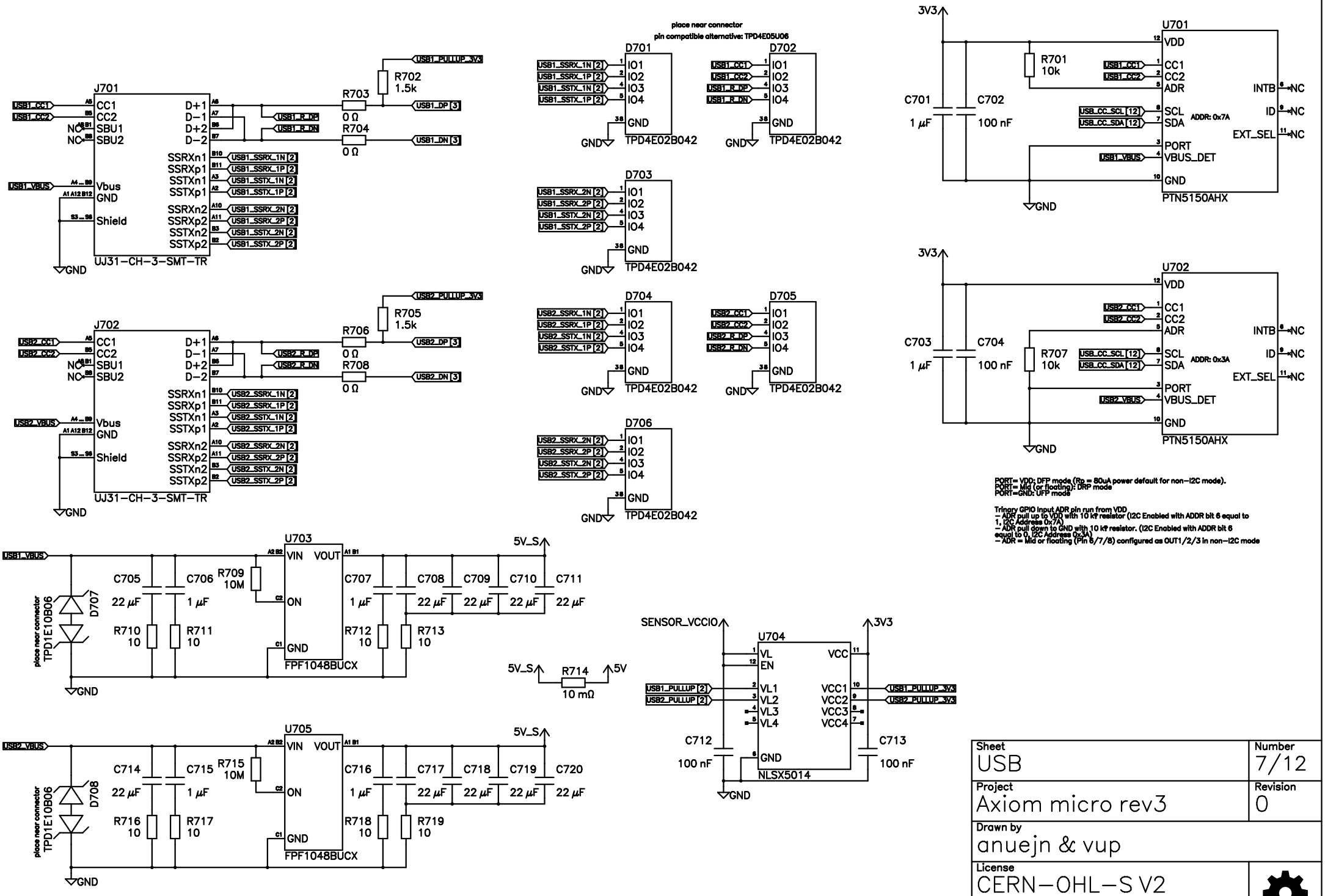
Sheet: ecp power	Number: 4/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	open source hardware
Date: 20200324	



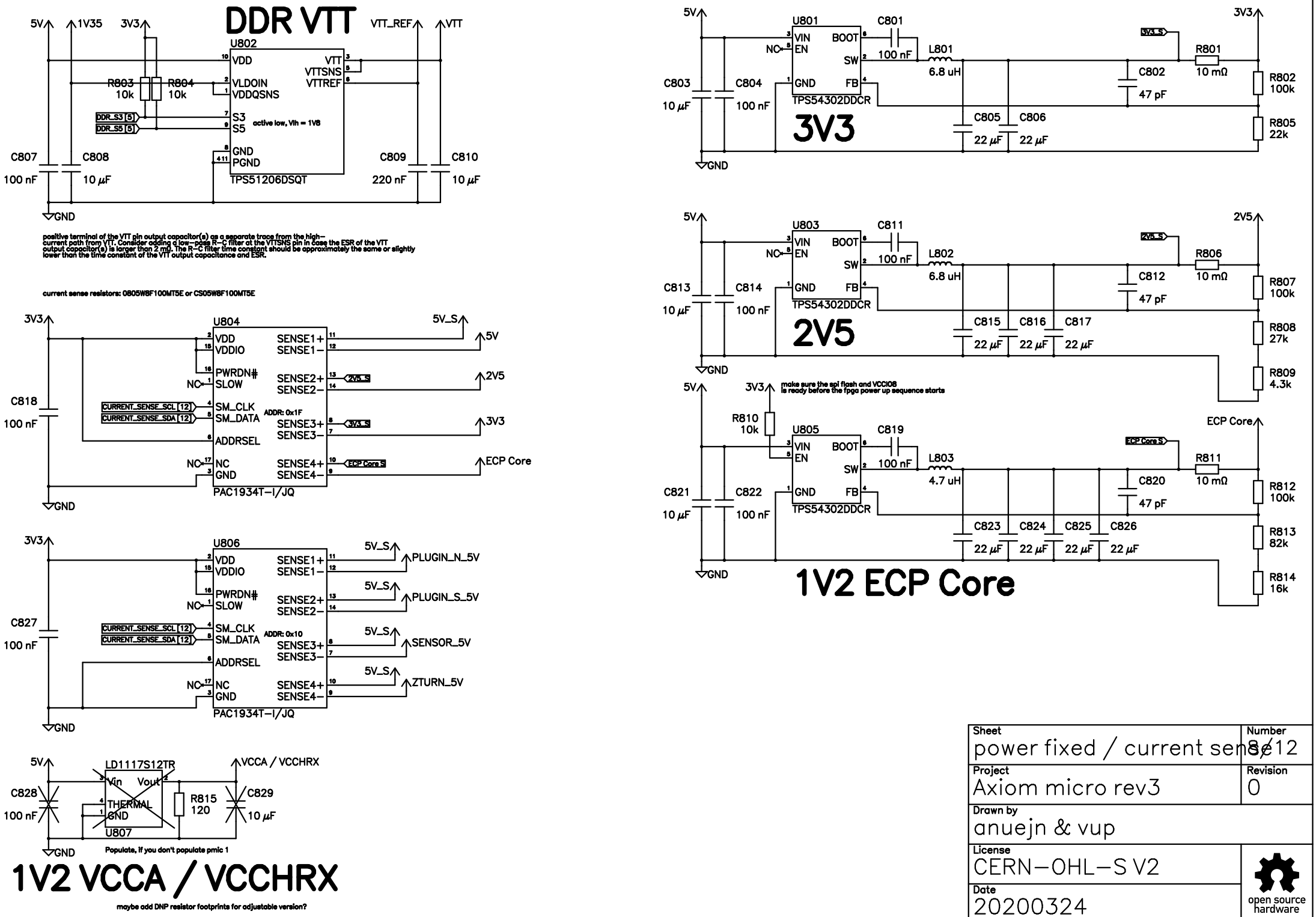
Sheet: RAM	Number: 5/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	open source hardware
Date: 20200324	



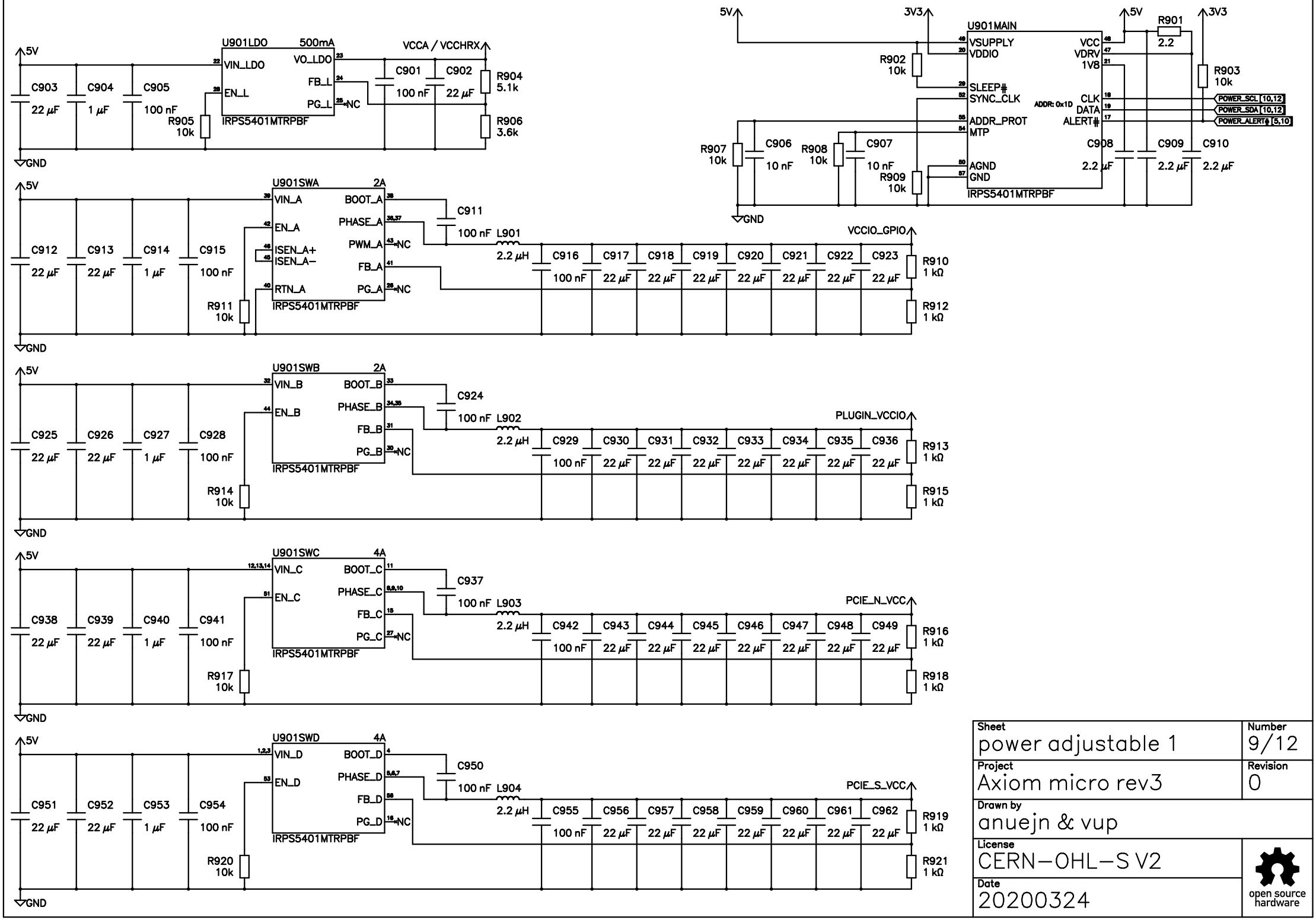
Sheet: plugins / shield	Number: 6/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	open source hardware
Date: 20200324	



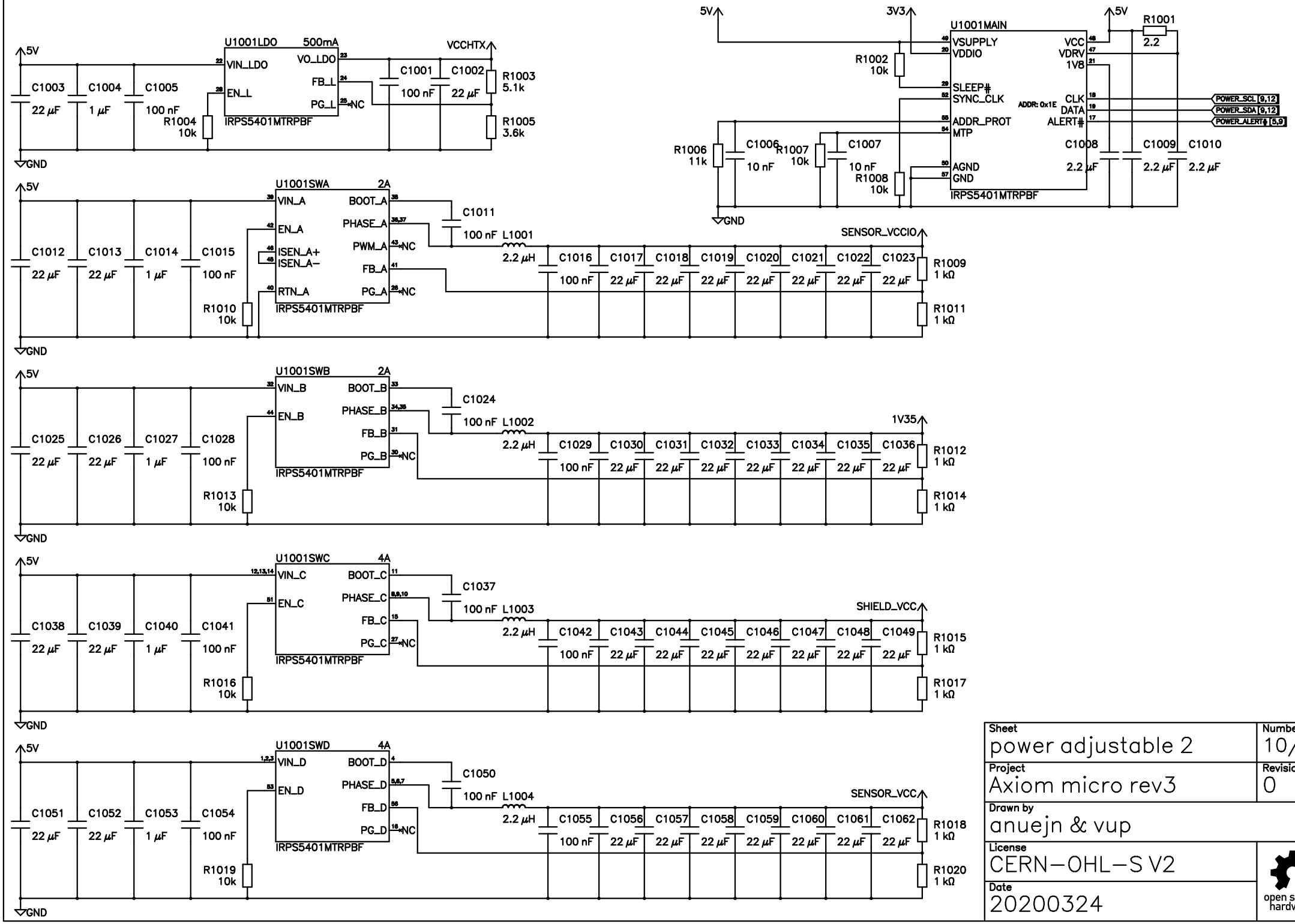
Sheet: USB	Number: 7/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN−OHL−S V2	
Date: 20200324	open source hardware



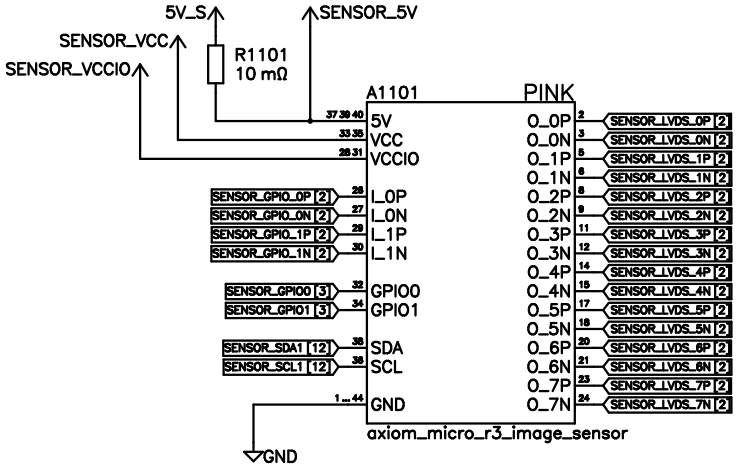
Sheet: power fixed / current sense	Number: 8/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN–OHL–S V2	open source hardware
Date: 20200324	

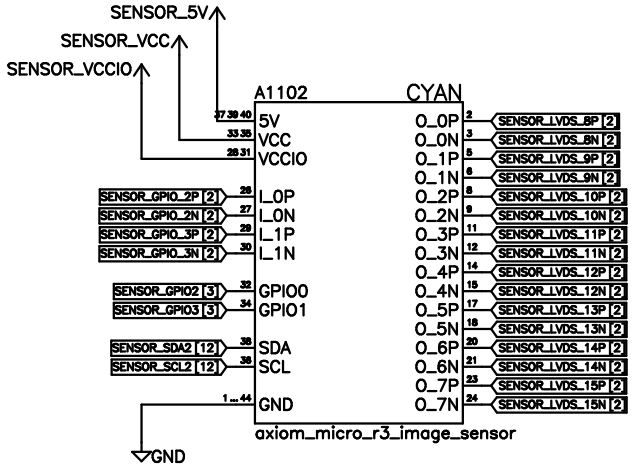


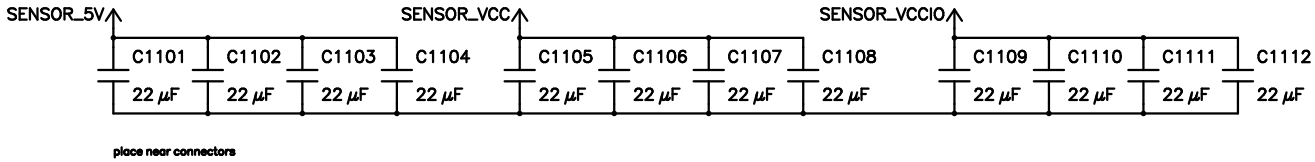
Sheet: power adjustable 1	Number: 9/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN−OHL−S V2	open source hardware
Date: 20200324	



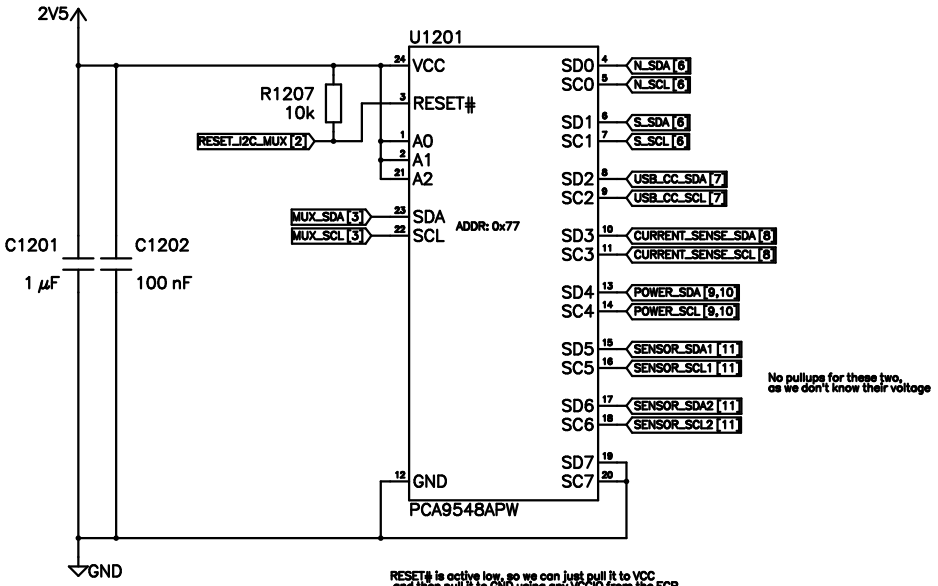
Sheet: power adjustable 2	Number: 10/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN−OHL−S V2	open source hardware
Date: 20200324	







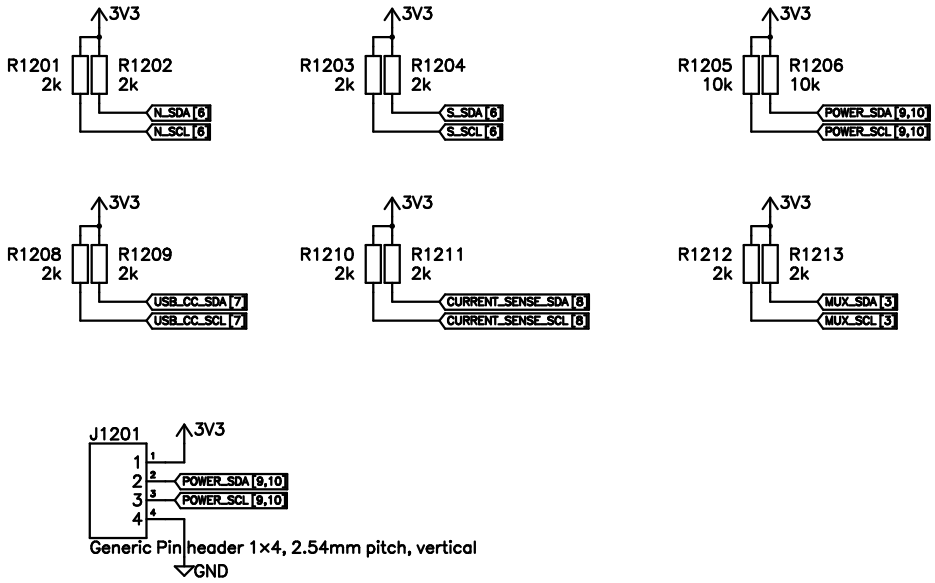
Sheet: image sensor	Number: 11/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN–OHL–S V2	open source hardware
Date: 20200324	



RESET# is active low, so we can just pull it to VCC
and then pull it to GND using any VCCIO from the ECP.
attention has to be paid to not make RESET# get over VCC,
as otherwise current flows from the RESET pin to the VCC pin.
this should be accomplishable by just making the fpga output HI-Z
if it is not pullen low

2V5 VCC means about 1V8 voltage clamping by the pass through translators
That sholud work for most applications, we just need to be careful with nothing with 1V2 is on the bus

Unused channels have to be tied to GND or VCC



Sheet: i2c mux	Number: 12/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	open source hardware
Date: 20200324	