
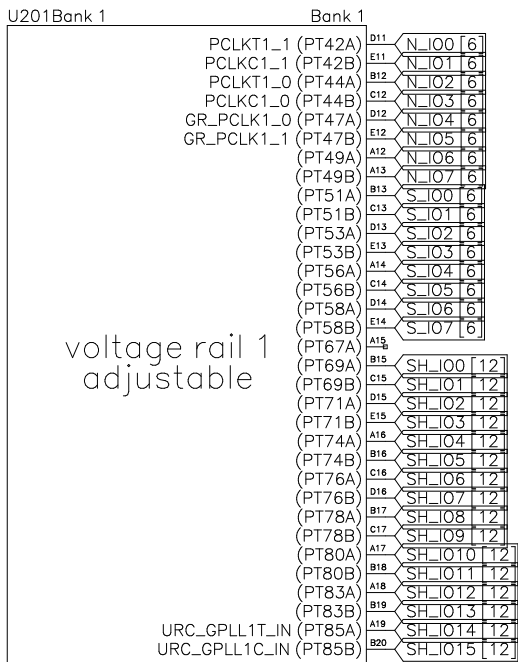
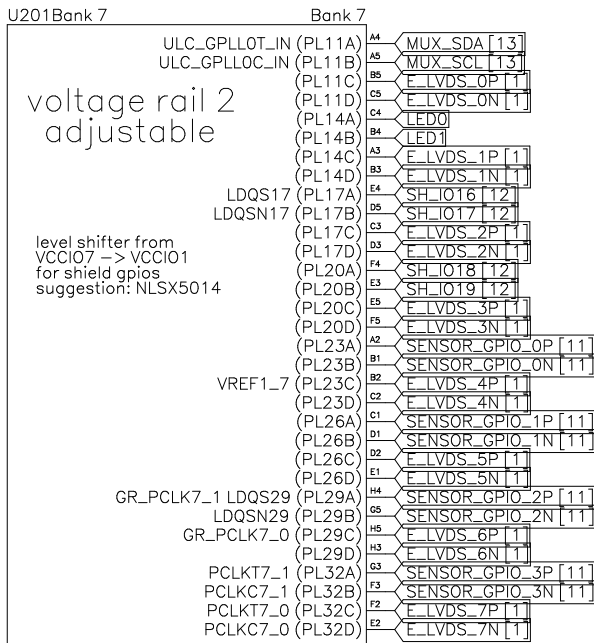
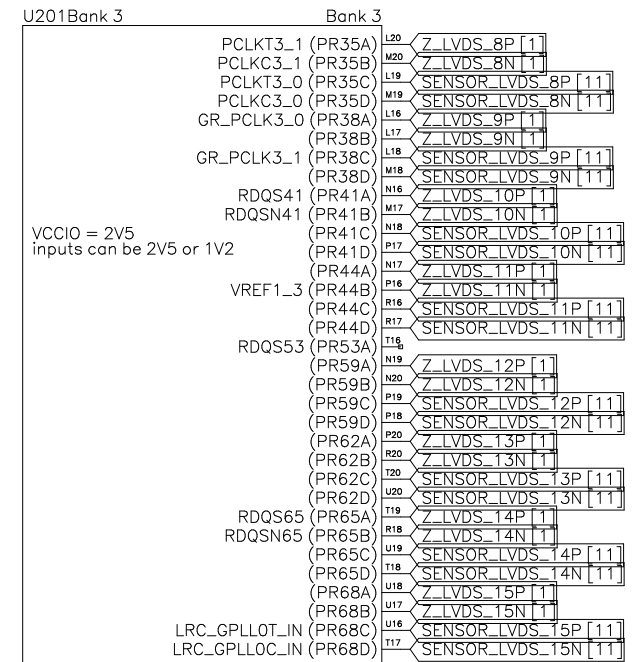
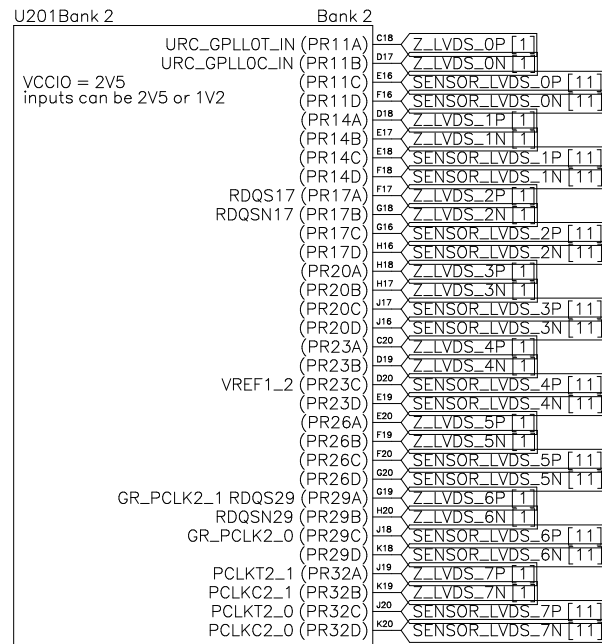


Sheet	zturn lite	Number	1/13
Project	Axiom micro rev3	Revision	0
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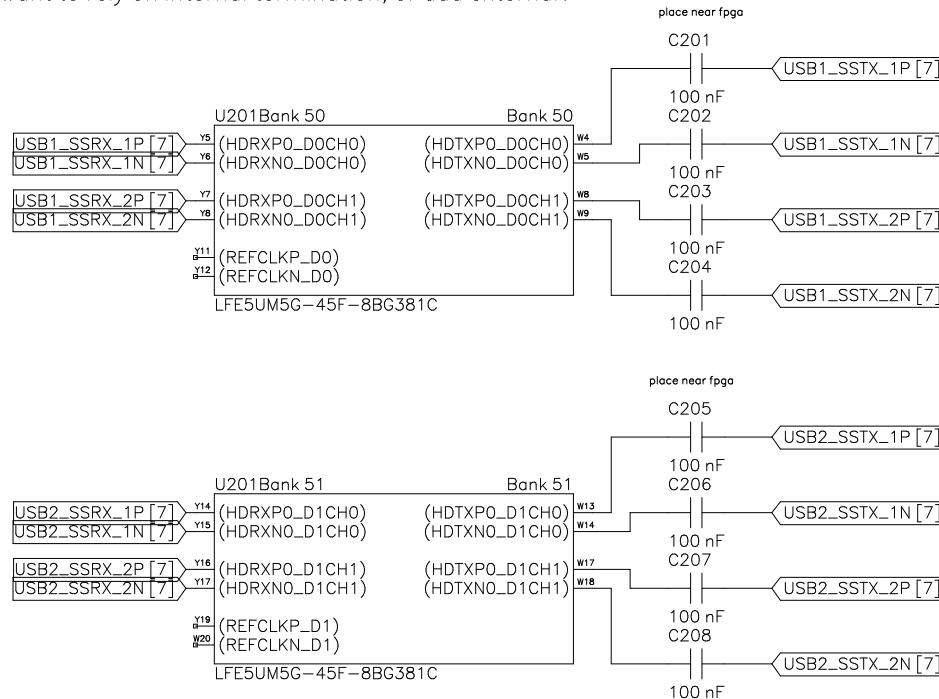


LFE5UM5G-45F-8BG381C

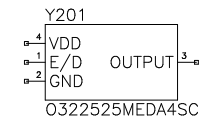


LFE5UM5G-45F-8BG381C

Do we want to rely on internal termination, or add external?



Z\_LVDS goes from ECP to ZYNQ  
E\_LVDS goes from ZYNQ to ECP  
SENSOR\_LVDS goes from sensor board to ECP



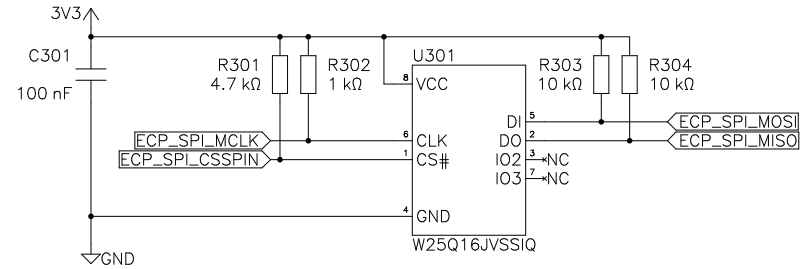
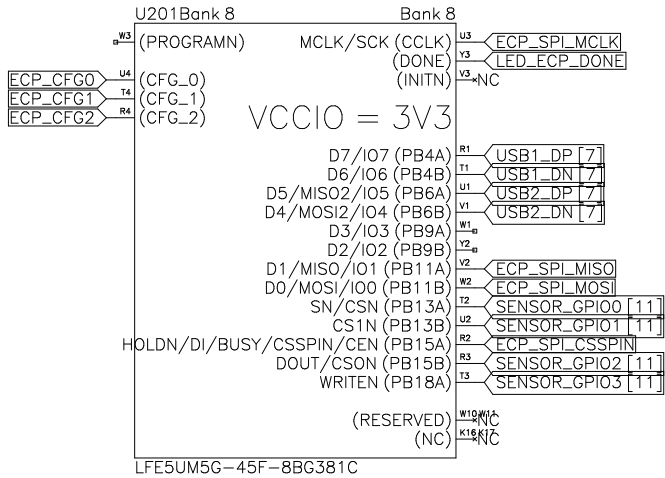
Sheet	Number
ecp	2/13
Project	Revision
Axiom micro rev3	0
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20200324	



# PROGRAMN

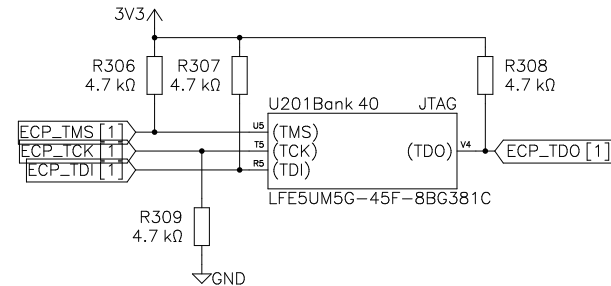
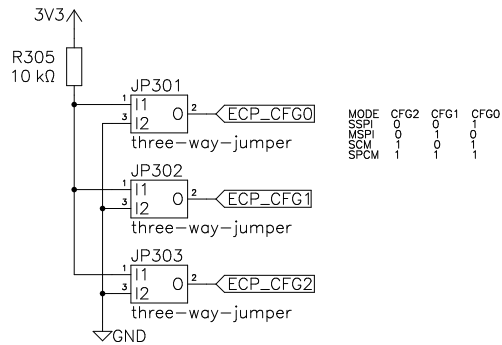
Maybe button for reset,  
or somehow connect to trigger reset?

Also has internal pullup during configuration, but maybe we want an external pullup to prevent floating?



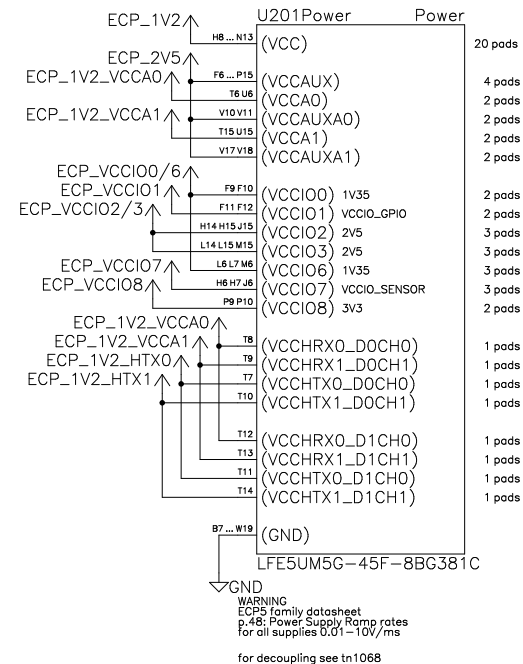
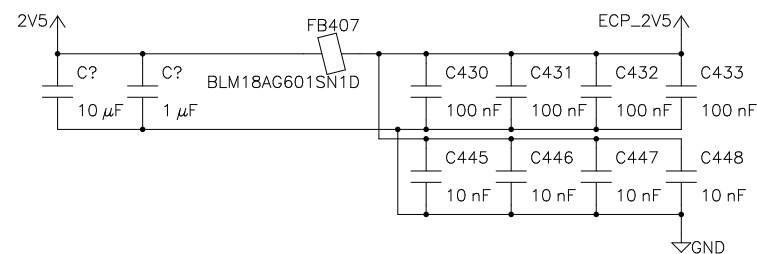
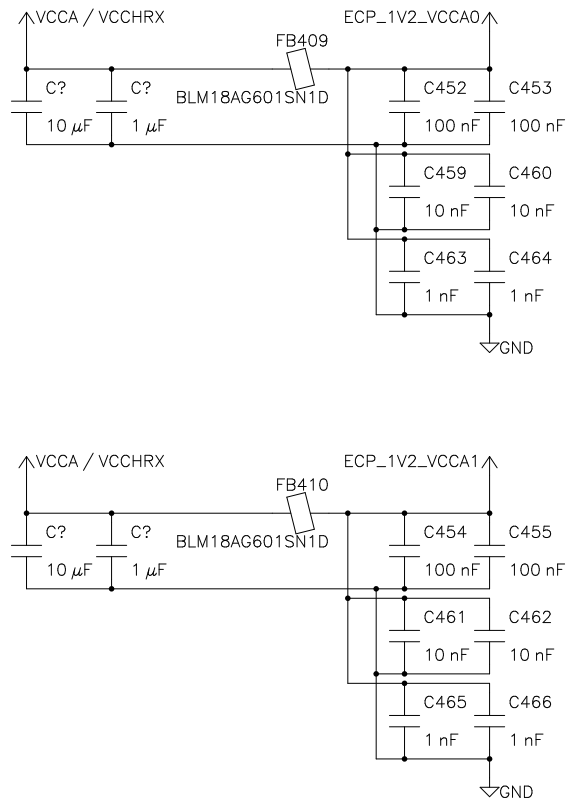
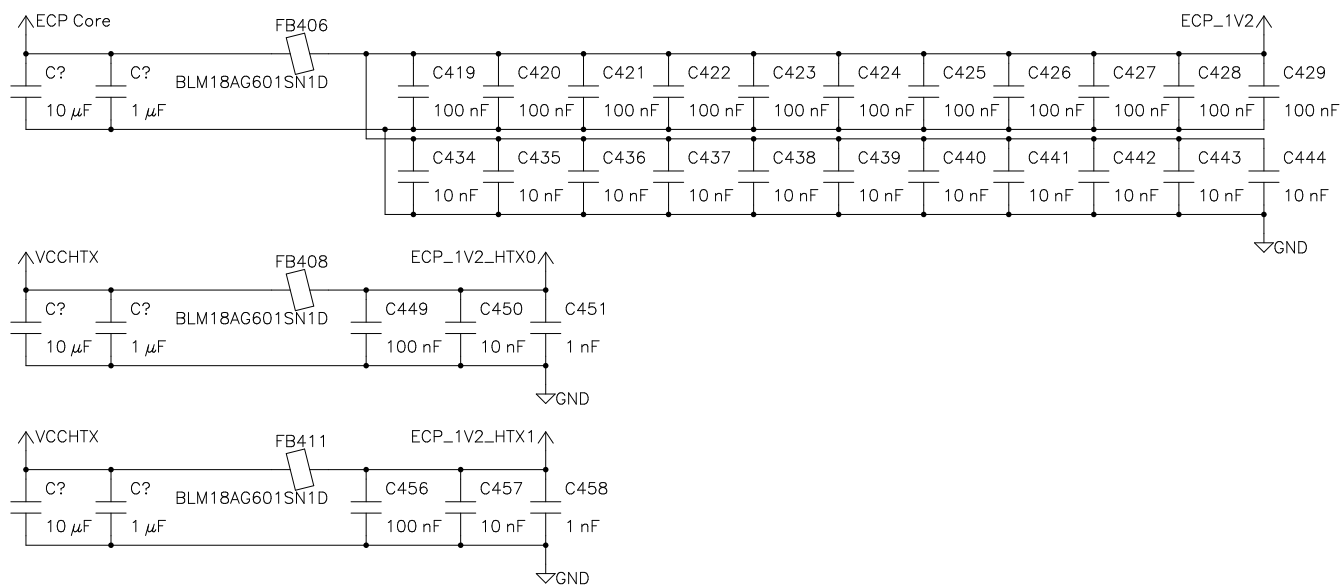
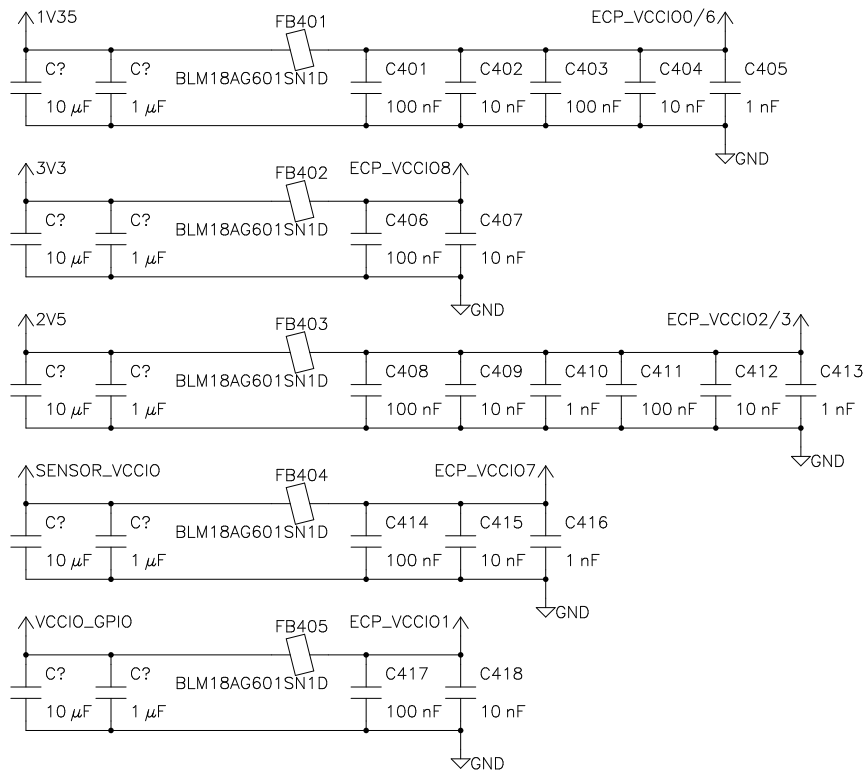
The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI operation. When the QE bit is set to a 0 state (factory default for part numbers with ordering options **TIMT**), the /WP pin and /HOLD are enabled. When the QE bit is set to a 1 (factory default for Quad Enabled part numbers with ordering option **TQTY**), the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled.

/CS must track VCC during VCC Ramp Up/Down



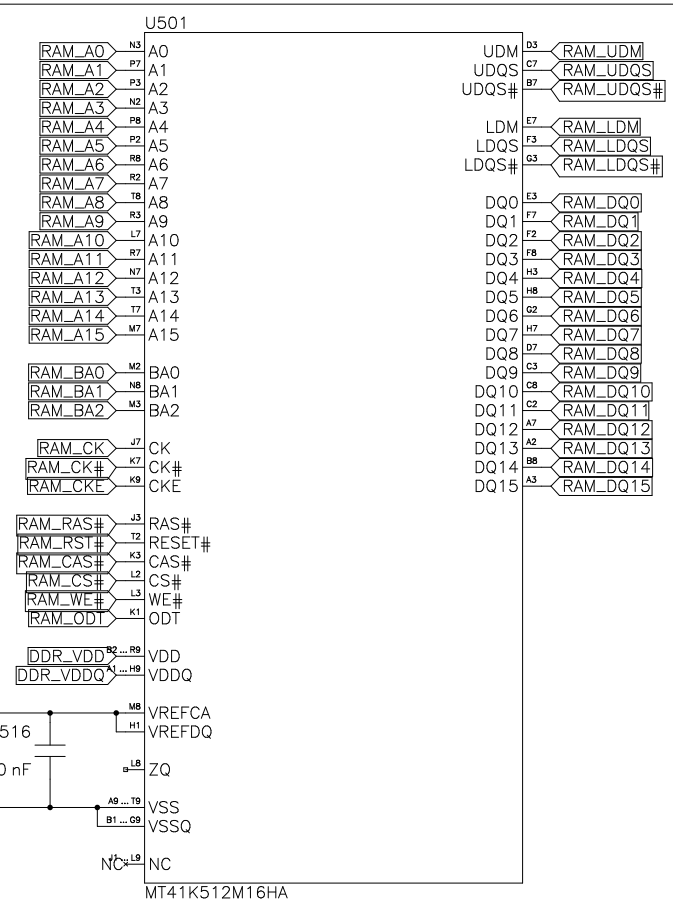
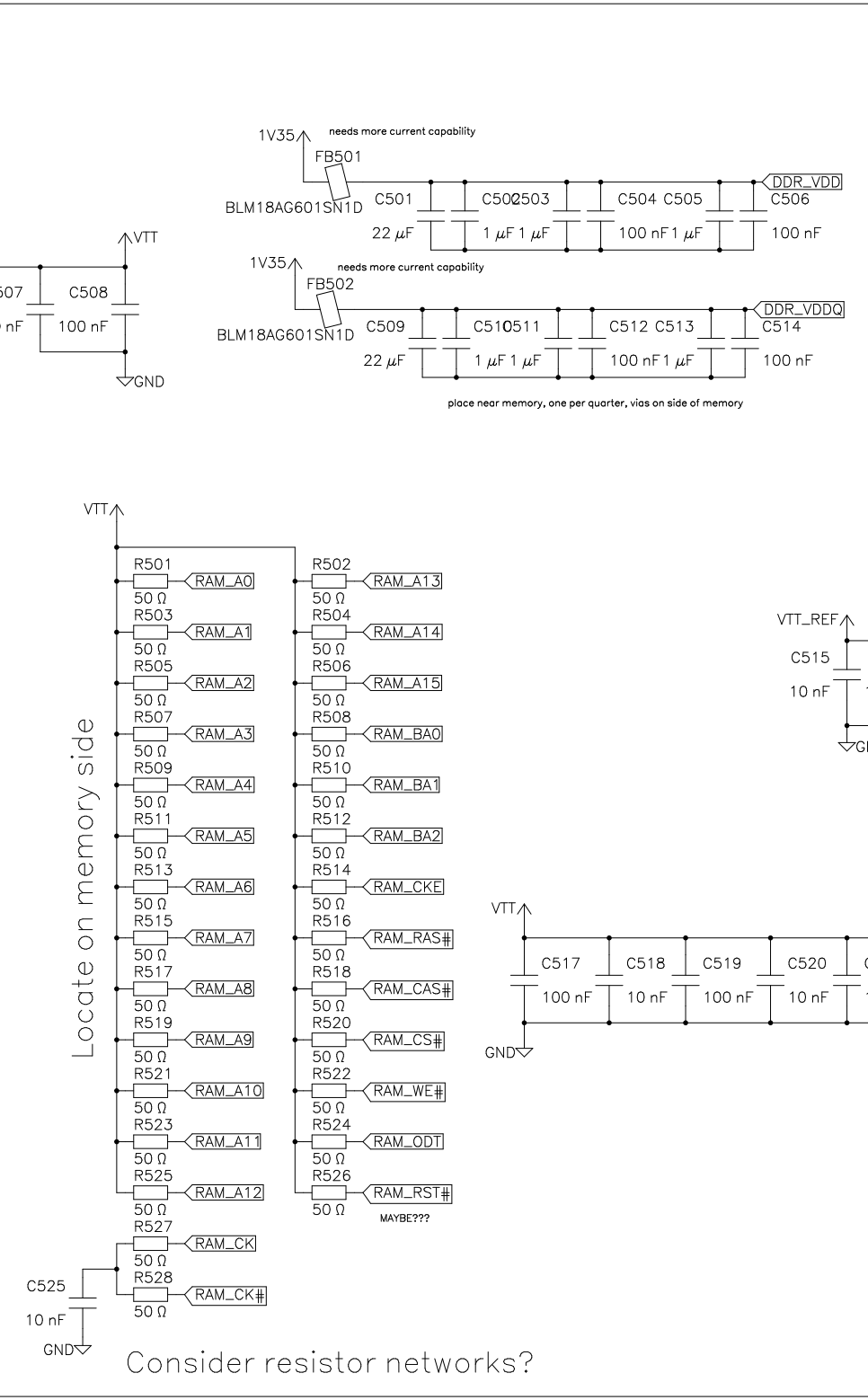
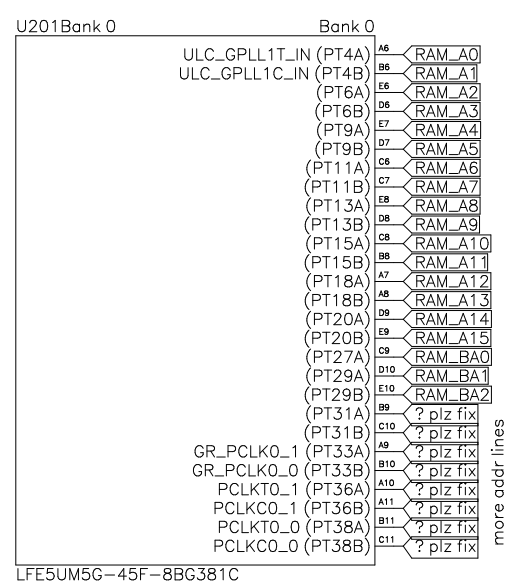
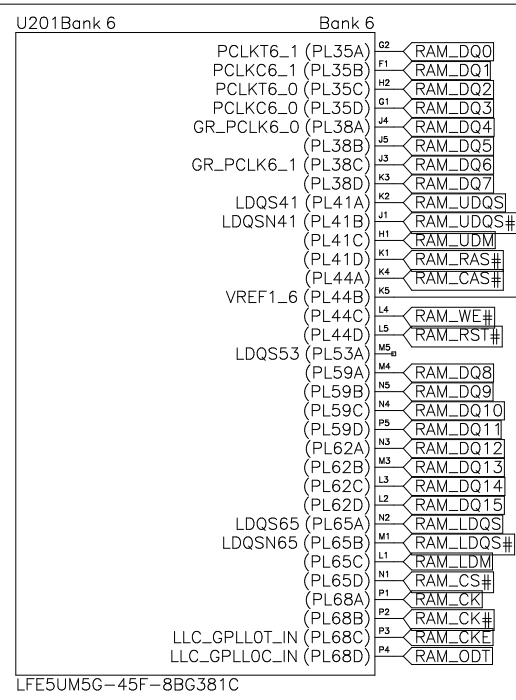
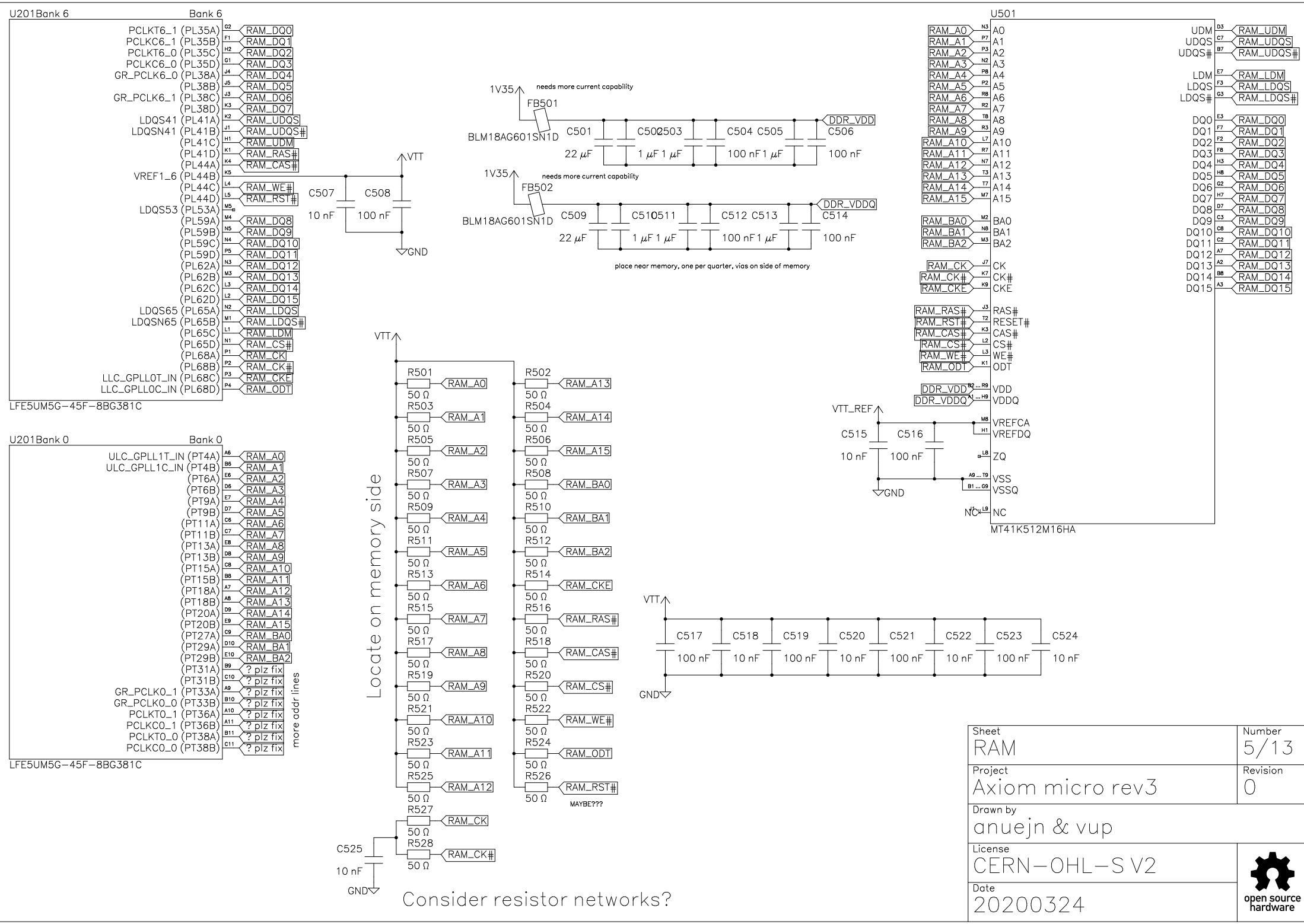
Sheet	Number
ecp config	3/13
Project	Revision
Axiom micro rev3	0
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Place decoupling near FPGA, alternate 100n and 10n per pad per rail




Sheet	Number
ecp power	4/13
Project	Revision
Axiom micro rev3	0
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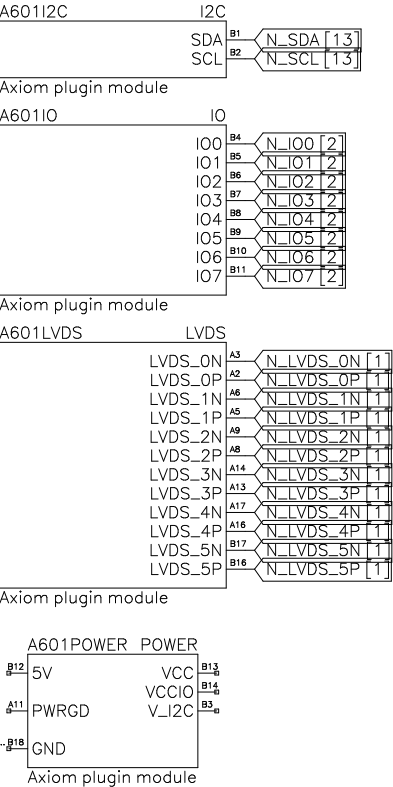


Sheet	RAM	Number	5/13
Project	Axiom micro rev3	Revision	0
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Date	20200324		

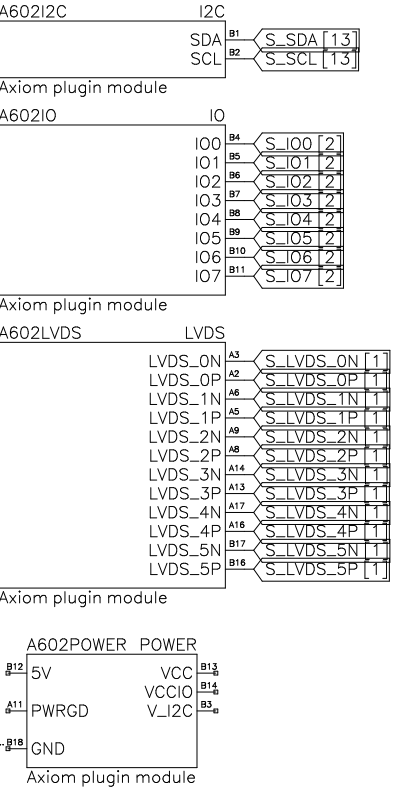


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plugin north



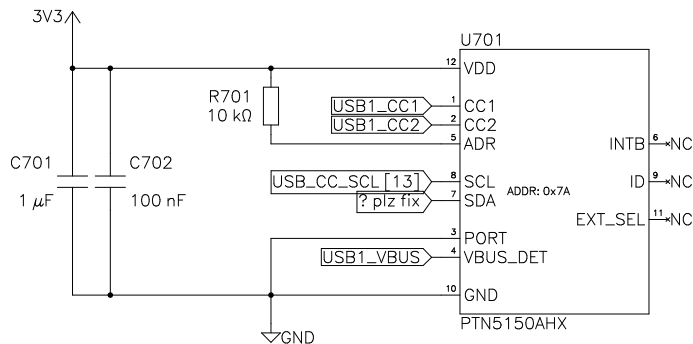
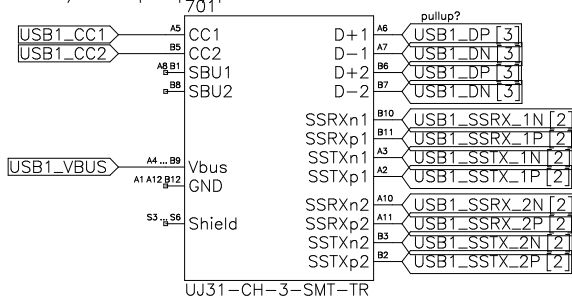
plugin south



Sheet	Number
plugin	6/13
Project	Revision
Axiom micro rev3	0
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Date	
20200324	

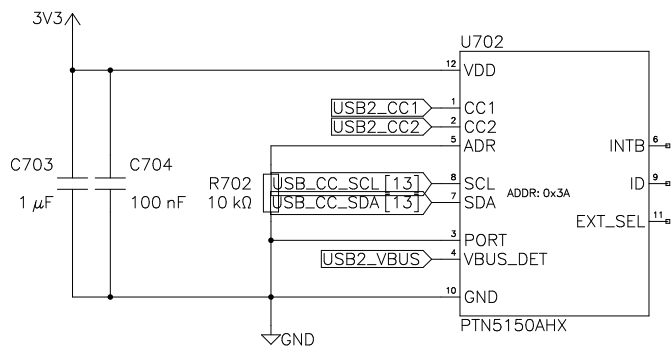
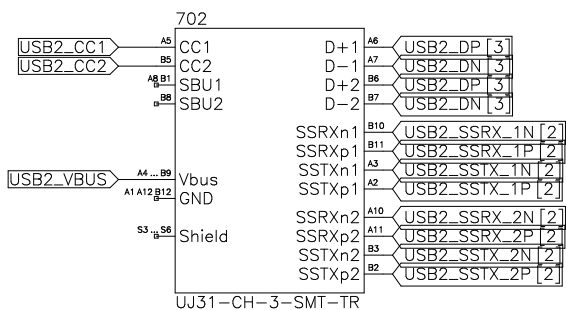
  
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We probably want to be a upwards facing port?  
CC1/2 need pullups / pulldowns

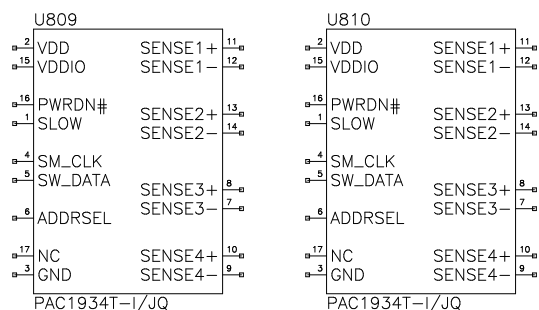


PORT= VDD; DFP mode ( $R_p = 80\mu A$  power default for non-I2C mode).  
PORT= Mid (or floating); DRP mode  
PORT=GND; UFP mode

Trinary GPIO Input ADDR pin run from VDD.  
- ADDR pull up to VDD with 10 kΩ resistor (I2C Enabled with ADDR bit 6 equal to 1, I2C Address 0x7A)  
- ADDR pull down to GND with 10 kΩ resistor. (I2C Enabled with ADDR bit 6 equal to 0, I2C Address 0x3A)  
- ADDR = Mid or floating (Pin 6/7/8) configured as OUT1/2/3 in non-I2C mode



Sheet USB	Number 7/13
Project Axiom micro rev3	Revision 0
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positive terminal of the VTT pin output capacitor(s) as a separate trace from the high-current path from VTT. Consider adding a low-pass R-C filter at the VTTSENS pin in case the ESR of the VTT output capacitor(s) is larger than 2 m $\Omega$ . The R-C filter time constant should be approximately the same or slightly lower than the time constant of the VTT output capacitance and ESR.



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PCIEN\_VCC

5V

EN\_PCIE\_N\_VCC

what to put here?

TPS65400RGZT

U901SW1 SW1 4A

PVIN1

CB1

1 234 100 nF

SW1

VFB1

47

COMP1

46

R902 30.1 kΩ

C904 22 pF

C905 22 μF

C906 100 nF

C907 100 nF

C908 22 μF

C909 22 μF

C902 1 nF

R901 100 kΩ

R903 100 kΩ

C910 100 μF

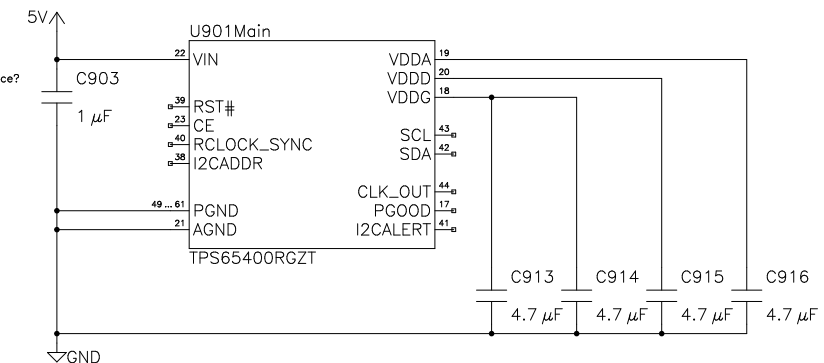
C911 100 μF

PCIEN\_VCC


The reference design has some more random resistors here

maybe m

GND



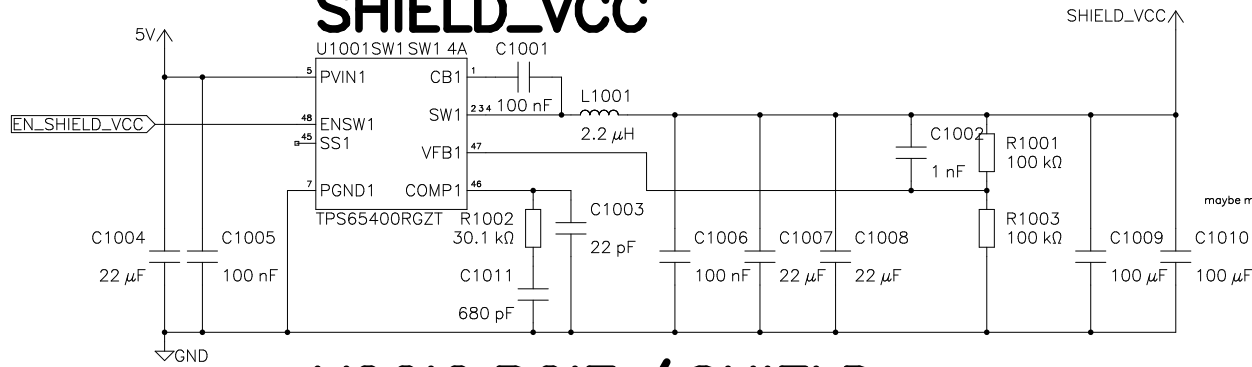
- more bulk capacitance?  
(for 1V2 the reference schematic has 470uF additionally)
- soft start capacitors
- current limiting resistor for feed forward capacitor
- think about the compensation network
- If the input supply is located more than a few inches from the TPS65400 converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47  $\mu$ F is a typical choice.

Sheet	power adjustable 1	Number	9/13
Project	Axiom micro rev3	Revision	0
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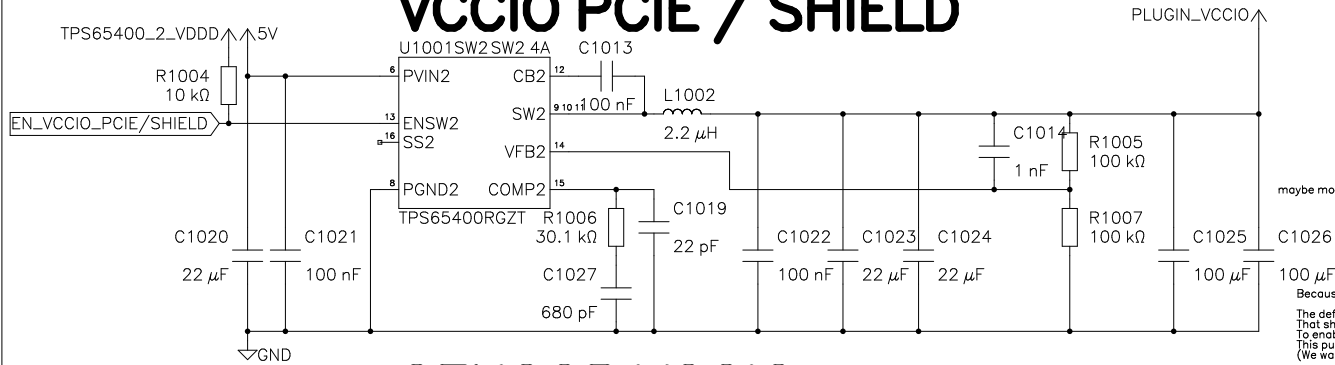


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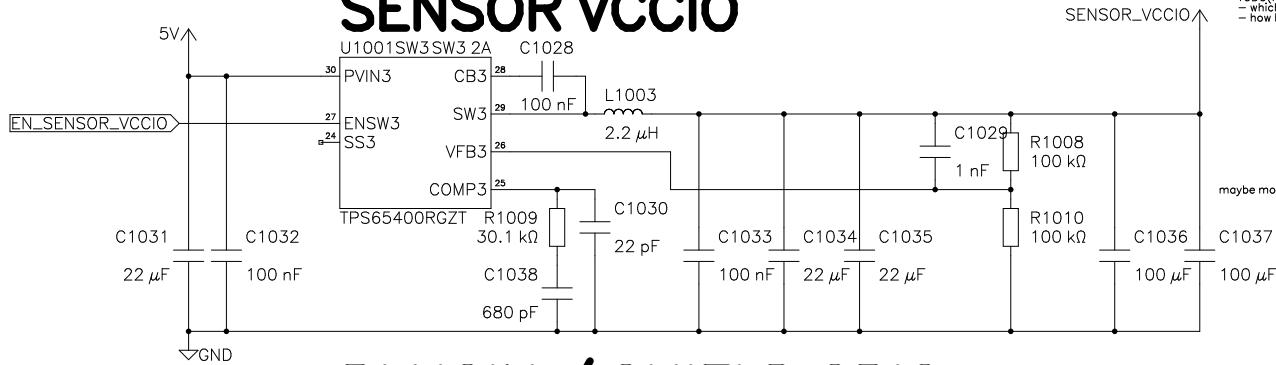
# SHIELD\_VCC



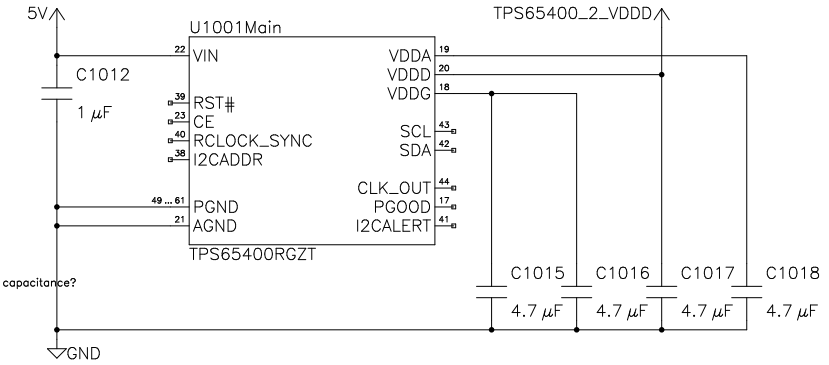
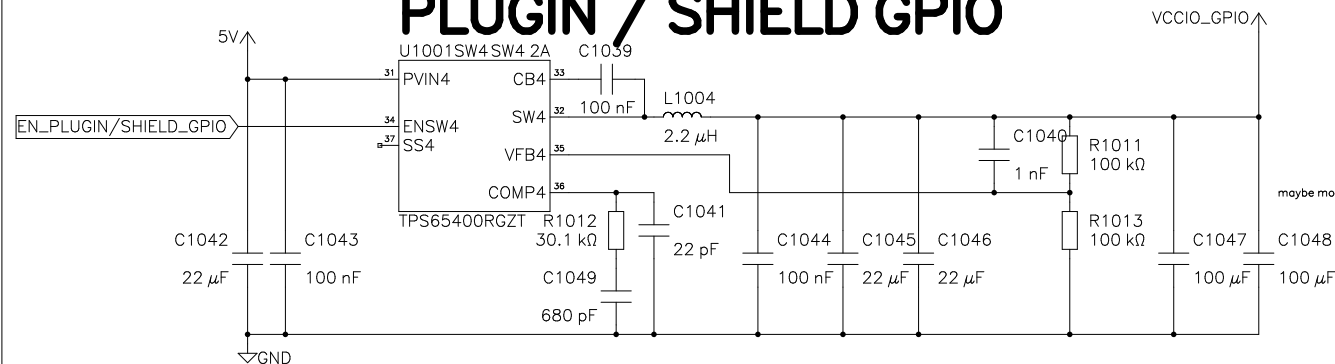
# VCCIO PCIE / SHIELD



# SENSOR VCCIO



# PLUGIN / SHIELD GPIO



Because JTAG is driven from PLUGIN\_VCCIO we somehow need to enable that one before ever being able to access the I2C bus.

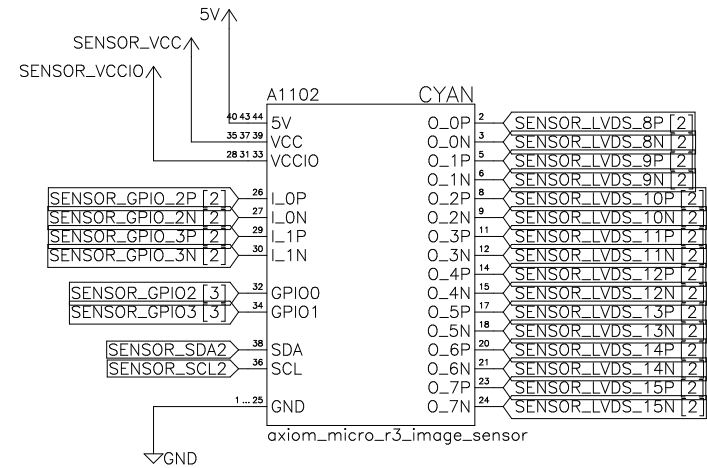
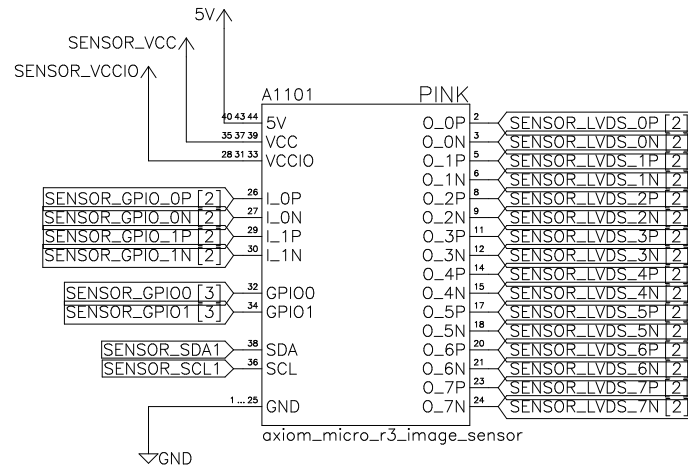
The default for the internal Vref is 0.8V, so we get a output voltage of  $0.8V \cdot (1 + 100k / 100k) = 1.6V$   
 That should work for jtag (its shifted to 3v3 with a level shifter)  
 To enable the rail, we also add a pullup to EN\_VCCIO\_PCIE/SHIELD  
 This pullup can later be overridden by using some I2C commands.  
 (We want to be able to do that to not damage the plugin modules, that get a direct link to this rail)

TODD(robin):  
 - which rail do we want to pull to? VDDD or maybe 3V3?  
 - how big should the pullup be?


Sheet	power adjustable 2	Number	10/13
Project	Axiom micro rev3	Revision	0
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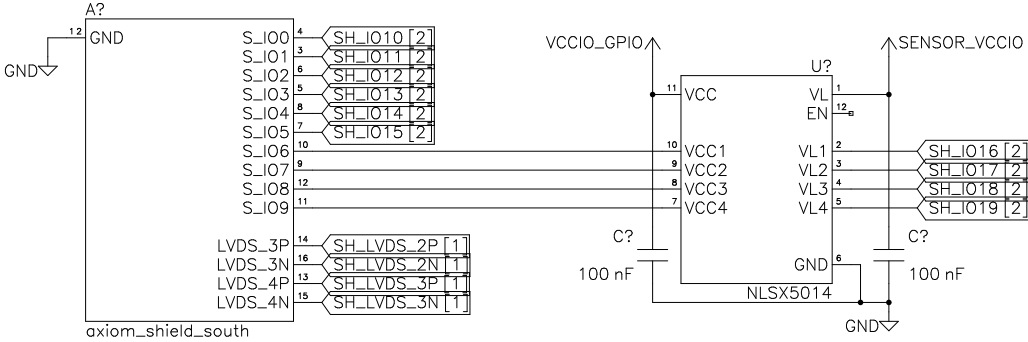
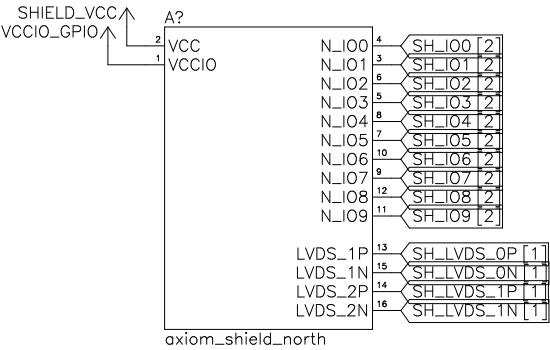



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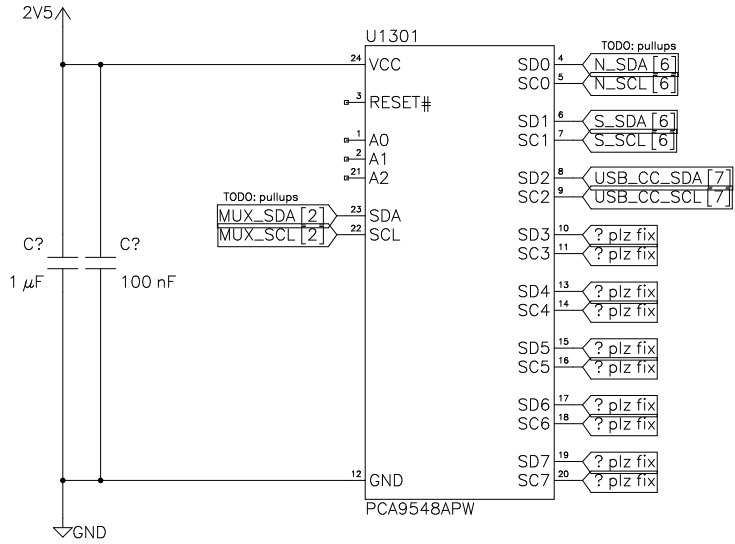
Bulk capacitance for sensor? (0(100uF))

Sheet	image_sensor	Number	11/13
Project	Axiom micro rev3	Revision	0
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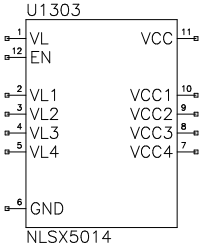



Sheet	shield	Number	12/13
Project	Axiom micro rev3	Revision	0
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2V5 VCC means about 1V8 voltage clamping by the pass through transistors  
That shold work for most applications, we just need to be careful with nothing with 1V2 is on the bus



Stuff we want to hang of the i2c mux:  
plugin modules  
pmic  
probably gpio expander for power stuff  
????



Sheet	misc	Number	13/13
Project	Axiom micro rev3	Revision	0
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