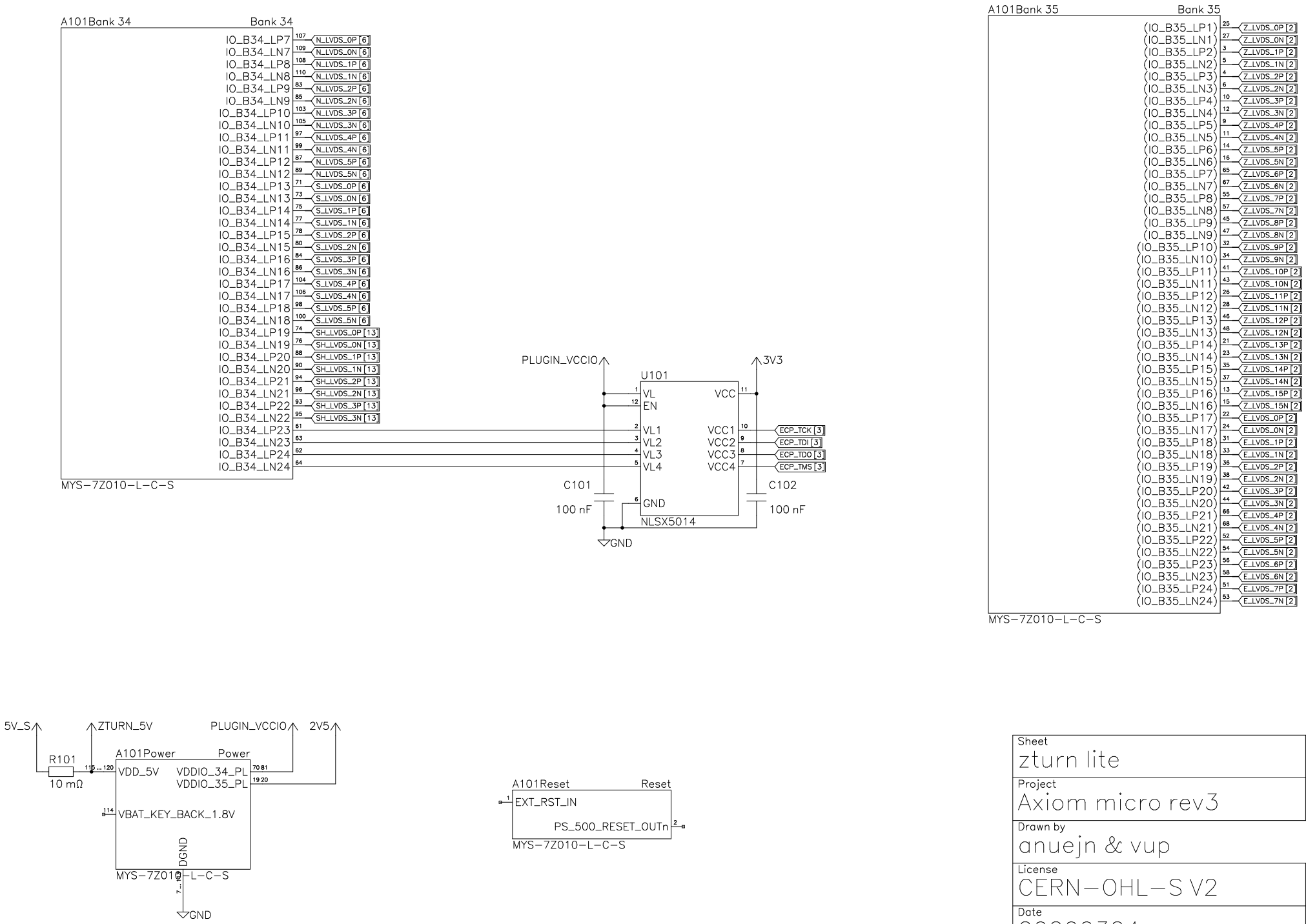
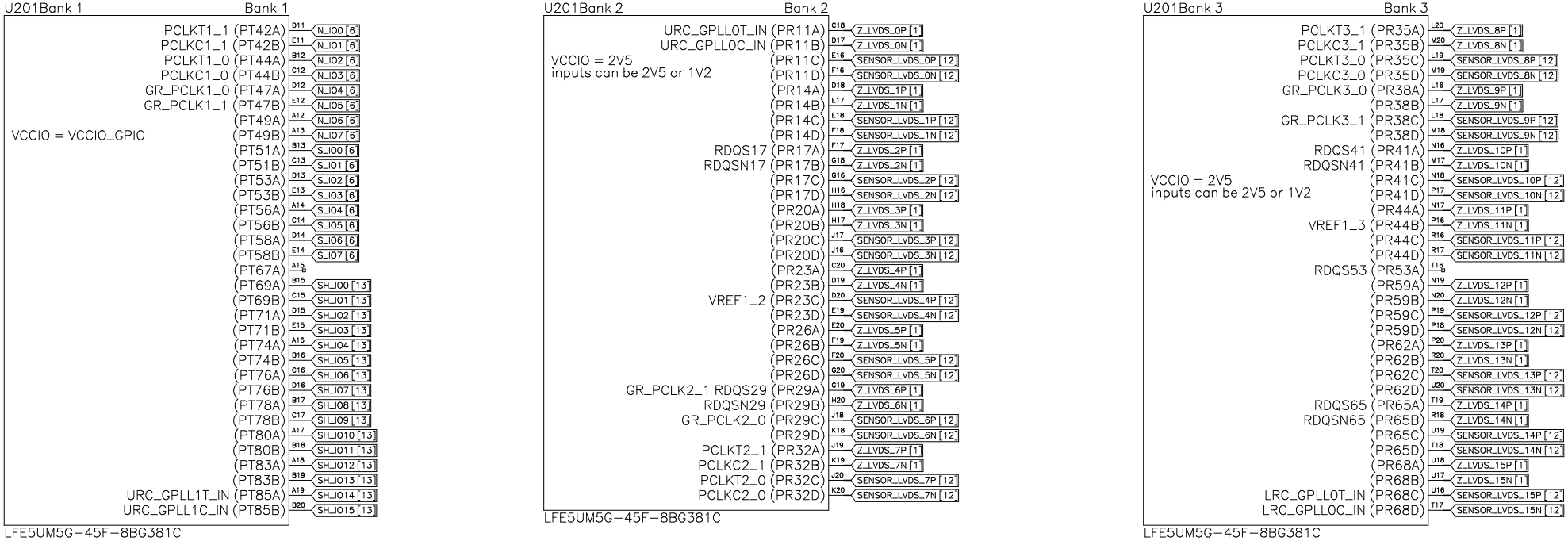
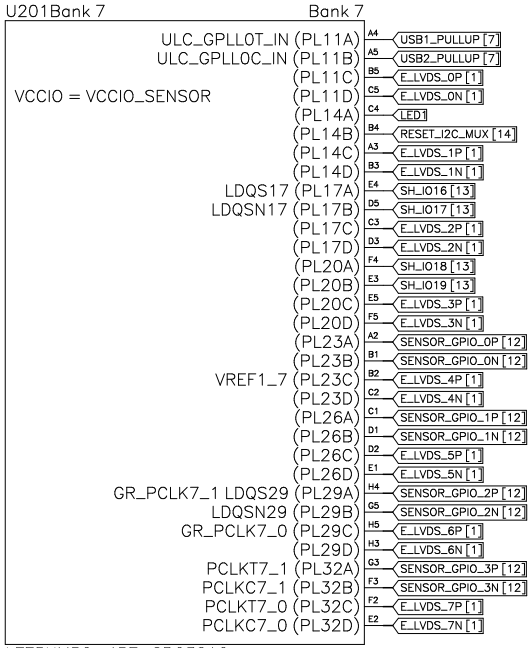
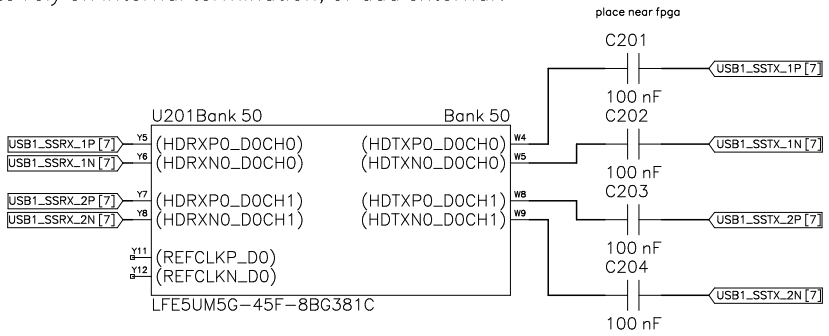


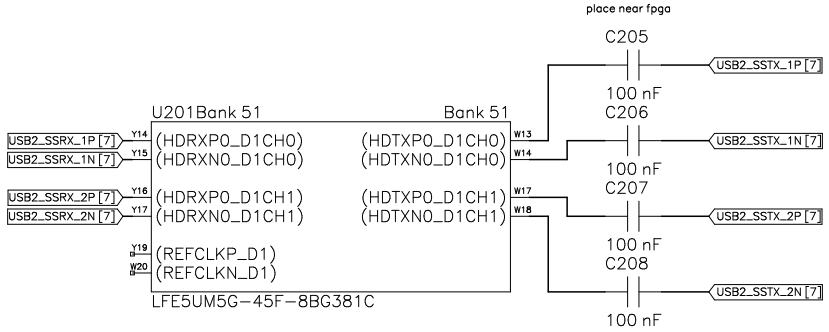
Sheet: zturn lite	Number: 1/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	open source hardware
Date: 20200324	



Do we want to rely on internal termination, or add external?

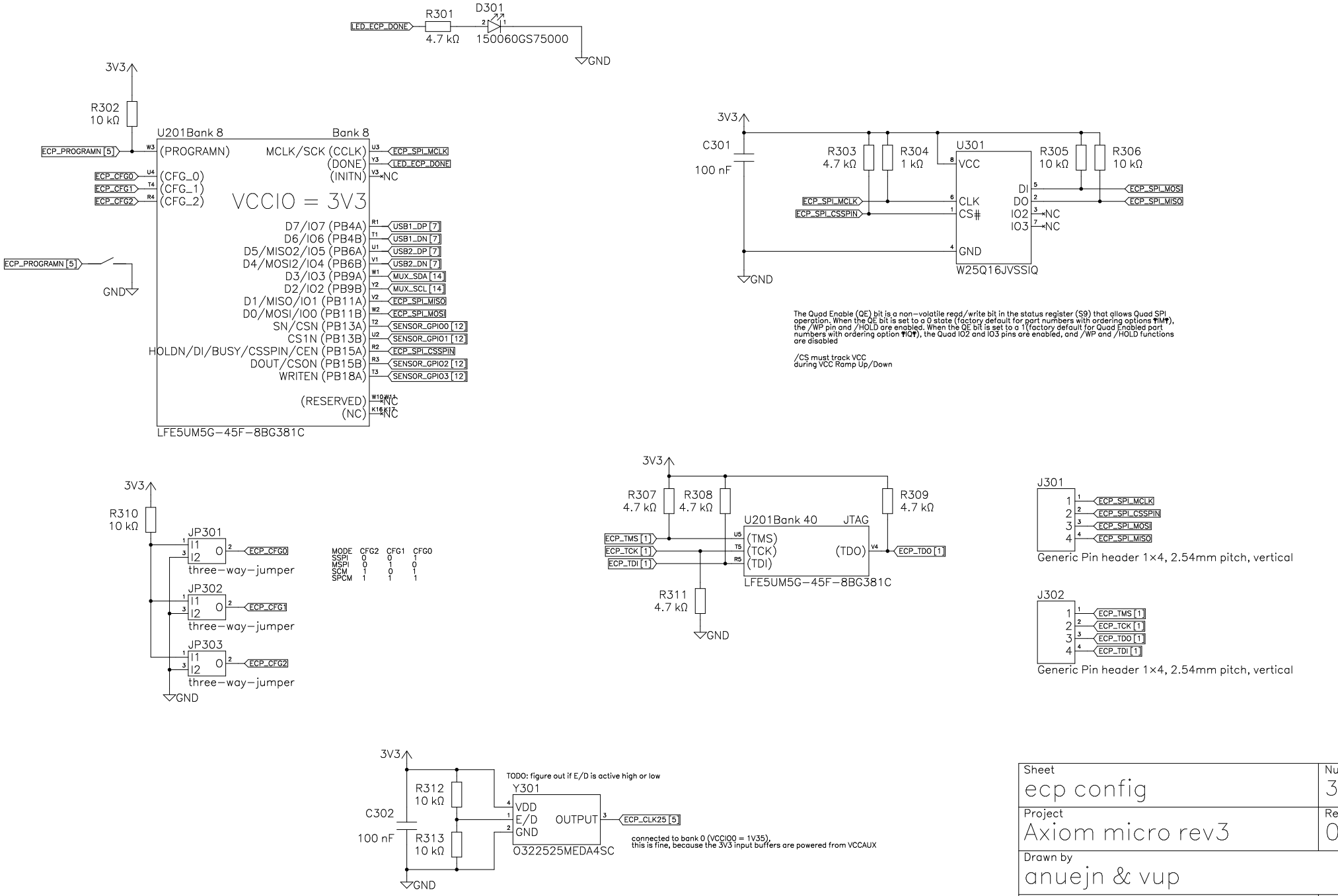






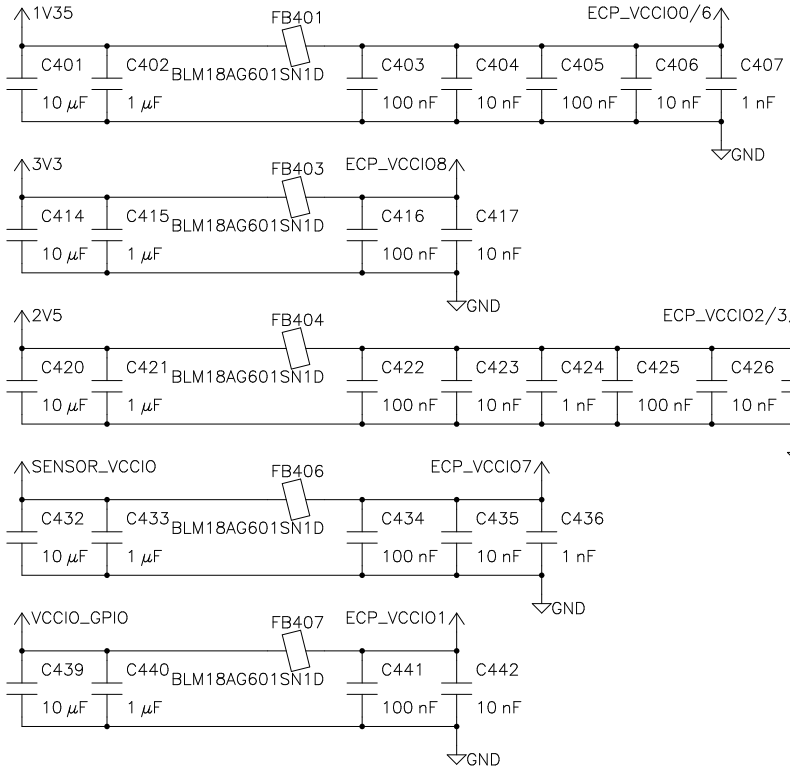
Z_LVDS goes from ECP to ZYNQ
E_LVDS goes from ZYNQ to ECP
SENSOR_LVDS goes from sensor board to ECP

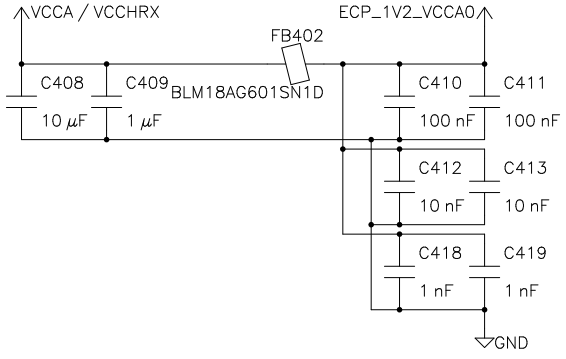
Sheet: ecp	Number: 2/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	open source hardware
Date: 20200324	

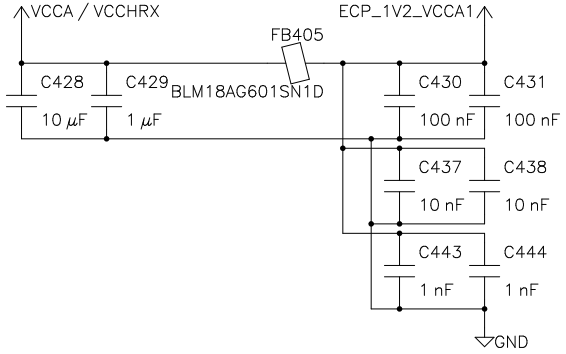


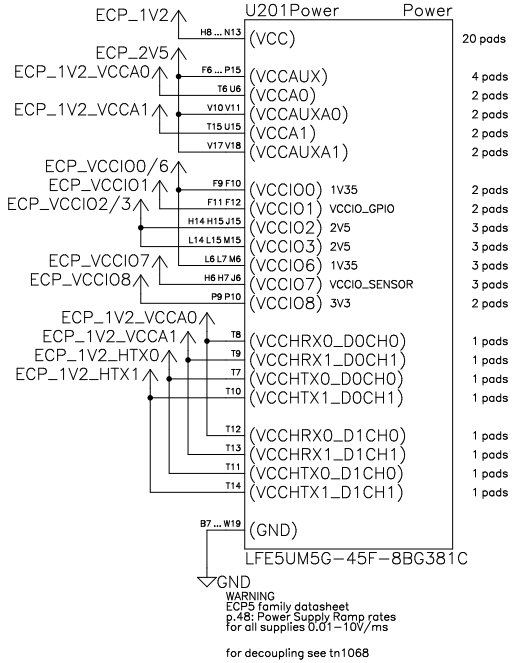
Sheet: ecp config	Number: 3/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	
Date: 20200324	open source hardware

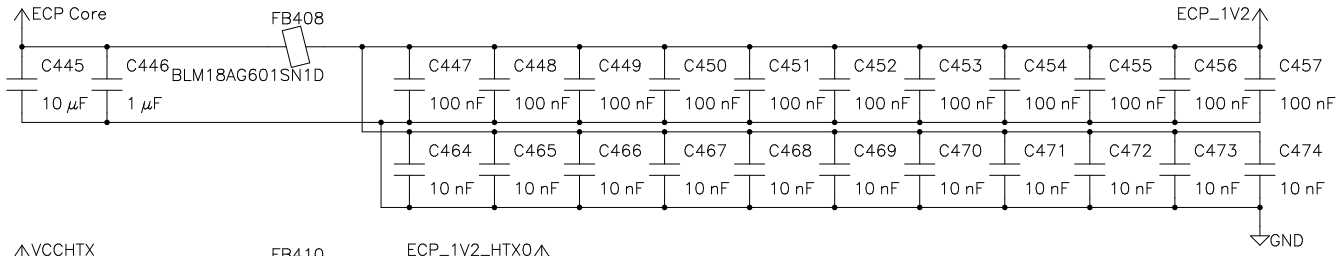
Place decoupling near FPGA, alternate 100n and 10n per pad per rail

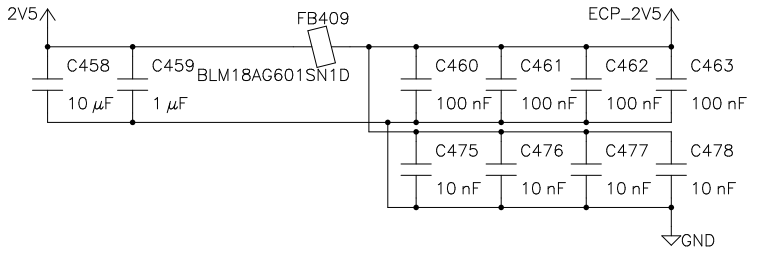


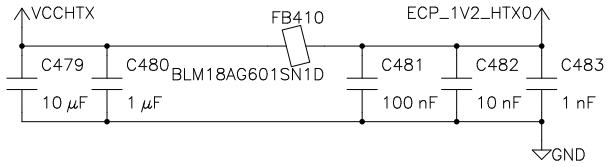


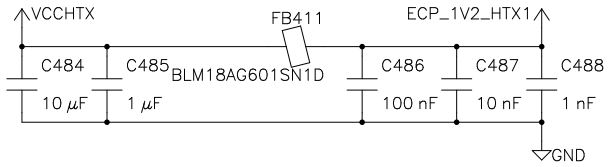




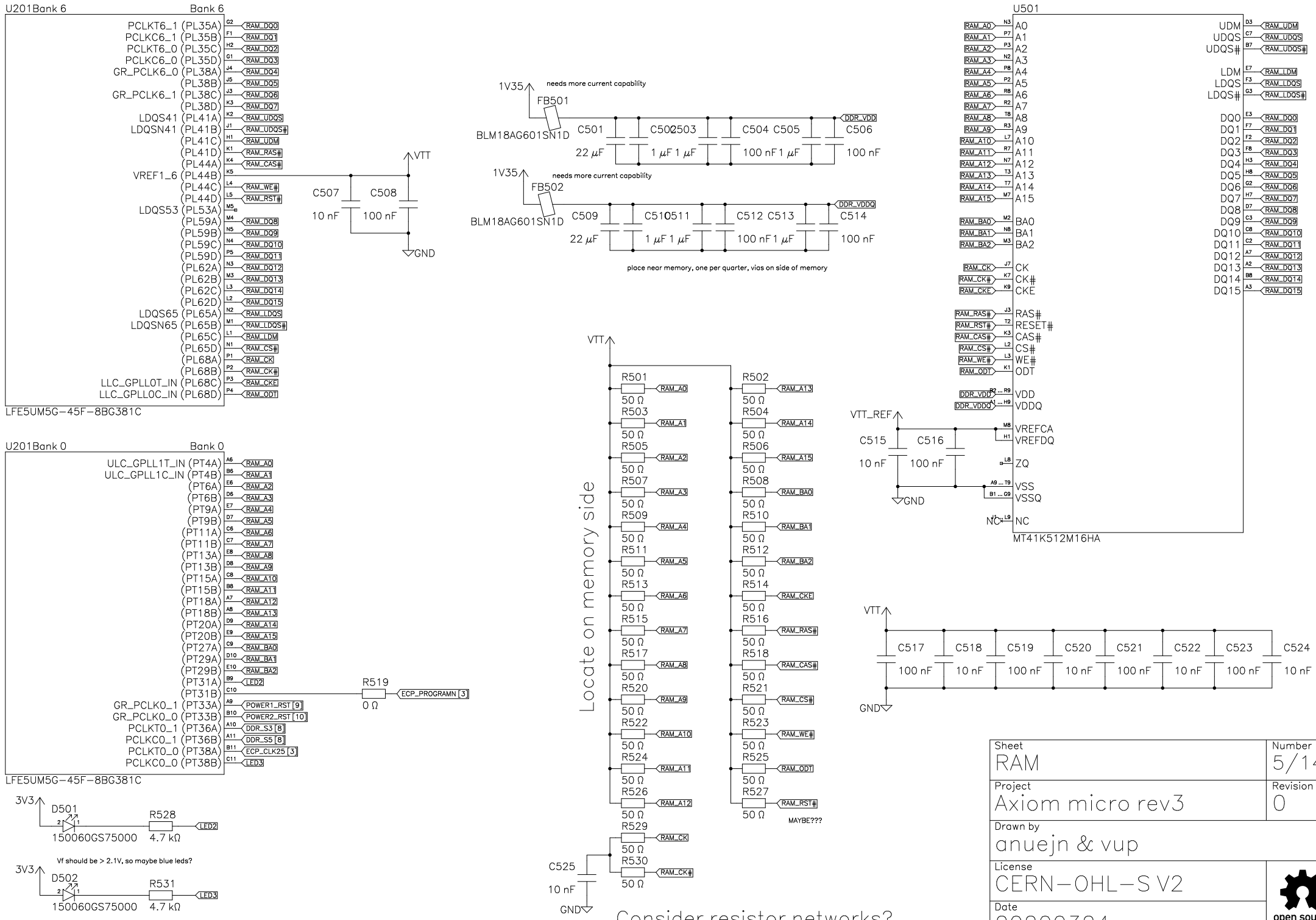




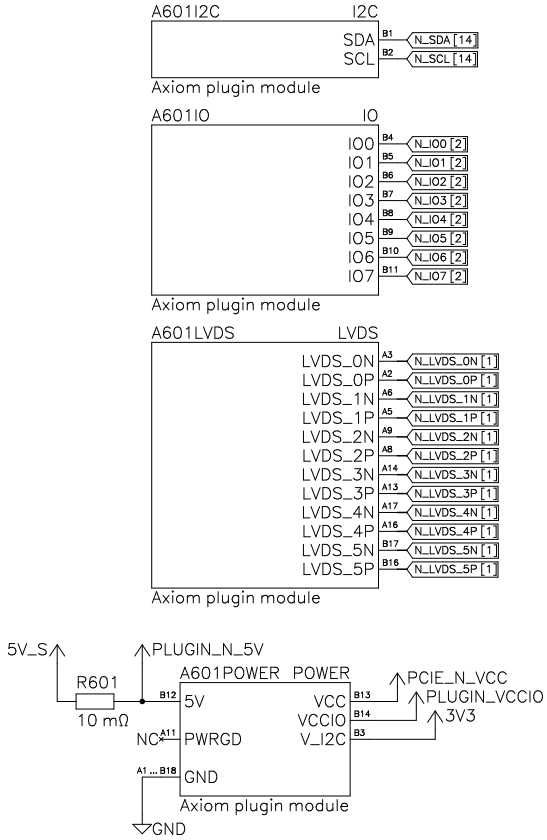




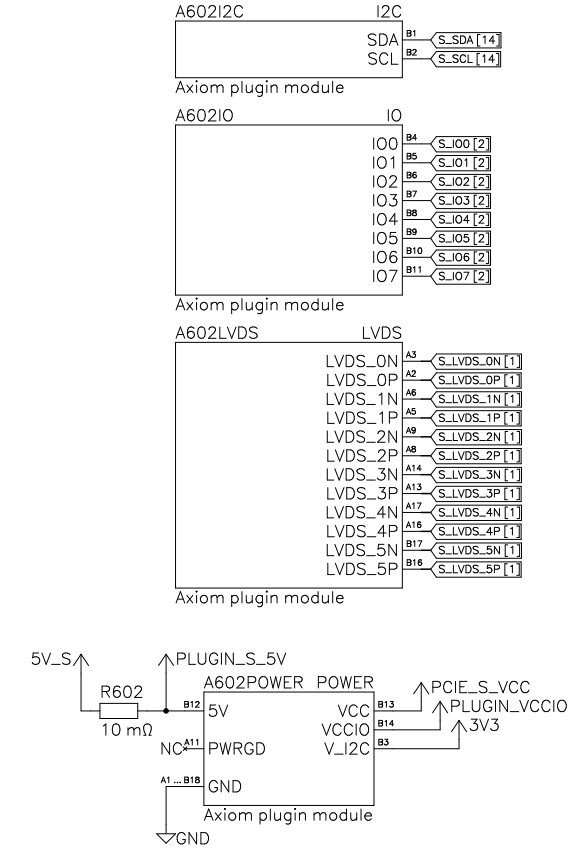
Sheet: ecp power	Number: 4/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	open source hardware
Date: 20200324	


U201Bank 6
Bank 6
PCLKT6_1 (PL35A)
PCLKC6_1 (PL35B)
PCLKT6_0 (PL35C)
PCLKC6_0 (PL35D)
GR_PCLK6_0 (PL38A)
(PL38B)
GR_PCLK6_1 (PL38C)
(PL38D)
LDQS41 (PL41A)
LDQSN41 (PL41B)
(PL41C)
(PL41D)
(PL44A)
VREF1_6 (PL44B)
(PL44C)
(PL44D)
LDQS53 (PL53A)
(PL59A)
(PL59B)
(PL59C)
(PL59D)
(PL62A)
(PL62B)
(PL62C)
(PL62D)
LDQS65 (PL65A)
LDQSN65 (PL65B)
(PL65C)
(PL65D)
(PL68A)
(PL68B)
LLC_GPLL0T_IN (PL68C)
LLC_GPLL0C_IN (PL68D)
RAM_DQ0
RAM_DQ1
RAM_DQ2
RAM_DQ3
RAM_DQ4
RAM_DQ5
RAM_DQ6
RAM_DQ7
RAM_UDQS
RAM_UDQS#
RAM_UDM
RAM_RAS#
RAM_CAS#
RAM_WE#
RAM_RST#
RAM_DQ8
RAM_DQ9
RAM_DQ10
RAM_DQ11
RAM_DQ12
RAM_DQ13
RAM_DQ14
RAM_DQ15
RAM_LDQS
RAM_LDQS#
RAM_LDM
RAM_CS#
RAM_CK
RAM_CK#
RAM_CKE
RAM_ODT
LFE5UM5G-45F-8BG381C
VTT
C507
10 nF
C508
100 nF
GND
1V35
needs more current capability
FB501
BLM18AG601SN1D
C501
22 µF
C502
C503
1 µF
1 µF
C504
C505
100 nF
1 µF
C506
100 nF
DDR_VDD
1V35
needs more current capability
FB502
BLM18AG601SN1D
C509
22 µF
C510
C511
1 µF
1 µF
C512
C513
100 nF
1 µF
C514
100 nF
DDR_VDDQ
place near memory, one per quarter, vias on side of memory
U501
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
BA0
BA1
BA2
CK
CK#
CKE
RAS#
RESET#
CAS#
CS#
WE#
ODT
VDD
VDDQ
VREFCA
VREFDQ
ZQ
VSS
VSSQ
NC
UDM
UDQS
UDQS#
LDM
LDQS
LDQS#
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
MT41K512M16HA
VTT_REF
C515
10 nF
C516
100 nF
GND
U201Bank 0
Bank 0
ULC_GPLL1T_IN (PT4A)
ULC_GPLL1C_IN (PT4B)
(PT6A)
(PT6B)
(PT9A)
(PT9B)
(PT11A)
(PT11B)
(PT13A)
(PT13B)
(PT15A)
(PT15B)
(PT18A)
(PT18B)
(PT20A)
(PT20B)
(PT27A)
(PT29A)
(PT29B)
(PT31A)
(PT31B)
GR_PCLK0_1 (PT33A)
GR_PCLK0_0 (PT33B)
PCLKT0_1 (PT36A)
PCLKC0_1 (PT36B)
PCLKT0_0 (PT38A)
PCLKC0_0 (PT38B)
RAM_A0
RAM_A1
RAM_A2
RAM_A3
RAM_A4
RAM_A5
RAM_A6
RAM_A7
RAM_A8
RAM_A9
RAM_A10
RAM_A11
RAM_A12
RAM_A13
RAM_A14
RAM_A15
RAM_BA0
RAM_BA1
RAM_BA2
LED2
R519
0 Ω
ECP_PROGRAMN [3]
POWER1_RST [9]
POWER2_RST [10]
DDR_S3 [8]
DDR_S5 [8]
ECP_CLK25 [3]
LED3
LFE5UM5G-45F-8BG381C
VTT
Locate on memory side
R501
R502
R503
R504
R505
R506
R507
R508
R509
R510
R511
R512
R513
R514
R515
R516
R517
R518
R520
R521
R522
R523
R524
R525
R526
R527
R529
R530
50 Ω
RAM_A0
RAM_A13
RAM_A1
RAM_A14
RAM_A2
RAM_A15
RAM_A3
RAM_BA0
RAM_A4
RAM_BA1
RAM_A5
RAM_BA2
RAM_A6
RAM_CKE
RAM_A7
RAM_RAS#
RAM_A8
RAM_CAS#
RAM_A9
RAM_CS#
RAM_A10
RAM_WE#
RAM_A11
RAM_ODT
RAM_A12
RAM_RST#
RAM_CK
RAM_CK#
MAYBE???
C525
10 nF
GND
VTT
C517
100 nF
C518
10 nF
C519
100 nF
C520
10 nF
C521
100 nF
C522
10 nF
C523
100 nF
C524
10 nF
GND
3V3
D501
150060GS75000
R528
4.7 kΩ
LED2
Vf should be > 2.1V, so maybe blue leds?
3V3
D502
150060GS75000
R531
4.7 kΩ
LED3
Consider resistor networks?
Sheet
RAM
Number
5/14
Project
Axiom micro rev3
Revision
0
Drawn by
anuejn & vup
License
CERN-OHL-S V2
Date
20200324
open source hardware

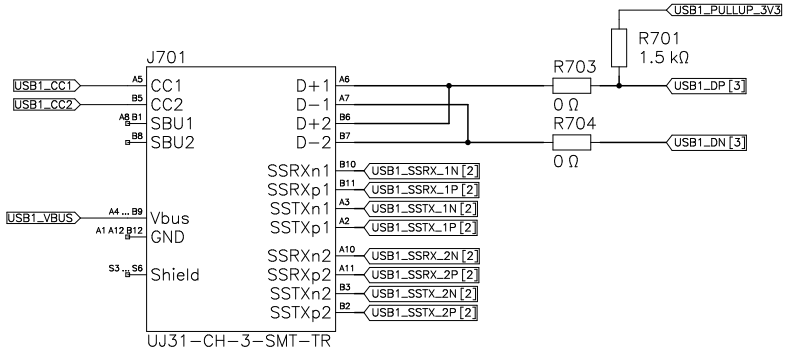
plugin north

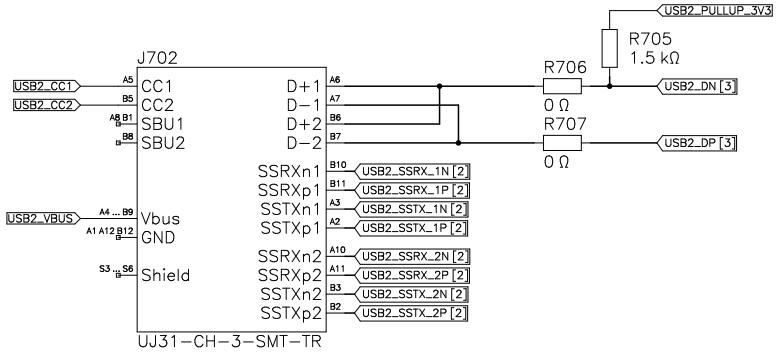


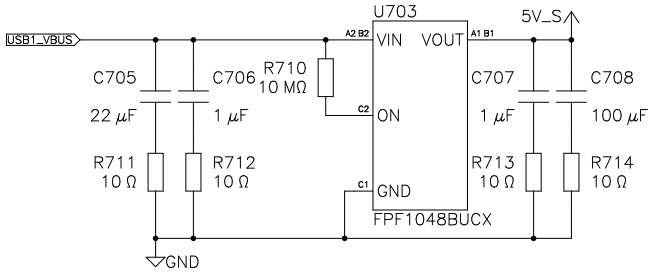
plugin south

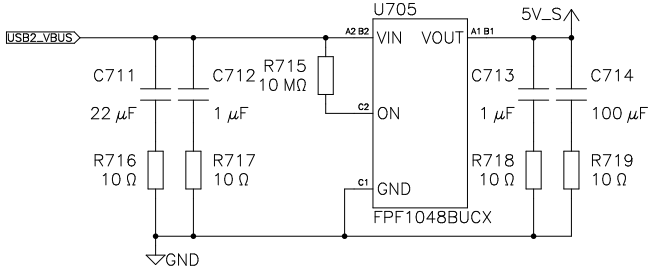


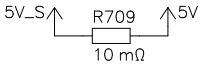
Sheet: plugin	Number: 6/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	open source hardware
Date: 20200324	

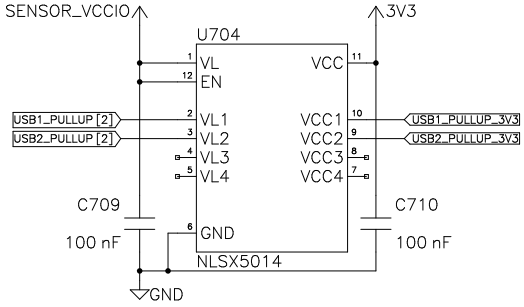


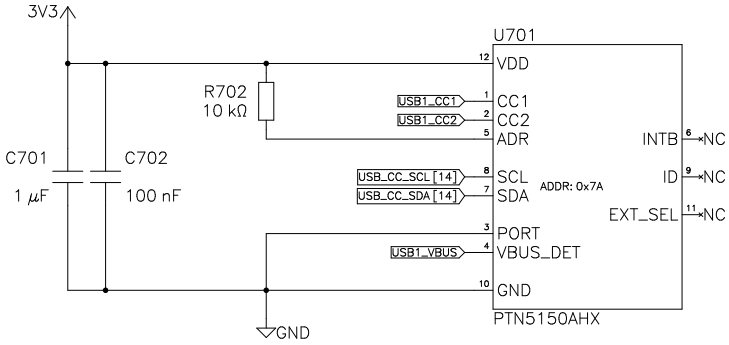


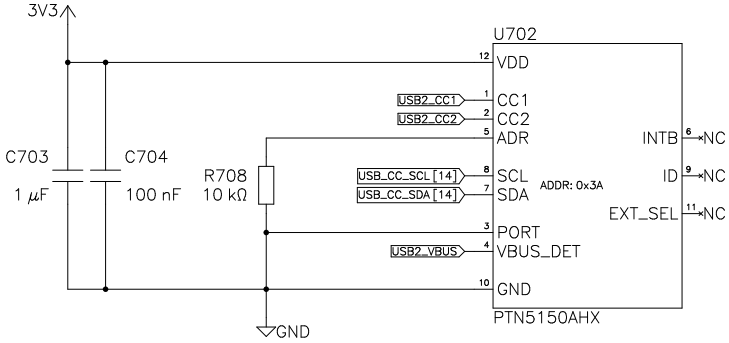












PORT= VDD: DFP mode (R_D = 80uA power default for non−I2C mode).
PORT= Mid (or floating): DRP mode
PORT=GND: UFP mode

Trinary GPIO Input ADR pin run from VDD
– ADR pull up to VDD with 10 kΩ resistor (I2C Enabled with ADDR bit 6 equal to 1, I2C Address 0x7A)
– ADR pull down to GND with 10 kΩ resistor. (I2C Enabled with ADDR bit 6 equal to 0, I2C Address 0x3A)
– ADR = Mid or floating (Pin 6/7/8) configured as OUT1/2/3 in non−I2C mode

Sheet: USB	Number: 7/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN−OHL−S V2	
Date: 20200324	

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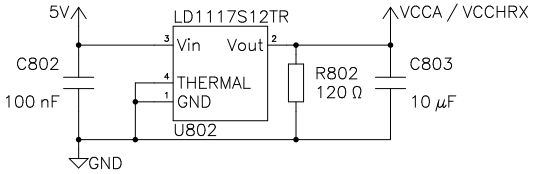
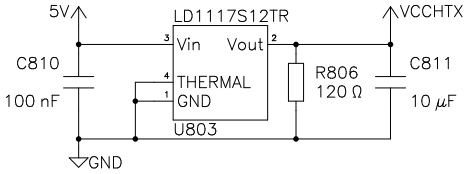
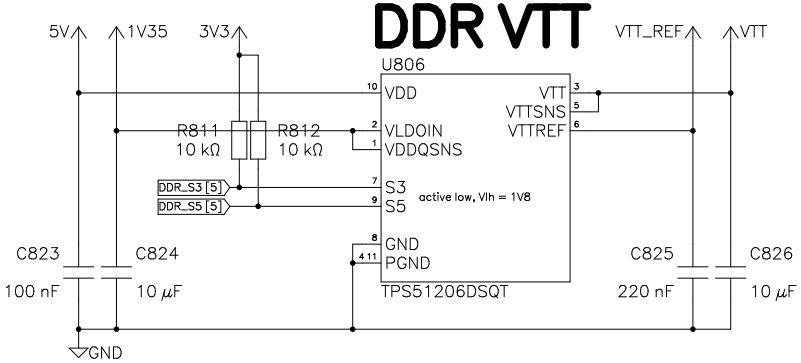


1V2 VCCA / VCCHRX

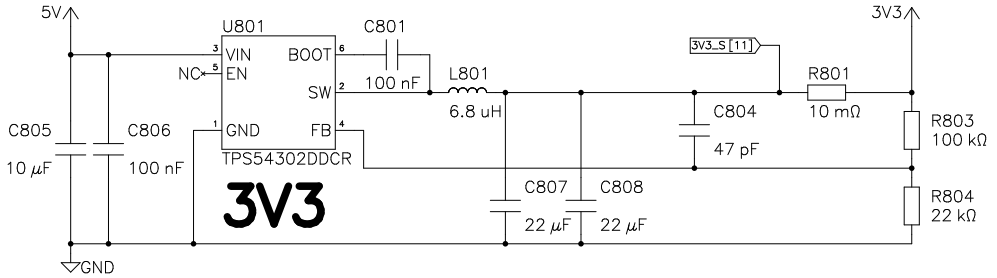


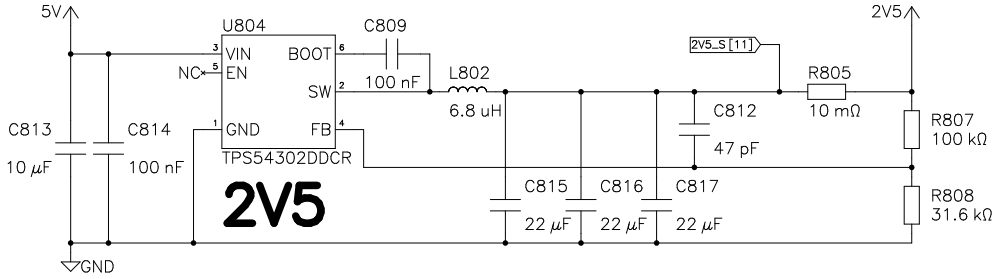
1V2 VCCHTX

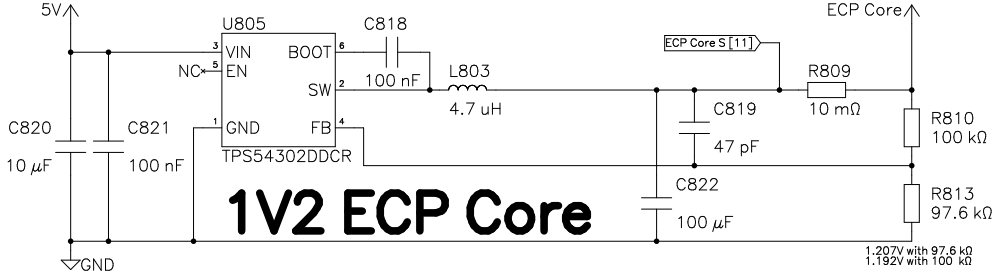
DDR VTT



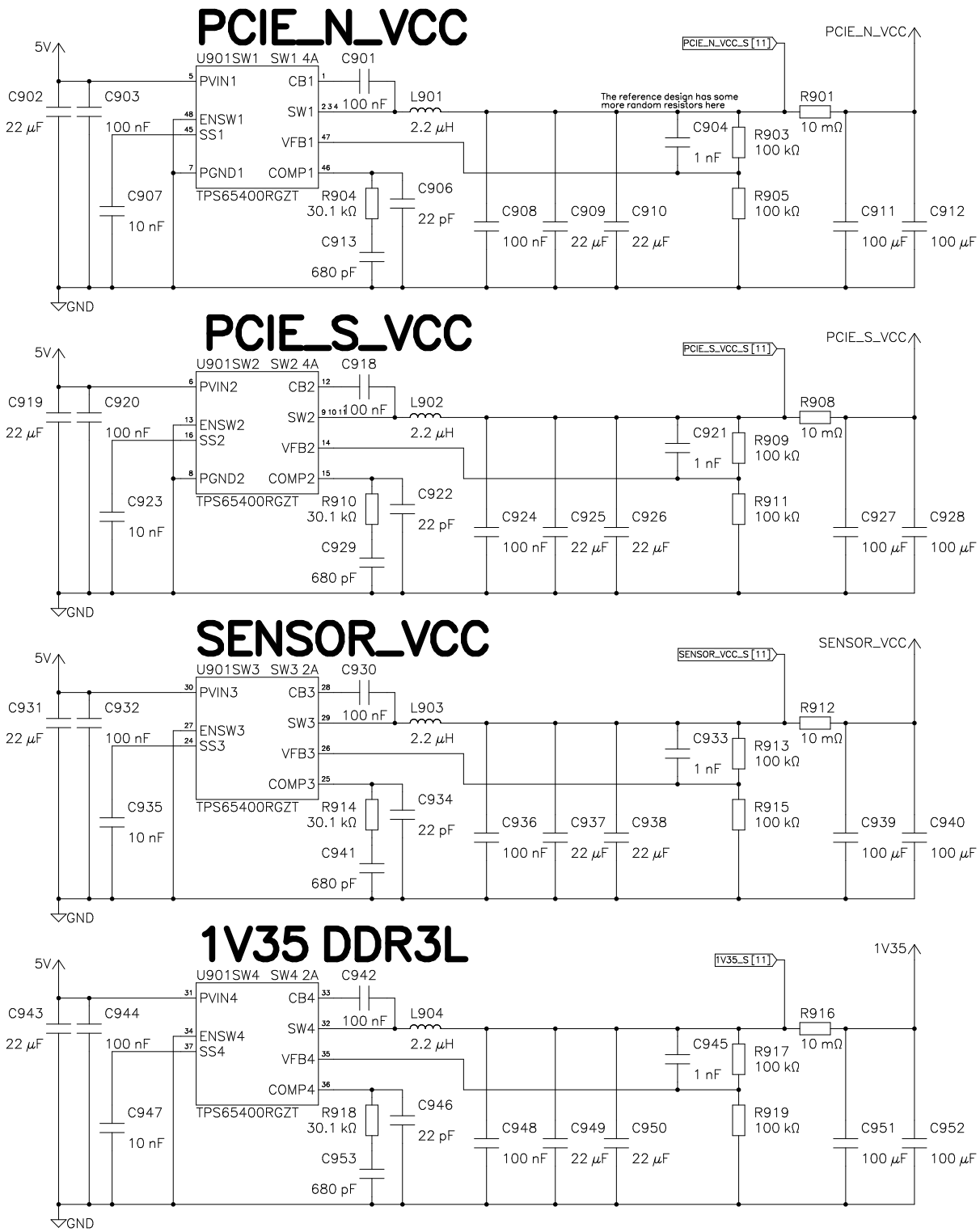
positive terminal of the VTT pin output capacitor(s) as a separate trace from the high–current path from VTT. Consider adding a low–pass R–C filter at the VTTSNS pin in case the ESR of the VTT output capacitor(s) is larger than 2 mΩ. The R–C filter time constant should be approximately the same or slightly lower than the time constant of the VTT output capacitance and ESR.





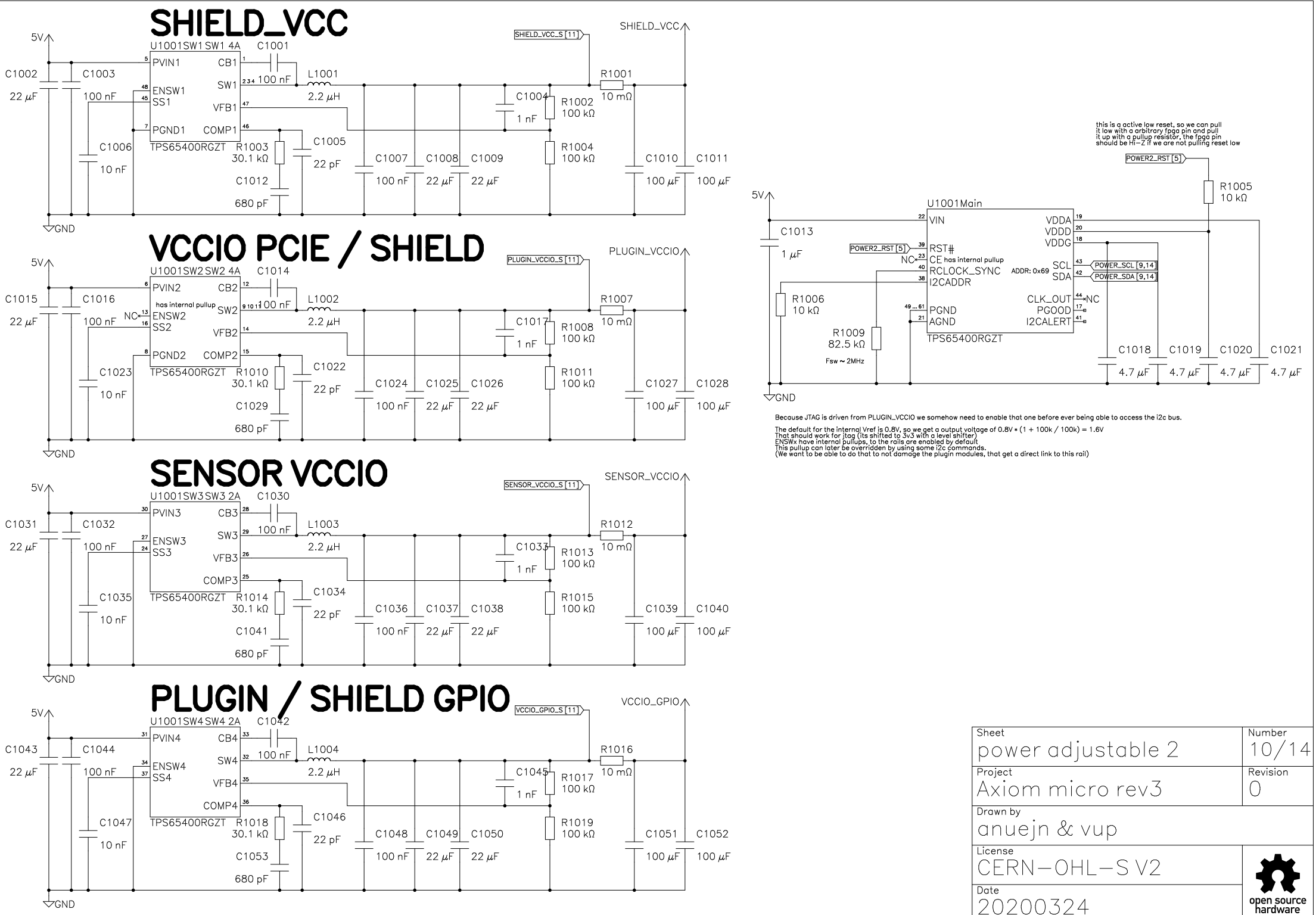


Sheet: power fixed	Number: 8/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN–OHL–S V2	open source hardware
Date: 20200324	



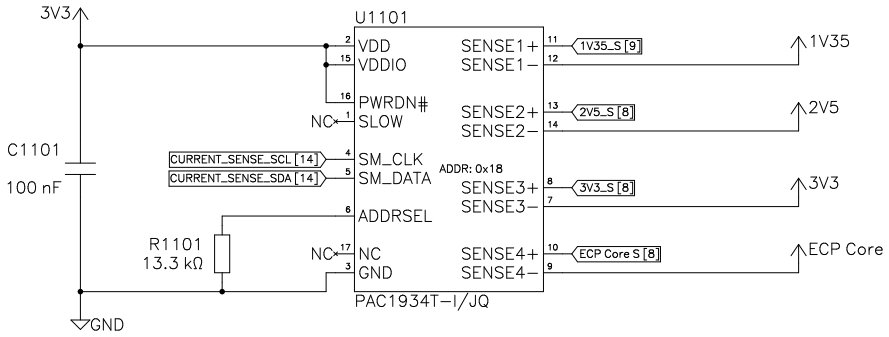
Sheet: power adjustable 1	Number: 9/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	
Date: 20200324	

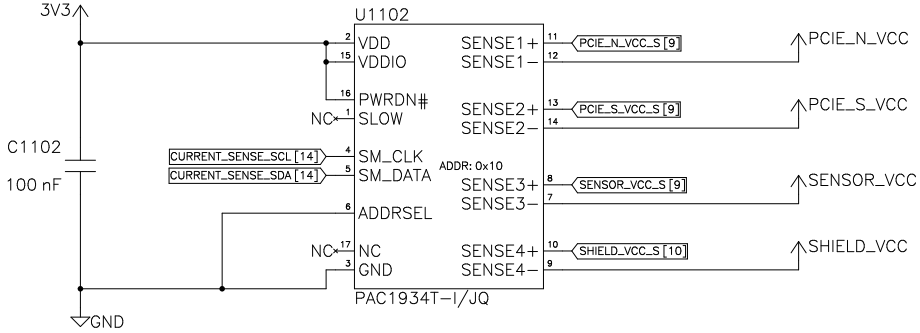
open source hardware

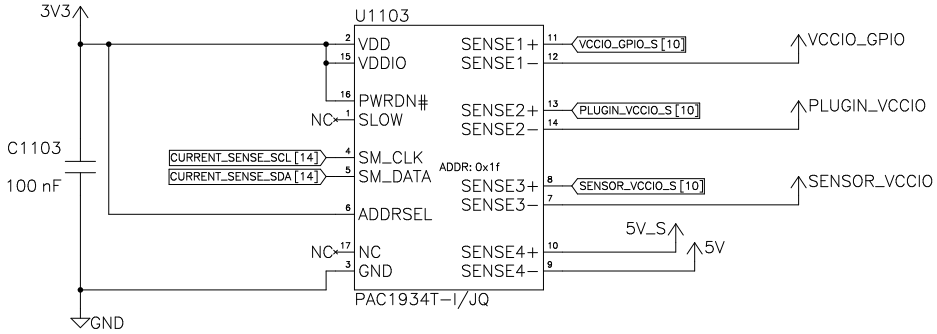


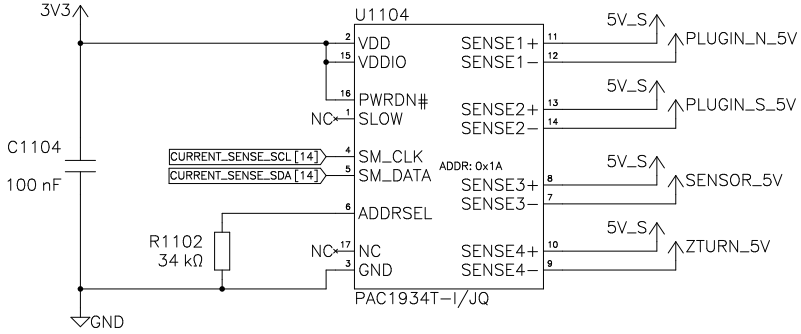
Sheet: power adjustable 2	Number: 10/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	open source hardware
Date: 20200324	

current sense resistors: 0805W8F100MT5E or CS05W8F100MT5E









Sheet: current sense	Number: 11/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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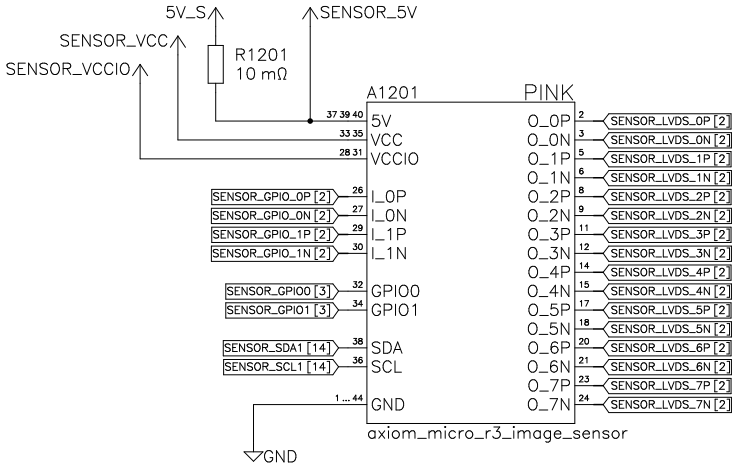

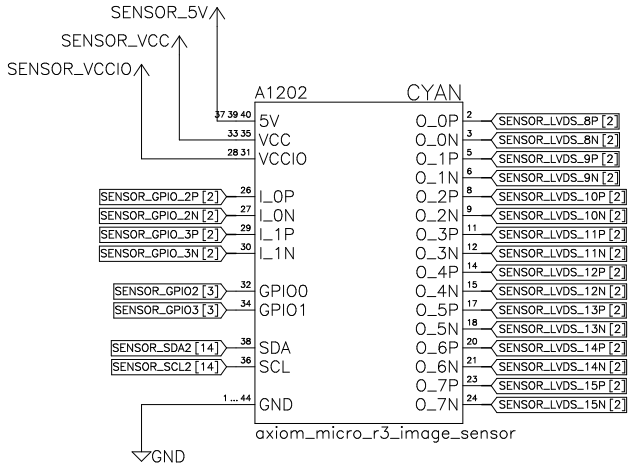

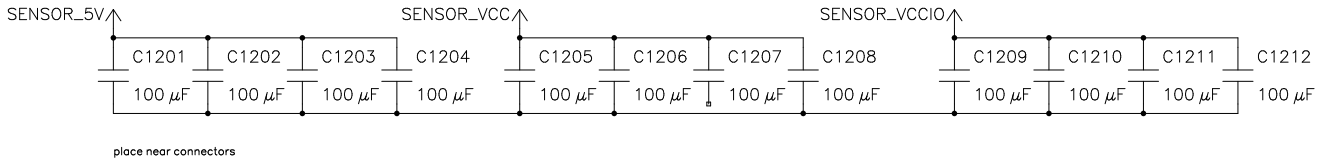

Sheet: image sensor	Number: 12/14
Project: Axiom micro rev3	Revision: 0
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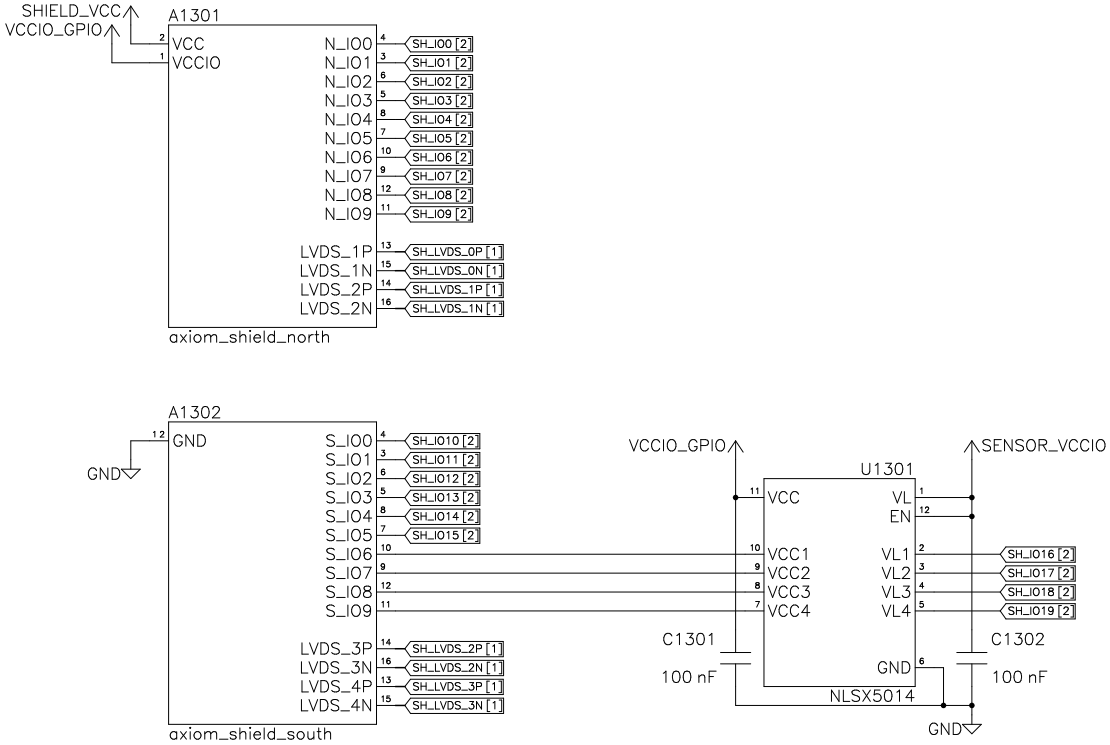
Date: 20200324	



Sheet: shield	Number: 13/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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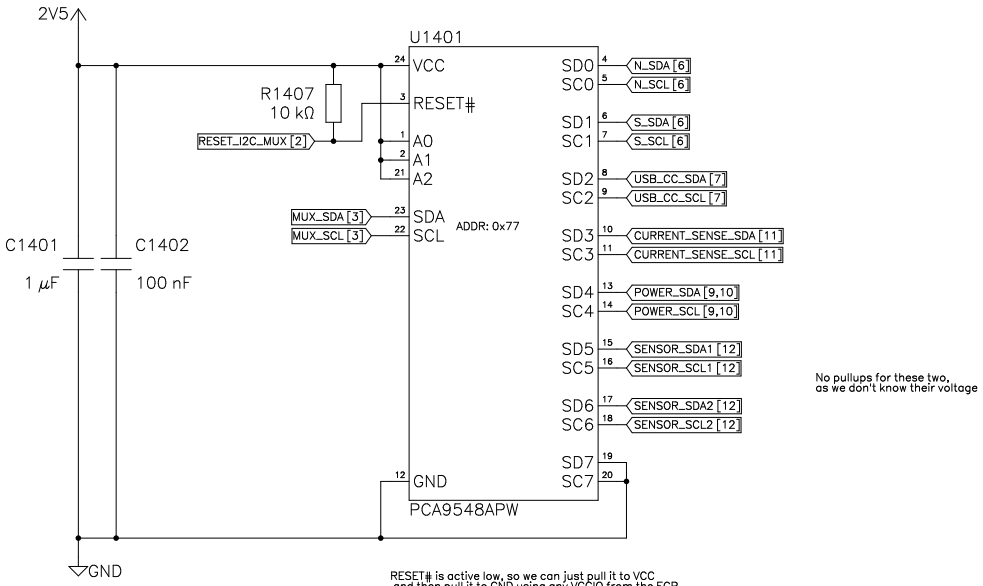
Date: 20200324	

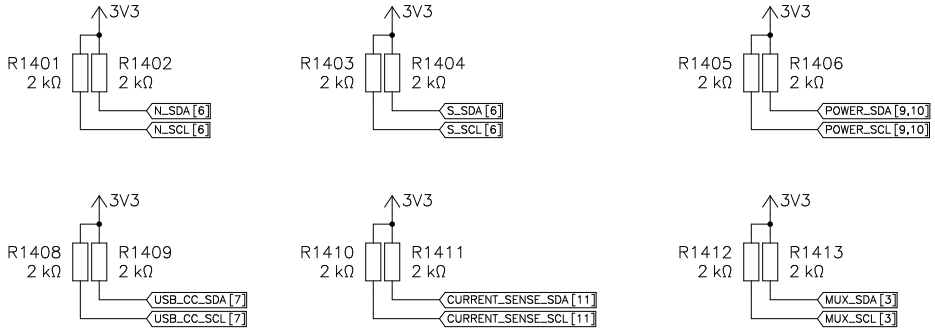


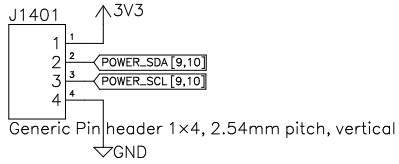
No pullups for these two,
as we don't know their voltage

RESET# is active low, so we can just pull it to VCC
and then pull it to GND using any VCCIO from the ECP,
attention has to be paid to not make RESET# get over VCC,
as otherwise current flows from the RESET pin to the VCC pin,
this should be accomplishable by just making the fpga output Hi-Z
if it is not pullen low

2V5 VCC means about 1V8 voltage clamping by the pass through transistors
That sholud work for most applications, we just need to be careful with nothing with 1V2 is on the bus

Unused channels have to be tied to GND or VCC





Sheet: i2c mux	Number: 14/14
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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