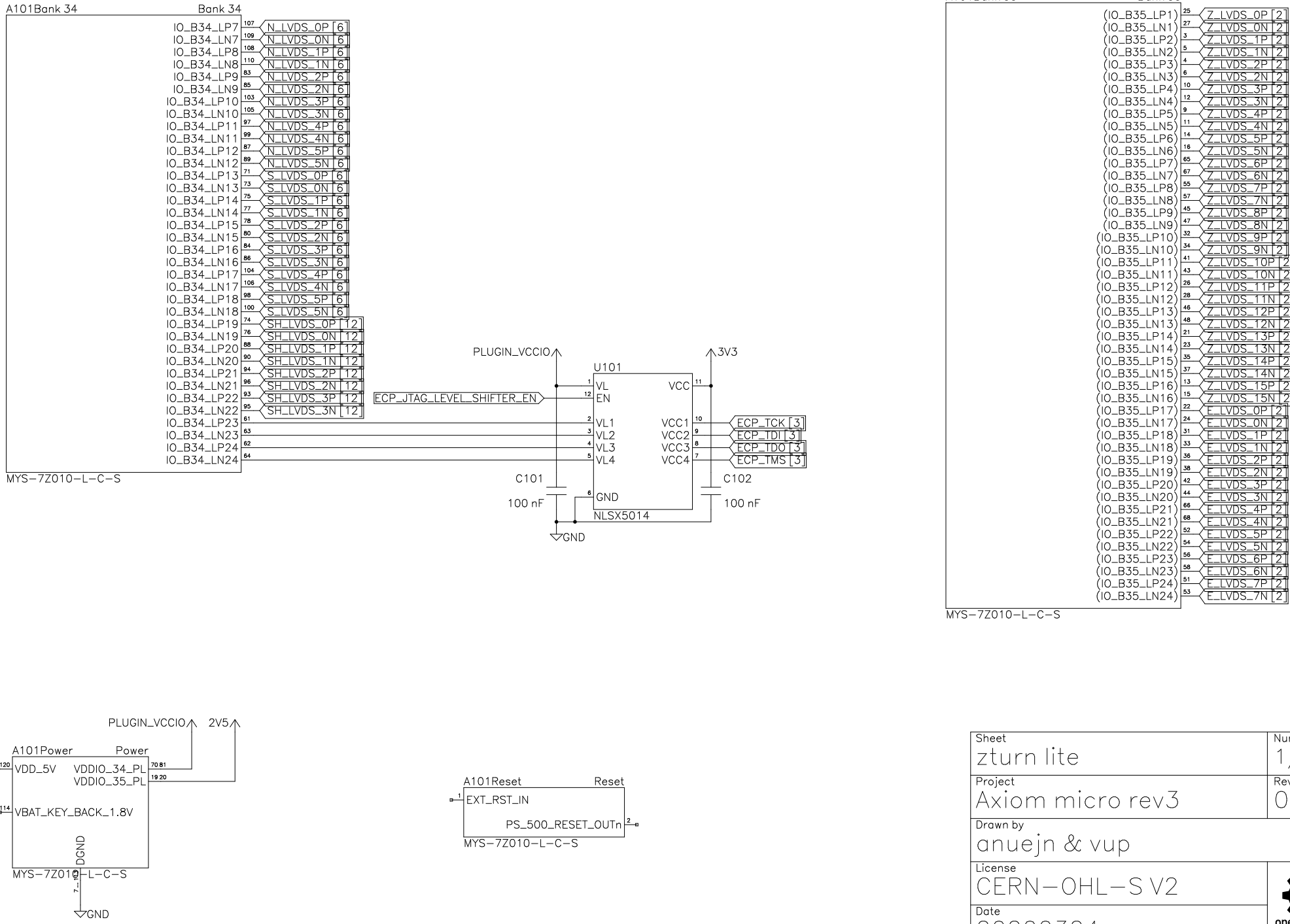
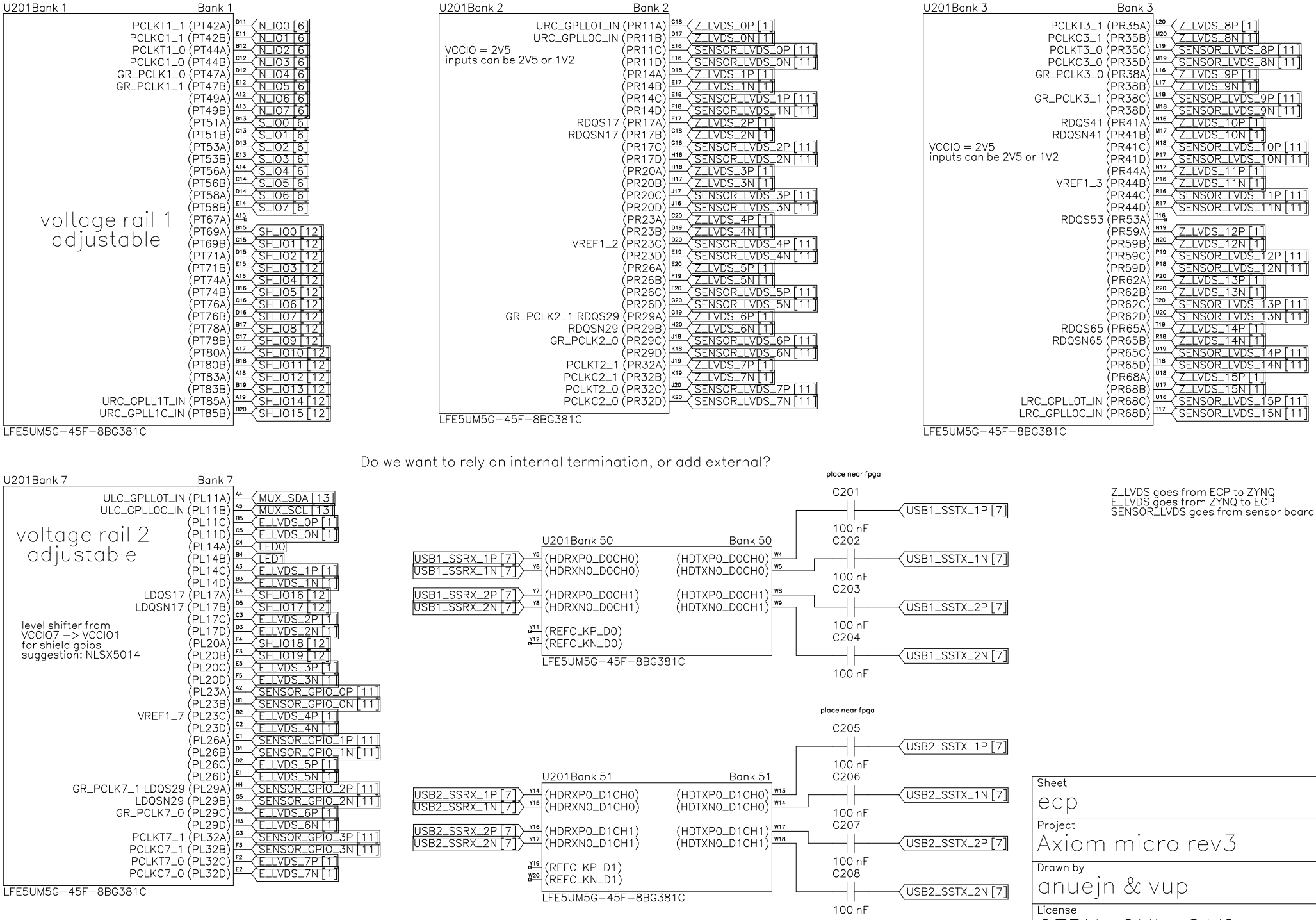
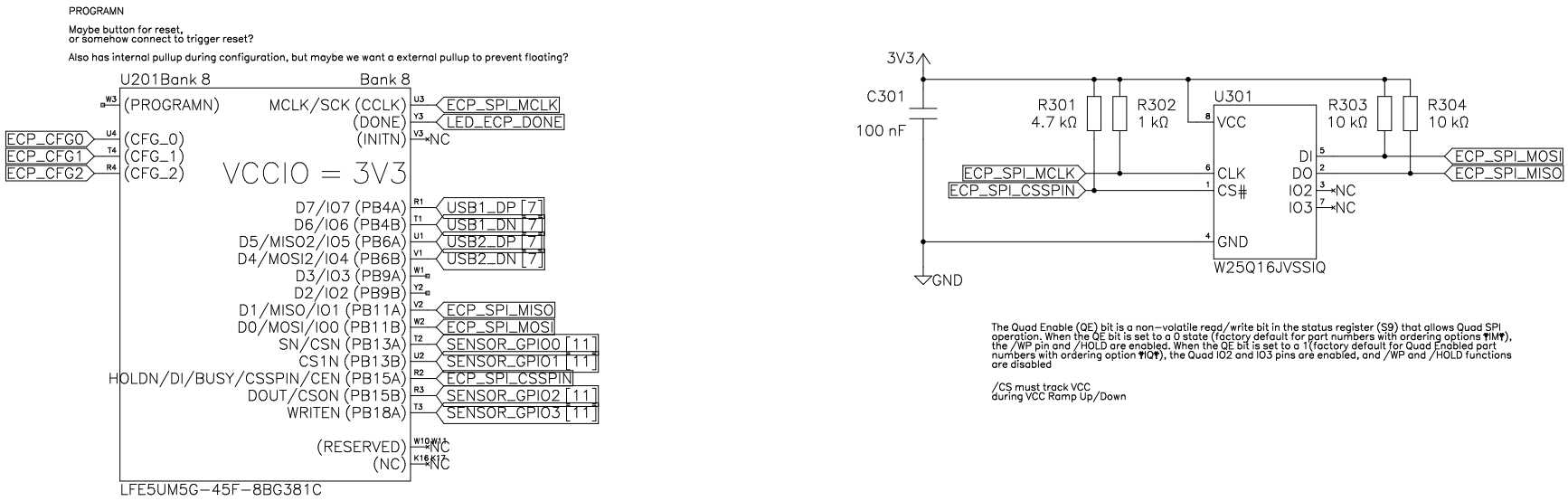


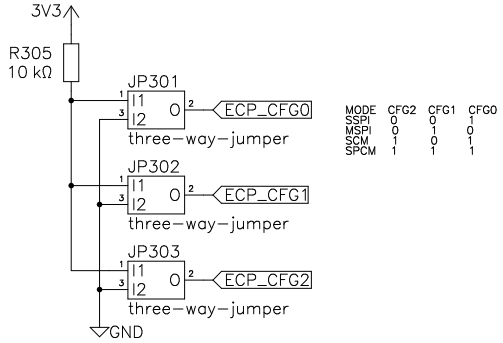
Sheet: zturn lite	Number: 1/13
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	
Date: 20200324	open source hardware


U201Bank 1
Bank 1
PCLKT1_1 (PT42A)
PCLKC1_1 (PT42B)
PCLKT1_0 (PT44A)
PCLKC1_0 (PT44B)
GR_PCLK1_0 (PT47A)
GR_PCLK1_1 (PT47B)
(PT49A)
(PT49B)
(PT51A)
(PT51B)
(PT53A)
(PT53B)
(PT56A)
(PT56B)
(PT58A)
(PT58B)
(PT67A)
(PT69A)
(PT69B)
(PT71A)
(PT71B)
(PT74A)
(PT74B)
(PT76A)
(PT76B)
(PT78A)
(PT78B)
(PT80A)
(PT80B)
(PT83A)
(PT83B)
URC_GPLL1T_IN (PT85A)
URC_GPLL1C_IN (PT85B)
N_IO0 [6]
N_IO1 [6]
N_IO2 [6]
N_IO3 [6]
N_IO4 [6]
N_IO5 [6]
N_IO6 [6]
N_IO7 [6]
S_IO0 [6]
S_IO1 [6]
S_IO2 [6]
S_IO3 [6]
S_IO4 [6]
S_IO5 [6]
S_IO6 [6]
S_IO7 [6]
SH_IO0 [12]
SH_IO1 [12]
SH_IO2 [12]
SH_IO3 [12]
SH_IO4 [12]
SH_IO5 [12]
SH_IO6 [12]
SH_IO7 [12]
SH_IO8 [12]
SH_IO9 [12]
SH_IO10 [12]
SH_IO11 [12]
SH_IO12 [12]
SH_IO13 [12]
SH_IO14 [12]
SH_IO15 [12]
voltage rail 1
adjustable
LFE5UM5G-45F-8BG381C
U201Bank 2
Bank 2
URC_GPLL0T_IN (PR11A)
URC_GPLL0C_IN (PR11B)
VCCIO = 2V5
inputs can be 2V5 or 1V2
(PR11C)
(PR11D)
(PR14A)
(PR14B)
(PR14C)
(PR14D)
RDQS17 (PR17A)
RDQSN17 (PR17B)
(PR17C)
(PR17D)
(PR20A)
(PR20B)
(PR20C)
(PR20D)
(PR23A)
(PR23B)
VREF1_2 (PR23C)
(PR23D)
(PR26A)
(PR26B)
(PR26C)
(PR26D)
GR_PCLK2_1 RDQS29 (PR29A)
RDQSN29 (PR29B)
GR_PCLK2_0 (PR29C)
(PR29D)
PCLKT2_1 (PR32A)
PCLKC2_1 (PR32B)
PCLKT2_0 (PR32C)
PCLKC2_0 (PR32D)
Z_LVDS_0P [1]
Z_LVDS_0N [1]
SENSOR_LVDS_0P [11]
SENSOR_LVDS_0N [11]
Z_LVDS_1P [1]
Z_LVDS_1N [1]
SENSOR_LVDS_1P [11]
SENSOR_LVDS_1N [11]
Z_LVDS_2P [1]
Z_LVDS_2N [1]
SENSOR_LVDS_2P [11]
SENSOR_LVDS_2N [11]
Z_LVDS_3P [1]
Z_LVDS_3N [1]
SENSOR_LVDS_3P [11]
SENSOR_LVDS_3N [11]
Z_LVDS_4P [1]
Z_LVDS_4N [1]
SENSOR_LVDS_4P [11]
SENSOR_LVDS_4N [11]
Z_LVDS_5P [1]
Z_LVDS_5N [1]
SENSOR_LVDS_5P [11]
SENSOR_LVDS_5N [11]
Z_LVDS_6P [1]
Z_LVDS_6N [1]
SENSOR_LVDS_6P [11]
SENSOR_LVDS_6N [11]
Z_LVDS_7P [1]
Z_LVDS_7N [1]
SENSOR_LVDS_7P [11]
SENSOR_LVDS_7N [11]
LFE5UM5G-45F-8BG381C
U201Bank 3
Bank 3
PCLKT3_1 (PR35A)
PCLKC3_1 (PR35B)
PCLKT3_0 (PR35C)
PCLKC3_0 (PR35D)
GR_PCLK3_0 (PR38A)
(PR38B)
GR_PCLK3_1 (PR38C)
(PR38D)
RDQS41 (PR41A)
RDQSN41 (PR41B)
VCCIO = 2V5
inputs can be 2V5 or 1V2
(PR41C)
(PR41D)
(PR44A)
VREF1_3 (PR44B)
(PR44C)
(PR44D)
RDQS53 (PR53A)
(PR59A)
(PR59B)
(PR59C)
(PR59D)
(PR62A)
(PR62B)
(PR62C)
(PR62D)
RDQS65 (PR65A)
RDQSN65 (PR65B)
(PR65C)
(PR65D)
(PR68A)
(PR68B)
LRC_GPLL0T_IN (PR68C)
LRC_GPLL0C_IN (PR68D)
Z_LVDS_8P [1]
Z_LVDS_8N [1]
SENSOR_LVDS_8P [11]
SENSOR_LVDS_8N [11]
Z_LVDS_9P [1]
Z_LVDS_9N [1]
SENSOR_LVDS_9P [11]
SENSOR_LVDS_9N [11]
Z_LVDS_10P [1]
Z_LVDS_10N [1]
SENSOR_LVDS_10P [11]
SENSOR_LVDS_10N [11]
Z_LVDS_11P [1]
Z_LVDS_11N [1]
SENSOR_LVDS_11P [11]
SENSOR_LVDS_11N [11]
Z_LVDS_12P [1]
Z_LVDS_12N [1]
SENSOR_LVDS_12P [11]
SENSOR_LVDS_12N [11]
Z_LVDS_13P [1]
Z_LVDS_13N [1]
SENSOR_LVDS_13P [11]
SENSOR_LVDS_13N [11]
Z_LVDS_14P [1]
Z_LVDS_14N [1]
SENSOR_LVDS_14P [11]
SENSOR_LVDS_14N [11]
Z_LVDS_15P [1]
Z_LVDS_15N [1]
SENSOR_LVDS_15P [11]
SENSOR_LVDS_15N [11]
LFE5UM5G-45F-8BG381C
Do we want to rely on internal termination, or add external?
U201Bank 7
Bank 7
ULC_GPLL0T_IN (PL11A)
ULC_GPLL0C_IN (PL11B)
(PL11C)
(PL11D)
(PL14A)
(PL14B)
(PL14C)
(PL14D)
LDQS17 (PL17A)
LDQSN17 (PL17B)
(PL17C)
(PL17D)
(PL20A)
(PL20B)
(PL20C)
(PL20D)
(PL23A)
(PL23B)
VREF1_7 (PL23C)
(PL23D)
(PL26A)
(PL26B)
(PL26C)
(PL26D)
GR_PCLK7_1 LDQS29 (PL29A)
LDQSN29 (PL29B)
GR_PCLK7_0 (PL29C)
(PL29D)
PCLKT7_1 (PL32A)
PCLKC7_1 (PL32B)
PCLKT7_0 (PL32C)
PCLKC7_0 (PL32D)
MUX_SDA [13]
MUX_SCL [13]
E_LVDS_0P [1]
E_LVDS_0N [1]
LED0
LED1
E_LVDS_1P [1]
E_LVDS_1N [1]
SH_IO16 [12]
SH_IO17 [12]
E_LVDS_2P [1]
E_LVDS_2N [1]
SH_IO18 [12]
SH_IO19 [12]
E_LVDS_3P [1]
E_LVDS_3N [1]
SENSOR_GPIO_0P [11]
SENSOR_GPIO_0N [11]
E_LVDS_4P [1]
E_LVDS_4N [1]
SENSOR_GPIO_1P [11]
SENSOR_GPIO_1N [11]
E_LVDS_5P [1]
E_LVDS_5N [1]
SENSOR_GPIO_2P [11]
SENSOR_GPIO_2N [11]
E_LVDS_6P [1]
E_LVDS_6N [1]
SENSOR_GPIO_3P [11]
SENSOR_GPIO_3N [11]
E_LVDS_7P [1]
E_LVDS_7N [1]
voltage rail 2
adjustable
level shifter from
VCCIO7 -> VCCIO1
for shield gpios
suggestion: NLSX5014
LFE5UM5G-45F-8BG381C
place near fpga
C201
C202
C203
C204
100 nF
U201Bank 50
Bank 50
USB1_SSRX_1P [7]
USB1_SSRX_1N [7]
USB1_SSRX_2P [7]
USB1_SSRX_2N [7]
(HDRXP0_D0CH0)
(HDRXN0_D0CH0)
(HDRXP0_D0CH1)
(HDRXN0_D0CH1)
(REFCLKP_D0)
(REFCLKN_D0)
(HDTXP0_D0CH0)
(HDTXN0_D0CH0)
(HDTXP0_D0CH1)
(HDTXN0_D0CH1)
USB1_SSTX_1P [7]
USB1_SSTX_1N [7]
USB1_SSTX_2P [7]
USB1_SSTX_2N [7]
LFE5UM5G-45F-8BG381C
place near fpga
C205
C206
C207
C208
100 nF
U201Bank 51
Bank 51
USB2_SSRX_1P [7]
USB2_SSRX_1N [7]
USB2_SSRX_2P [7]
USB2_SSRX_2N [7]
(HDRXP0_D1CH0)
(HDRXN0_D1CH0)
(HDRXP0_D1CH1)
(HDRXN0_D1CH1)
(REFCLKP_D1)
(REFCLKN_D1)
(HDTXP0_D1CH0)
(HDTXN0_D1CH0)
(HDTXP0_D1CH1)
(HDTXN0_D1CH1)
USB2_SSTX_1P [7]
USB2_SSTX_1N [7]
USB2_SSTX_2P [7]
USB2_SSTX_2N [7]
LFE5UM5G-45F-8BG381C
Z_LVDS goes from ECP to ZYNQ
E_LVDS goes from ZYNQ to ECP
SENSOR_LVDS goes from sensor board to ECP
Sheet
ecp
Number
2/13
Project
Axiom micro rev3
Revision
0
Drawn by
anuejn & vup
License
CERN-OHL-S V2
Date
20200324
open source hardware

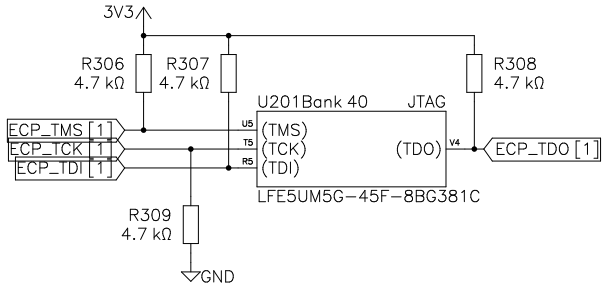


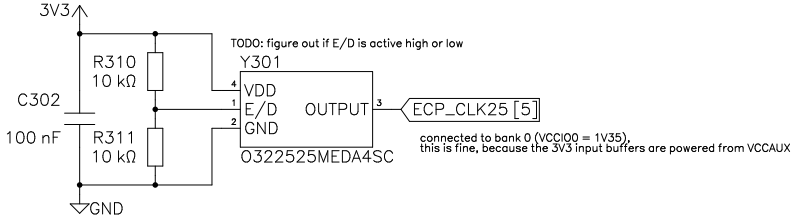
The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI operation. When the QE bit is set to a 0 state (factory default for part numbers with ordering options ŦIMŦ), the /WP pin and /HOLD are enabled. When the QE bit is set to a 1 (factory default for Quad Enabled part numbers with ordering option ŦIQŦ), the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled

/CS must track VCC
during VCC Ramp Up/Down



MODE	CFG2	CFG1	CFG0
SSPI	0	0	1
MSPI	0	1	0
SCM	1	0	1
SPCM	1	1	1





Sheet: ecp config	Number: 3/13
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	
Date: 20200324	

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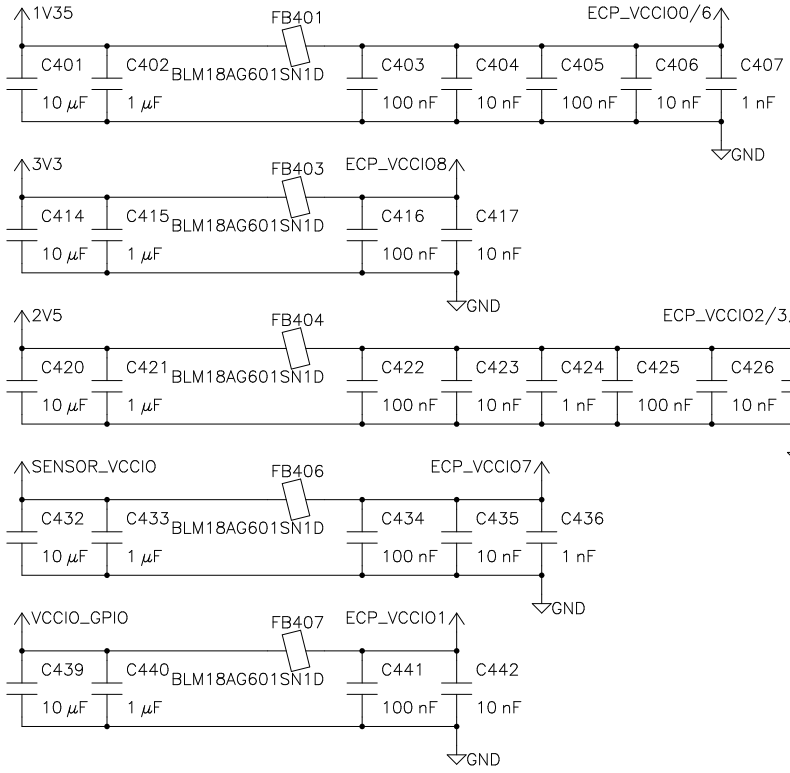
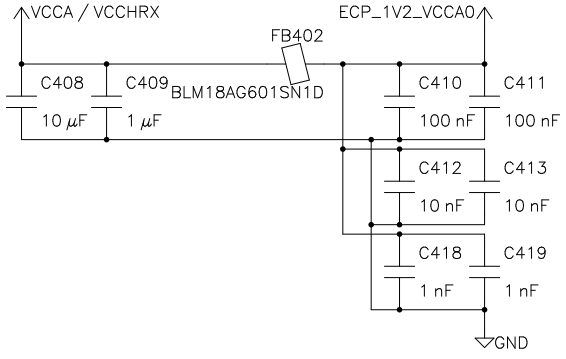
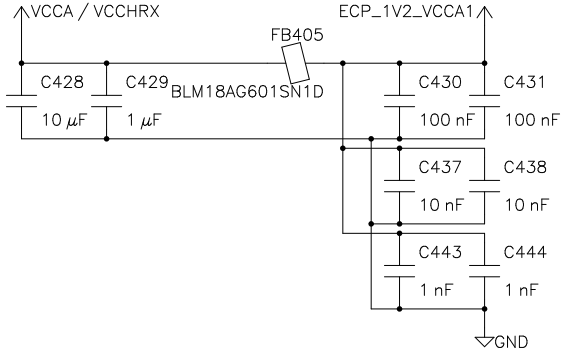
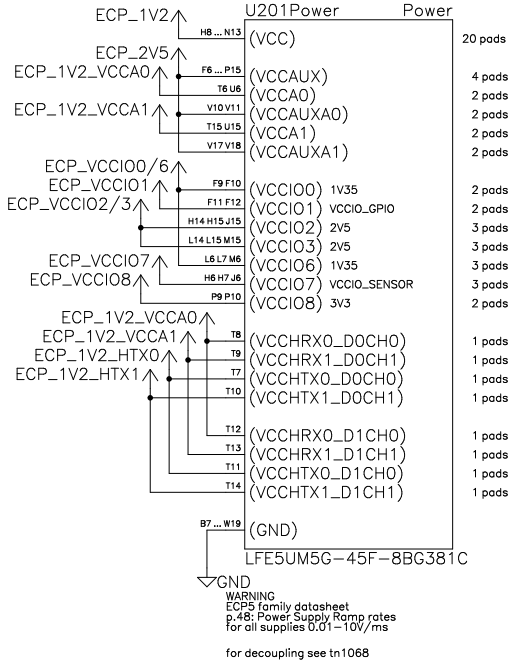
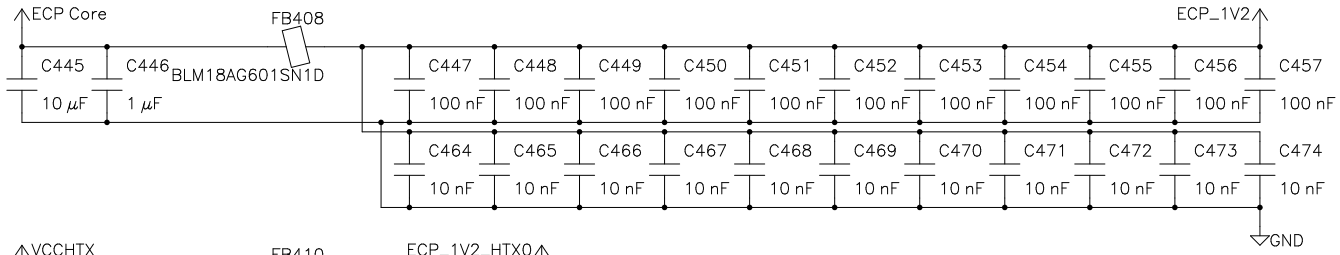
Place decoupling near FPGA, alternate 100n and 10n per pad per rail

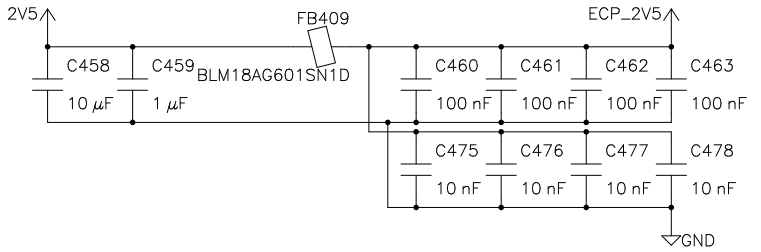


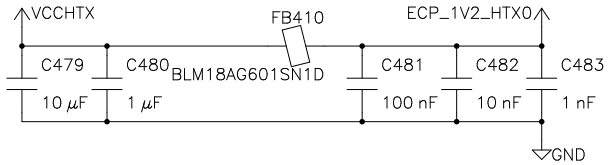


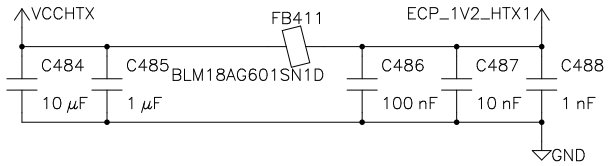




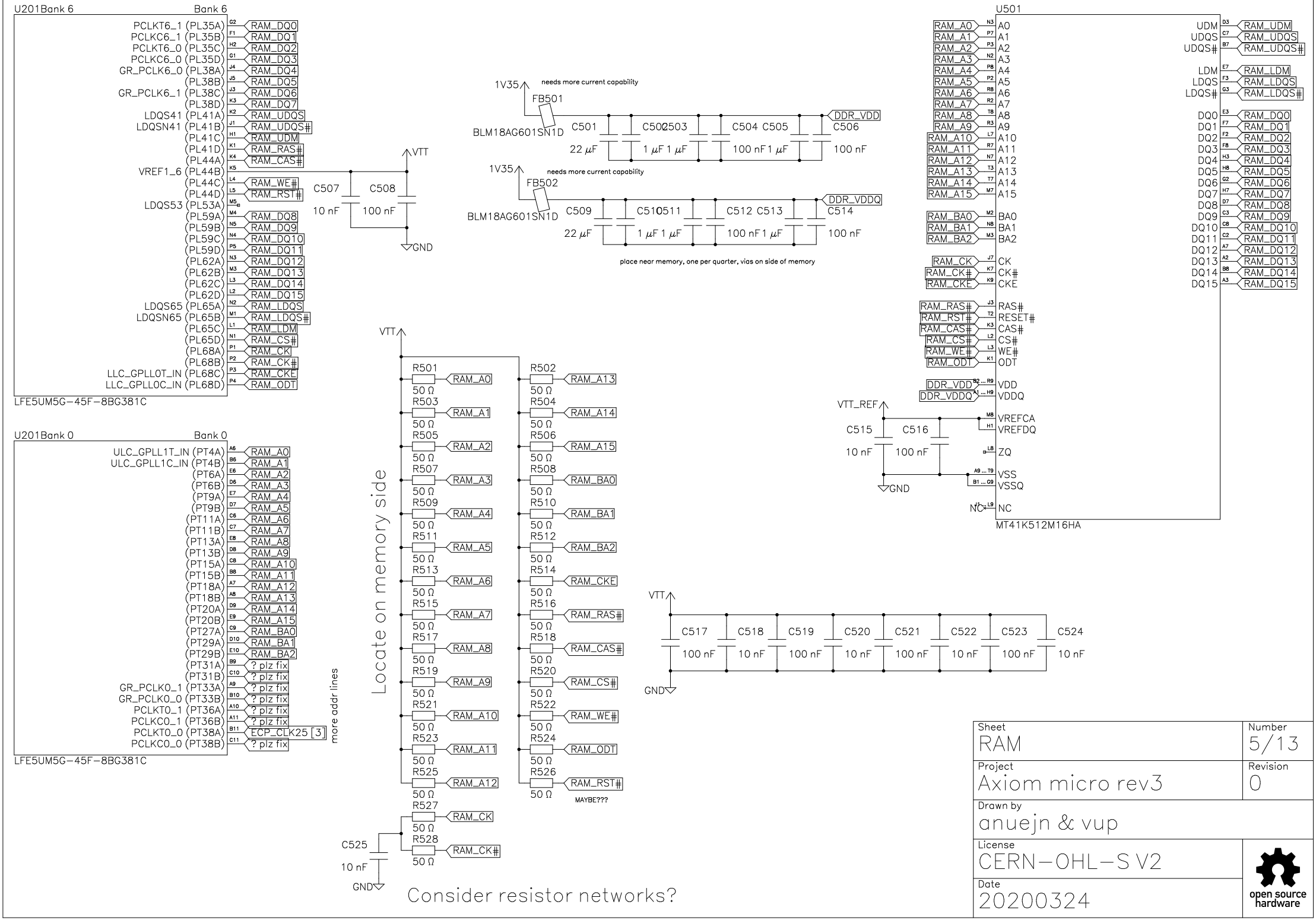




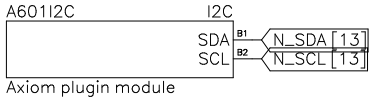




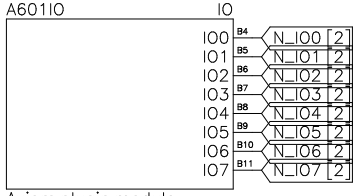
Sheet: ecp power	Number: 4/13
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	open source hardware
Date: 20200324	


U201Bank 6
Bank 6
PCLKT6_1 (PL35A) G2 RAM_DQ0
PCLKC6_1 (PL35B) F1 RAM_DQ1
PCLKT6_0 (PL35C) H2 RAM_DQ2
PCLKC6_0 (PL35D) G1 RAM_DQ3
GR_PCLK6_0 (PL38A) J4 RAM_DQ4
(PL38B) J5 RAM_DQ5
GR_PCLK6_1 (PL38C) J3 RAM_DQ6
(PL38D) K3 RAM_DQ7
LDQS41 (PL41A) K2 RAM_UDQS
LDQSN41 (PL41B) J1 RAM_UDQS#
(PL41C) H1 RAM_UDM
(PL41D) K1 RAM_RAS#
(PL44A) K4 RAM_CAS#
VREF1_6 (PL44B) K5
(PL44C) L4 RAM_WE#
(PL44D) L5 RAM_RST#
LDQS53 (PL53A) M5
(PL59A) M4 RAM_DQ8
(PL59B) N5 RAM_DQ9
(PL59C) N4 RAM_DQ10
(PL59D) P5 RAM_DQ11
(PL62A) N3 RAM_DQ12
(PL62B) M3 RAM_DQ13
(PL62C) L3 RAM_DQ14
(PL62D) L2 RAM_DQ15
LDQS65 (PL65A) N2 RAM_LDQS
LDQSN65 (PL65B) M1 RAM_LDQS#
(PL65C) L1 RAM_LDM
(PL65D) N1 RAM_CS#
(PL68A) P1 RAM_CK
(PL68B) P2 RAM_CK#
LLC_GPLL0T_IN (PL68C) P3 RAM_CKE
LLC_GPLL0C_IN (PL68D) P4 RAM_ODT
LFE5UM5G-45F-8BG381C
VTT
C507 10 nF
C508 100 nF
GND
U201Bank 0
Bank 0
ULC_GPLL1T_IN (PT4A) A6 RAM_A0
ULC_GPLL1C_IN (PT4B) B6 RAM_A1
(PT6A) E6 RAM_A2
(PT6B) D6 RAM_A3
(PT9A) E7 RAM_A4
(PT9B) D7 RAM_A5
(PT11A) C6 RAM_A6
(PT11B) C7 RAM_A7
(PT13A) E8 RAM_A8
(PT13B) D8 RAM_A9
(PT15A) C8 RAM_A10
(PT15B) B8 RAM_A11
(PT18A) A7 RAM_A12
(PT18B) A8 RAM_A13
(PT20A) D9 RAM_A14
(PT20B) E9 RAM_A15
(PT27A) C9 RAM_BA0
(PT29A) D10 RAM_BA1
(PT29B) E10 RAM_BA2
(PT31A) B9 ? plz fix
(PT31B) C10 ? plz fix
GR_PCLK0_1 (PT33A) A9 ? plz fix
GR_PCLK0_0 (PT33B) B10 ? plz fix
PCLKT0_1 (PT36A) A10 ? plz fix
PCLKC0_1 (PT36B) A11 ? plz fix
PCLKT0_0 (PT38A) B11 ECP_CLK25 [3]
PCLKC0_0 (PT38B) C11 ? plz fix
LFE5UM5G-45F-8BG381C
more addr lines
1V35
needs more current capability
FB501
BLM18AG601SN1D
C501 22 µF
C502 1 µF
C503 1 µF
C504 100 nF
C505 1 µF
C506 100 nF
DDR_VDD
1V35
needs more current capability
FB502
BLM18AG601SN1D
C509 22 µF
C510 1 µF
C511 1 µF
C512 100 nF
C513 1 µF
C514 100 nF
DDR_VDDQ
place near memory, one per quarter, vias on side of memory
U501
RAM_A0 N3 A0
RAM_A1 P7 A1
RAM_A2 P3 A2
RAM_A3 N2 A3
RAM_A4 P8 A4
RAM_A5 P2 A5
RAM_A6 R8 A6
RAM_A7 R2 A7
RAM_A8 T8 A8
RAM_A9 R3 A9
RAM_A10 L7 A10
RAM_A11 R7 A11
RAM_A12 N7 A12
RAM_A13 T3 A13
RAM_A14 T7 A14
RAM_A15 M7 A15
RAM_BA0 M2 BA0
RAM_BA1 N8 BA1
RAM_BA2 M3 BA2
RAM_CK J7 CK
RAM_CK# K7 CK#
RAM_CKE K9 CKE
RAM_RAS# J3 RAS#
RAM_RST# T2 RESET#
RAM_CAS# K3 CAS#
RAM_CS# L2 CS#
RAM_WE# L3 WE#
RAM_ODT K1 ODT
DDR_VDD B2 ... R9 VDD
DDR_VDDQ A1 ... H9 VDDQ
M8 VREFCA
H1 VREFDQ
L8 ZQ
A9 ... T9 VSS
B1 ... G9 VSSQ
NC L9 NC
UDM D3 RAM_UDM
UDQS C7 RAM_UDQS
UDQS# B7 RAM_UDQS#
LDM E7 RAM_LDM
LDQS F3 RAM_LDQS
LDQS# G3 RAM_LDQS#
DQ0 E3 RAM_DQ0
DQ1 F7 RAM_DQ1
DQ2 F2 RAM_DQ2
DQ3 F8 RAM_DQ3
DQ4 H3 RAM_DQ4
DQ5 H8 RAM_DQ5
DQ6 G2 RAM_DQ6
DQ7 H7 RAM_DQ7
DQ8 D7 RAM_DQ8
DQ9 C3 RAM_DQ9
DQ10 C8 RAM_DQ10
DQ11 C2 RAM_DQ11
DQ12 A7 RAM_DQ12
DQ13 A2 RAM_DQ13
DQ14 B8 RAM_DQ14
DQ15 A3 RAM_DQ15
MT41K512M16HA
VTT_REF
C515 10 nF
C516 100 nF
GND
VTT
Locate on memory side
R501 50 Ω RAM_A0
R502 50 Ω RAM_A13
R503 50 Ω RAM_A1
R504 50 Ω RAM_A14
R505 50 Ω RAM_A2
R506 50 Ω RAM_A15
R507 50 Ω RAM_A3
R508 50 Ω RAM_BA0
R509 50 Ω RAM_A4
R510 50 Ω RAM_BA1
R511 50 Ω RAM_A5
R512 50 Ω RAM_BA2
R513 50 Ω RAM_A6
R514 50 Ω RAM_CKE
R515 50 Ω RAM_A7
R516 50 Ω RAM_RAS#
R517 50 Ω RAM_A8
R518 50 Ω RAM_CAS#
R519 50 Ω RAM_A9
R520 50 Ω RAM_CS#
R521 50 Ω RAM_A10
R522 50 Ω RAM_WE#
R523 50 Ω RAM_A11
R524 50 Ω RAM_ODT
R525 50 Ω RAM_A12
R526 50 Ω RAM_RST#
MAYBE???
R527 50 Ω RAM_CK
R528 50 Ω RAM_CK#
C525 10 nF
GND
Consider resistor networks?
VTT
C517 100 nF
C518 10 nF
C519 100 nF
C520 10 nF
C521 100 nF
C522 10 nF
C523 100 nF
C524 10 nF
GND
Sheet
RAM
Number
5/13
Project
Axiom micro rev3
Revision
0
Drawn by
anuejn & vup
License
CERN-OHL-S V2
Date
20200324
open source hardware

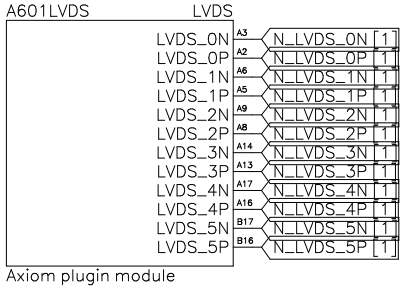
plugin north



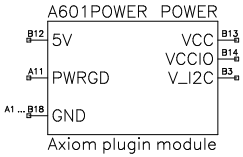
Axiom plugin module



Axiom plugin module

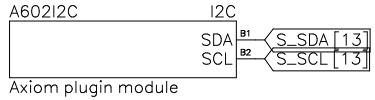


Axiom plugin module

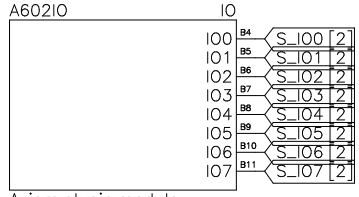


Axiom plugin module

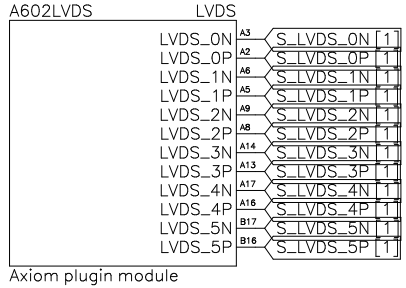
plugin south



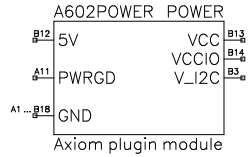
Axiom plugin module



Axiom plugin module



Axiom plugin module



Axiom plugin module

Sheet plugin	Number 6/13
Project Axiom micro rev3	Revision 0
Drawn by anuejn & vup	
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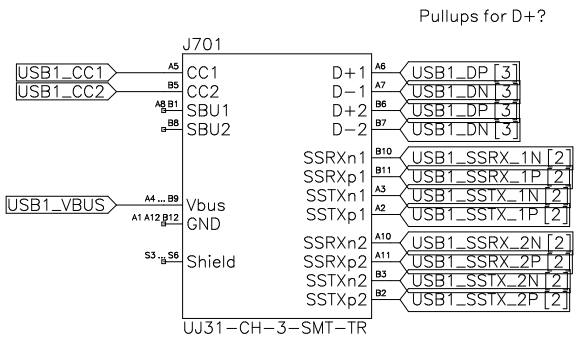
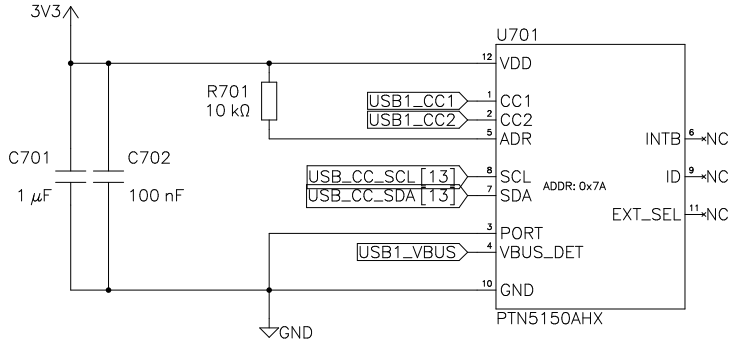
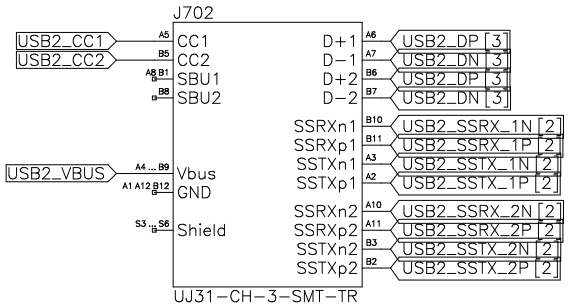
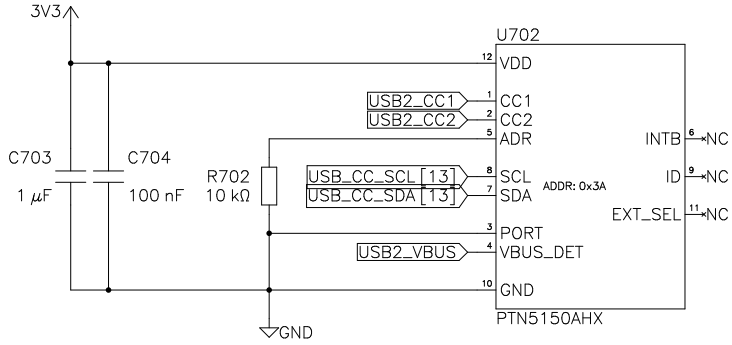


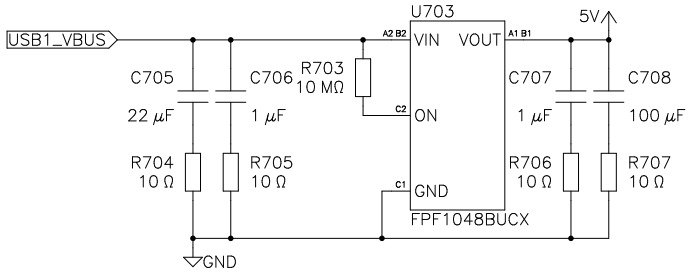


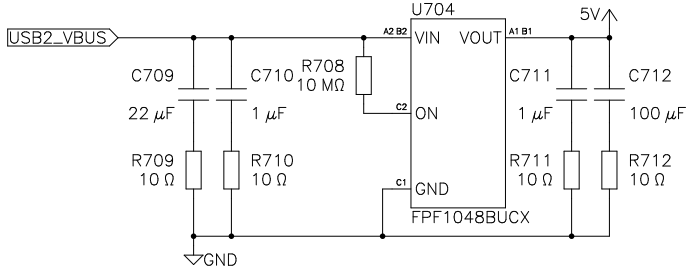
PORT= VDD: DFP mode (R_p = 80uA power default for non−I2C mode).
PORT= Mid (or floating): DRP mode
PORT=GND: UFP mode

Tringry GPIO Input ADR pin run from VDD
− ADR pull up to VDD with 10 kΩ resistor (I2C Enabled with ADDR bit 6 equal to 1, I2C Address 0x7A)
− ADR pull down to GND with 10 kΩ resistor. (I2C Enabled with ADDR bit 6 equal to 0, I2C Address 0x3A)
− ADR = Mid or floating (Pin 6/7/8) configured as OUT1/2/3 in non−I2C mode









Sheet: USB	Number: 7/13
Project: Axiom micro rev3	Revision: 0
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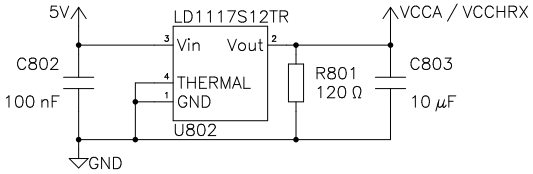
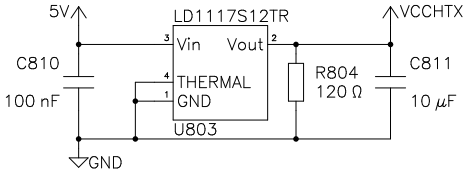
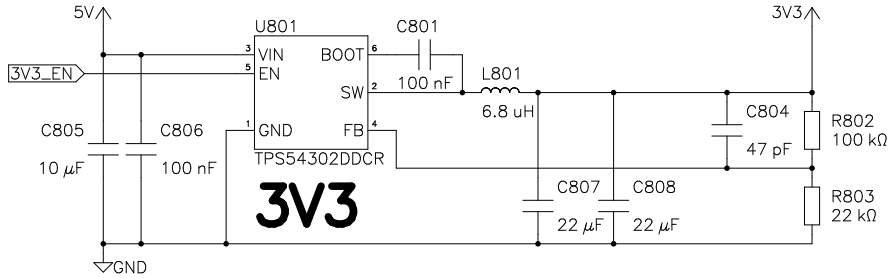


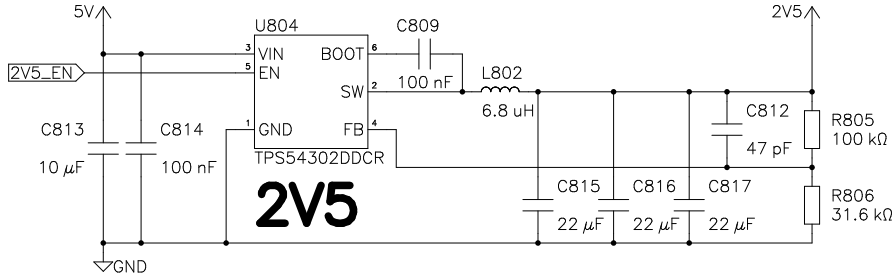
1V2 VCCA / VCCHRX



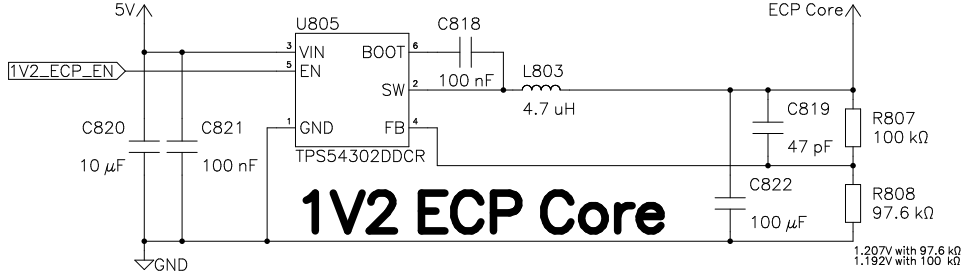
1V2 VCCHTX



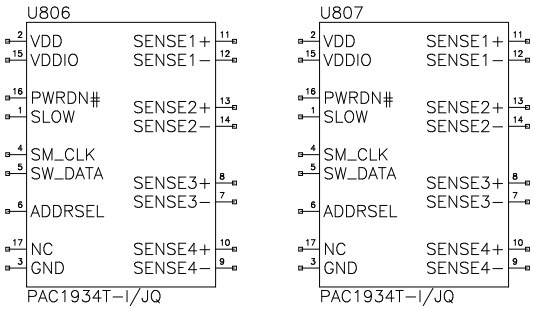
3V3

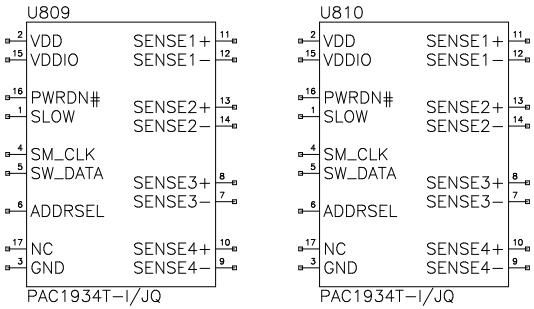


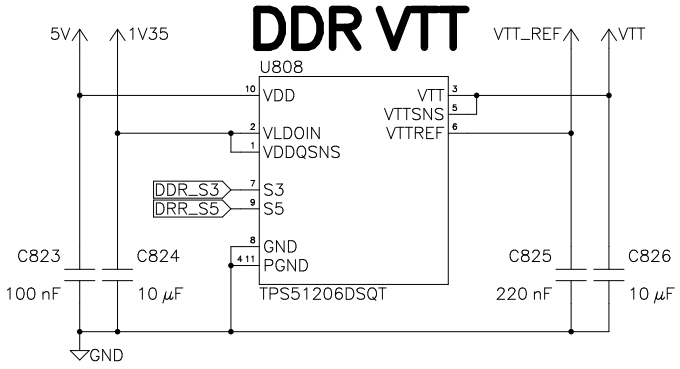
2V5



1V2 ECP Core







positive terminal of the VTT pin output capacitor(s) as a separate trace from the high−current path from VTT. Consider adding a low−pass R−C filter at the VTTSNS pin in case the ESR of the VTT output capacitor(s) is larger than 2 mΩ. The R−C filter time constant should be approximately the same or slightly lower than the time constant of the VTT output capacitance and ESR.

Sheet: power fixed	Number: 8/13
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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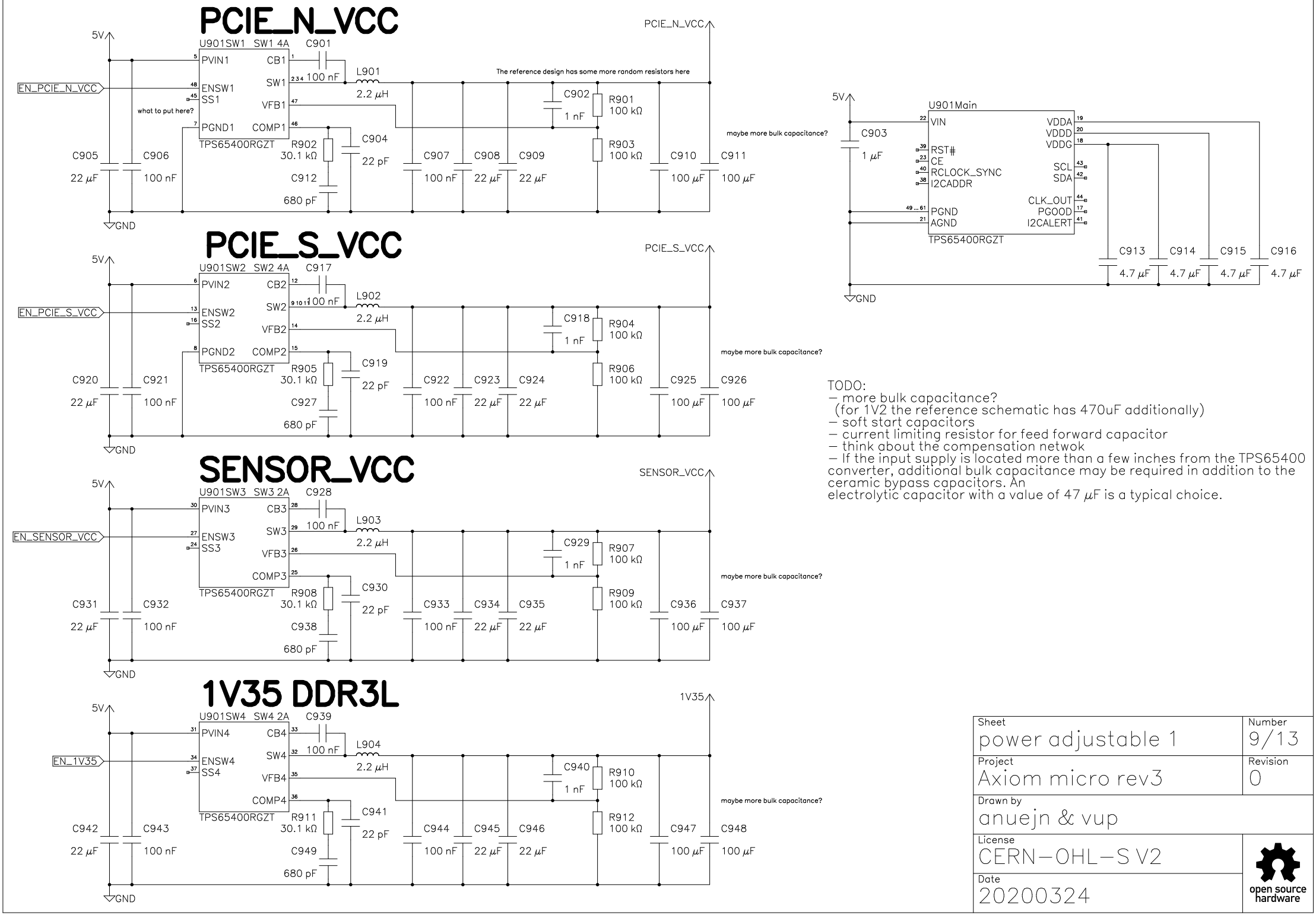

TODO:
- more bulk capacitance?
  (for 1V2 the reference schematic has 470uF additionally)
- soft start capacitors
- current limiting resistor for feed forward capacitor
- think about the compensation netwok
- If the input supply is located more than a few inches from the TPS65400 converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

Sheet: power adjustable 1	Number: 9/13
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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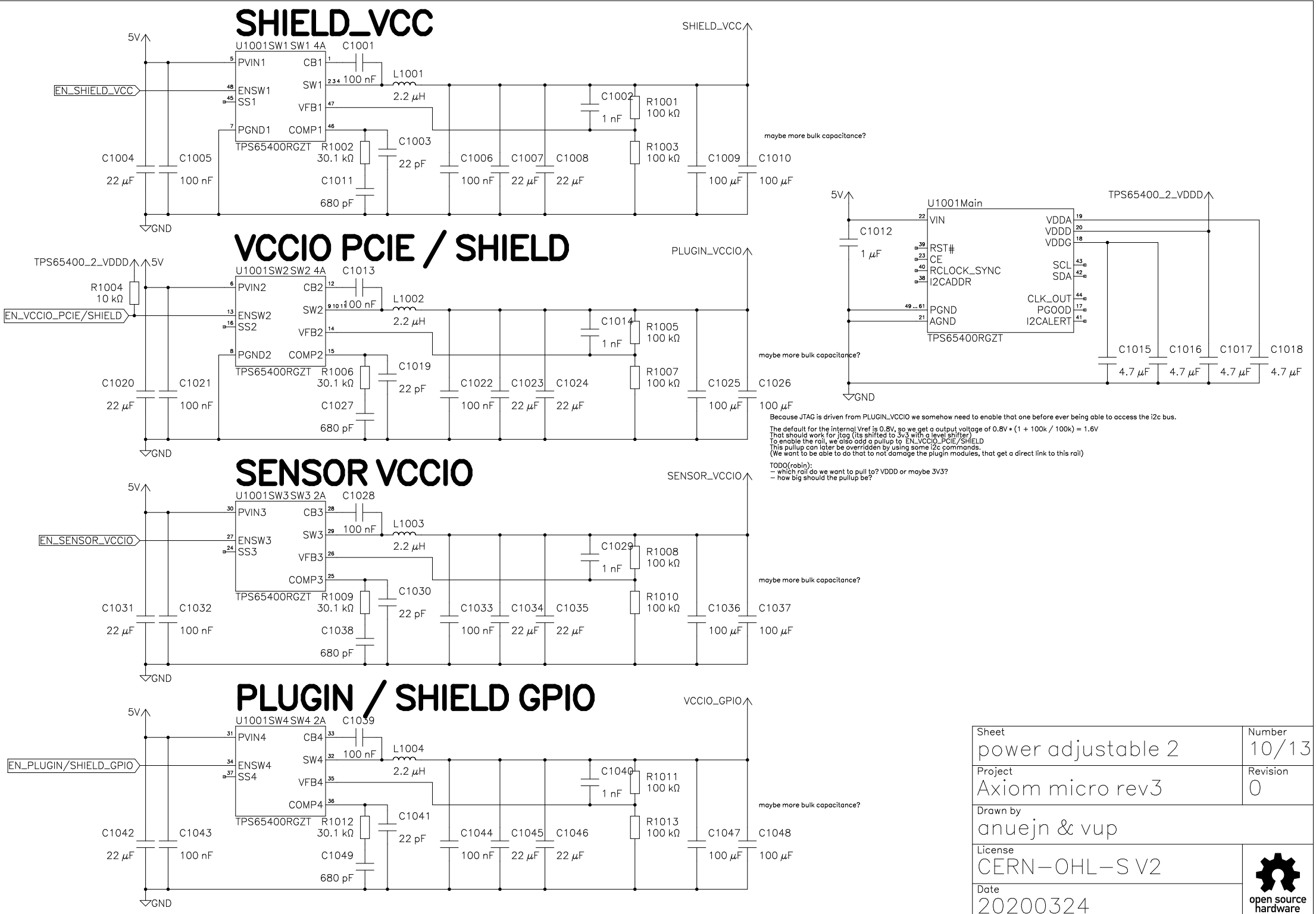

Sheet: power adjustable 2	Number: 10/13
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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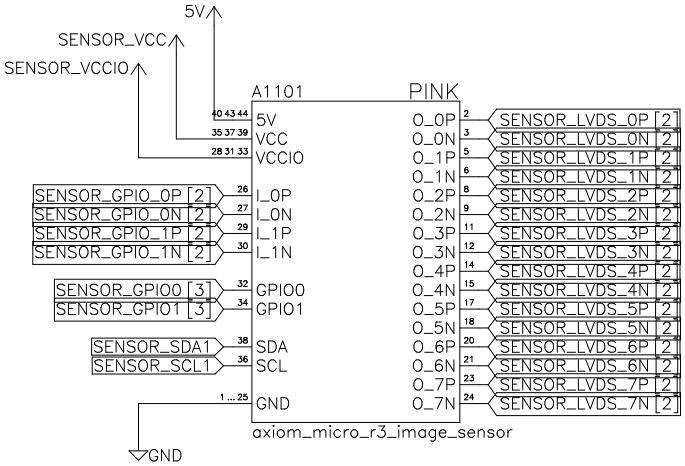
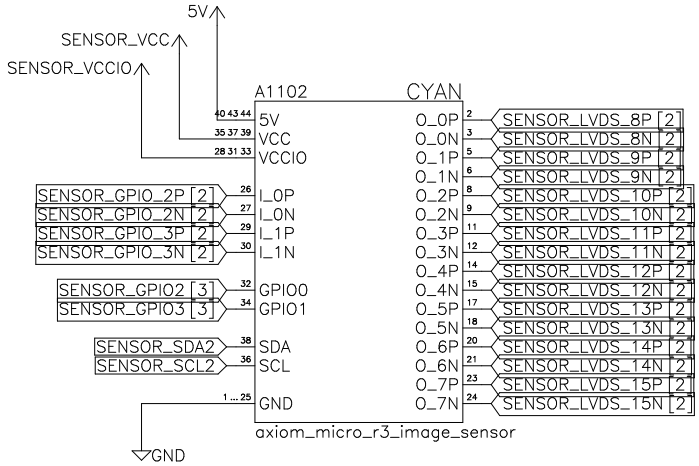
open source hardware





Bulk capacitance for sensor? (O(100uF))

Sheet: image_sensor	Number: 11/13
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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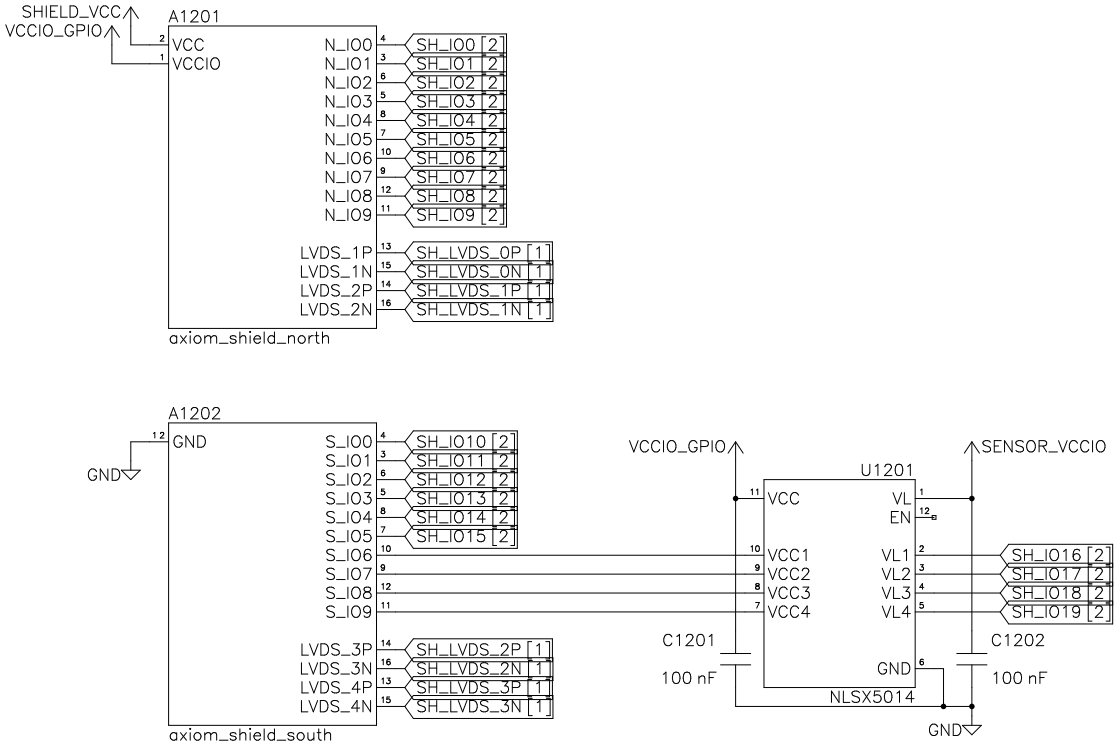

Sheet: shield	Number: 12/13
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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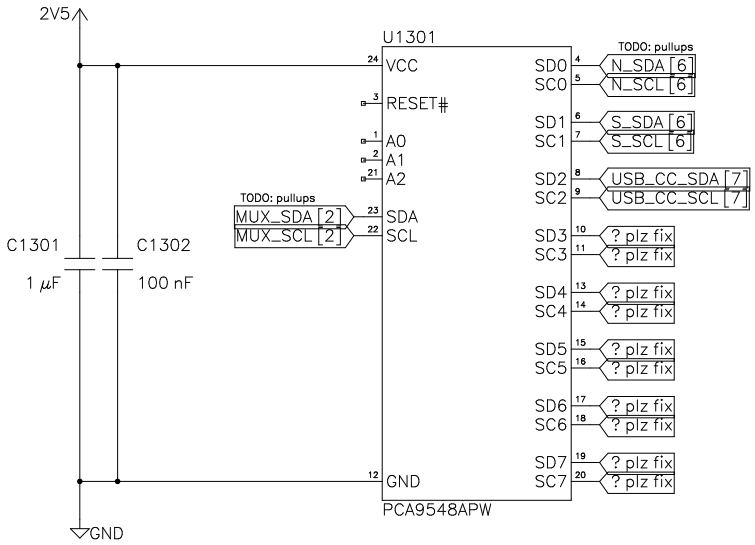
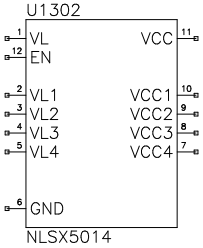
Date: 20200324	

2V5 VCC means about 1V8 voltage clamping by the pass through transistors
That sholud work for most applications, we just need to be careful with nothing with 1V2 is on the bus





Stuff we want to hang of the i2c mux:
plugin modules
pmic
probably gpio expander for power stuff
????

Sheet: misc	Number: 13/13
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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