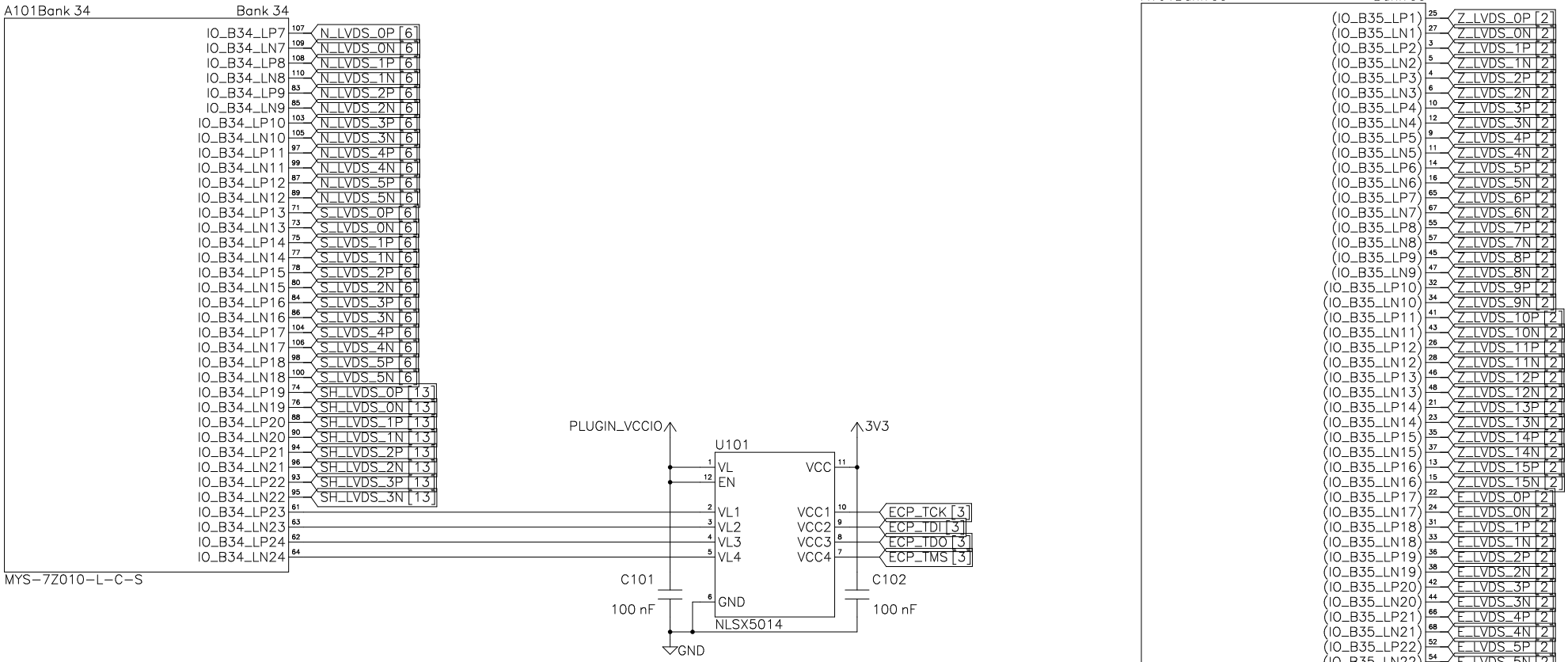
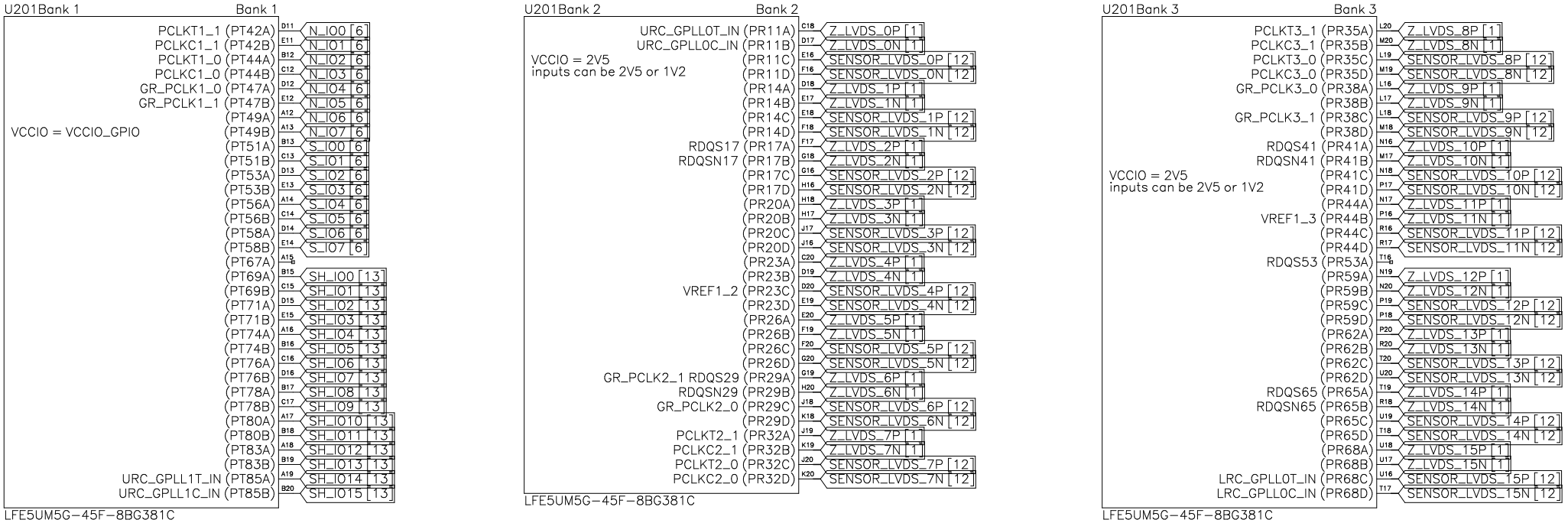
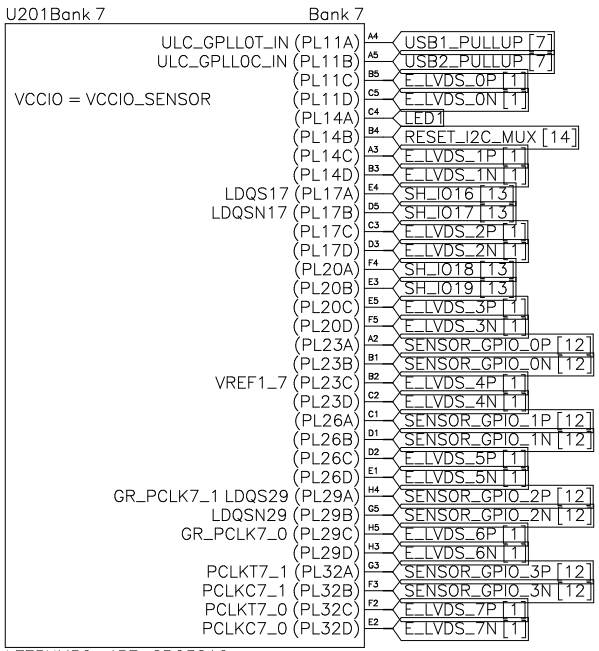
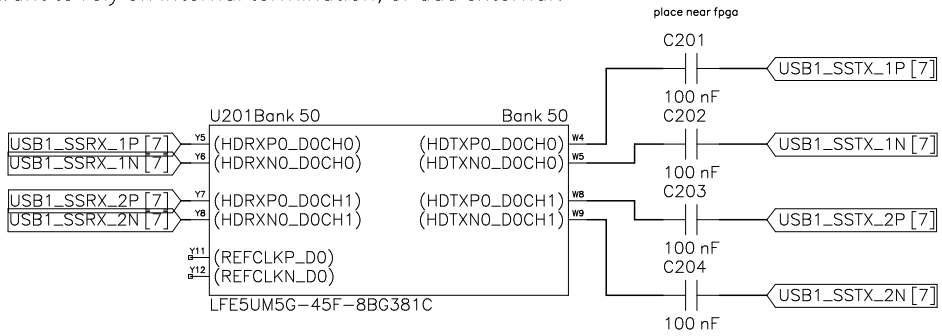


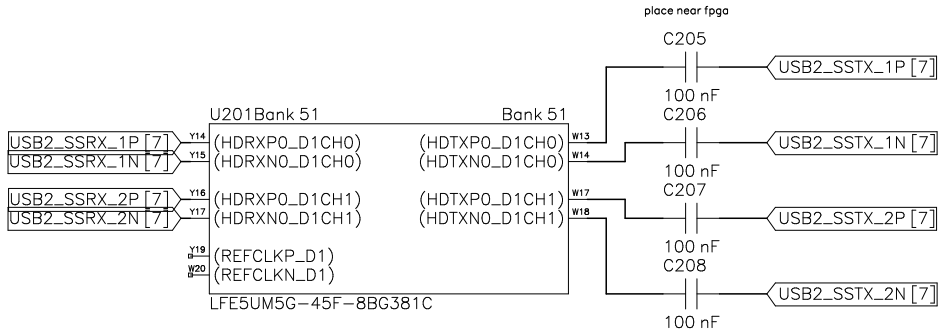

| | |
|---|---|
| Sheet: zturn lite | Number: 1/14 |
| Project: Axiom micro rev3 | Revision: 0 |
| Drawn by: anuejn & vup | |
| License: CERN-OHL-S V2 | |
| Date: 20200324 | open source hardware |




Do we want to rely on internal termination, or add external?

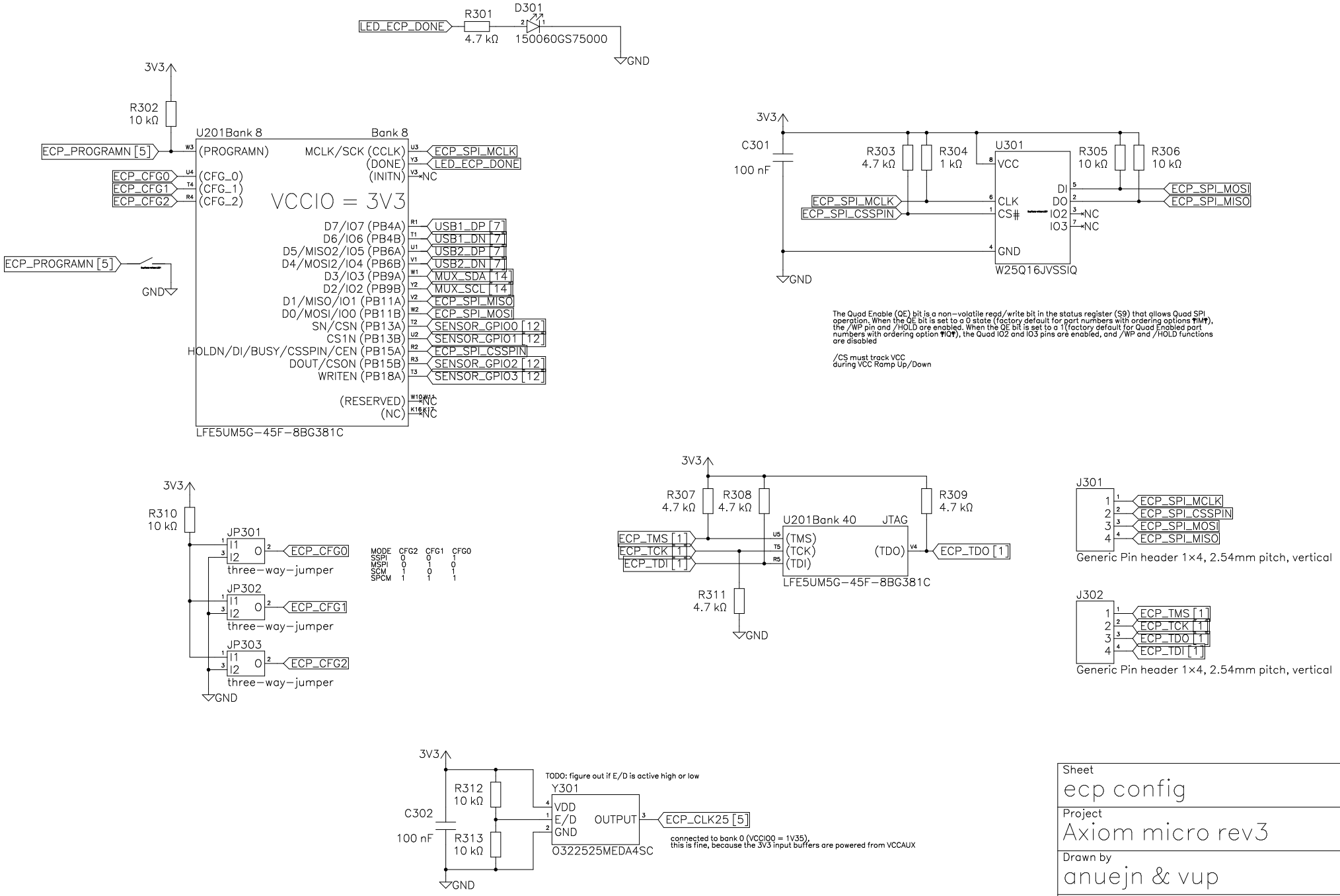



Z_LVDS goes from ECP to ZYNQ
E_LVDS goes from ZYNQ to ECP
SENSOR_LVDS goes from sensor board to ECP

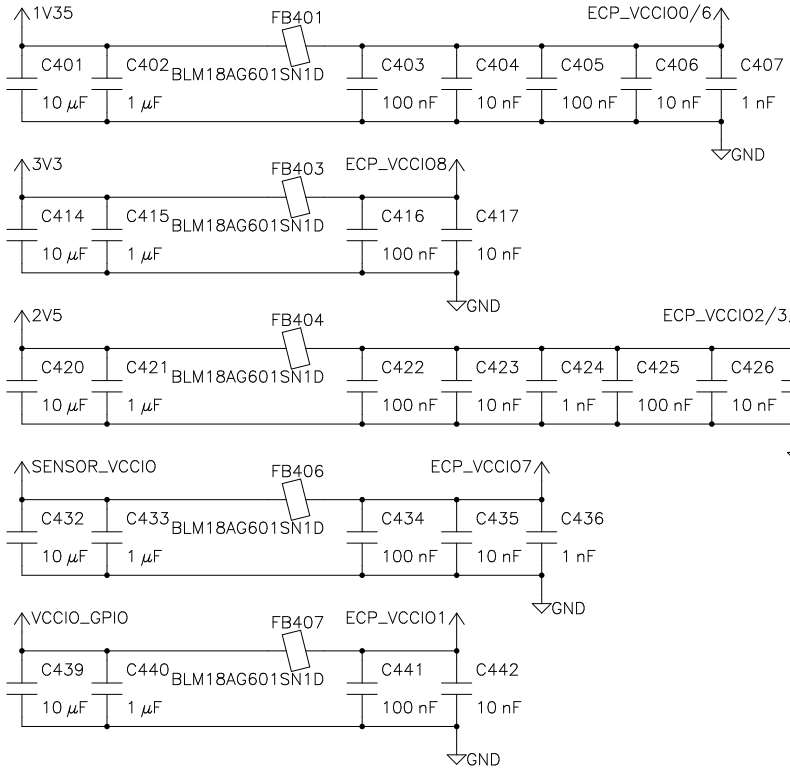
| | |
|---|---|
| Sheet: ecp | Number: 2/14 |
| Project: Axiom micro rev3 | Revision: 0 |
| Drawn by: anuejn & vup | |
| License: CERN-OHL-S V2 | |
| Date: 20200324 | open source hardware |

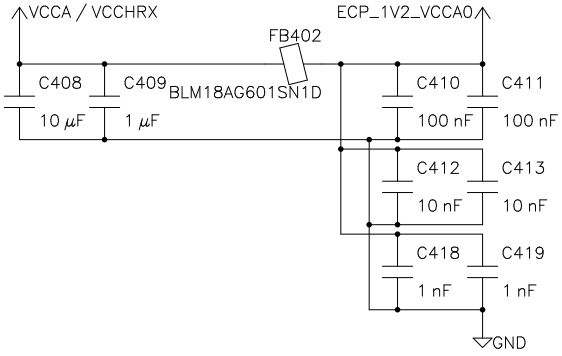


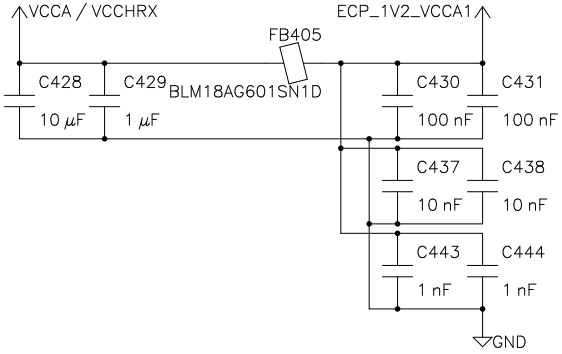

| | |
|---|---|
| Sheet: ecp config | Number: 3/14 |
| Project: Axiom micro rev3 | Revision: 0 |
| Drawn by: anuejn & vup | |
| License: CERN-OHL-S V2 | |
| Date: 20200324 | |

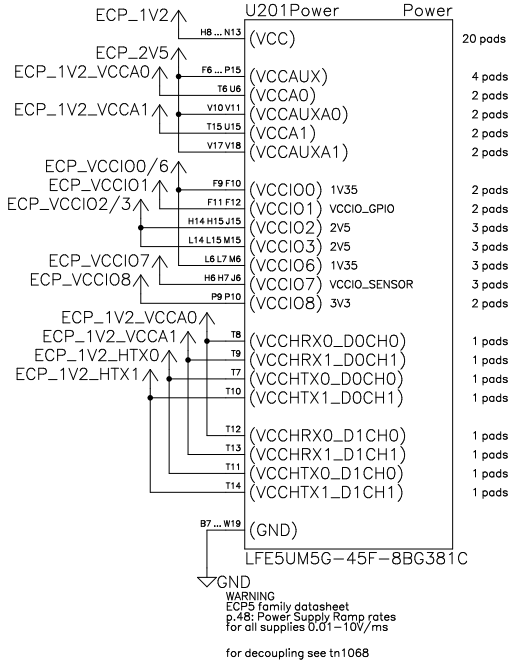
open source hardware

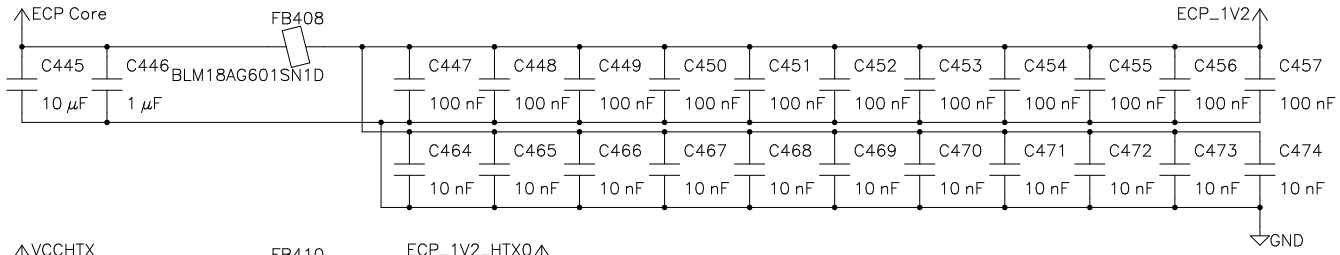
Place decoupling near FPGA, alternate 100n and 10n per pad per rail

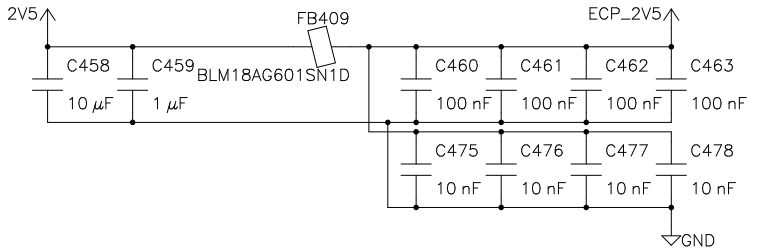


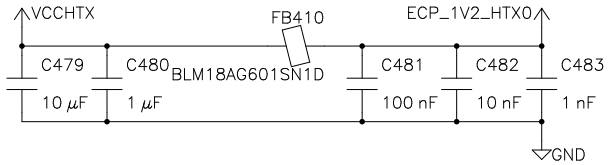



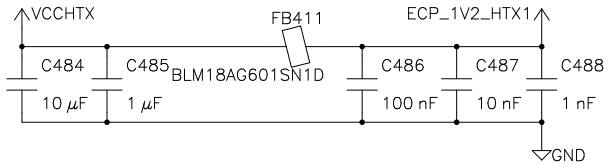



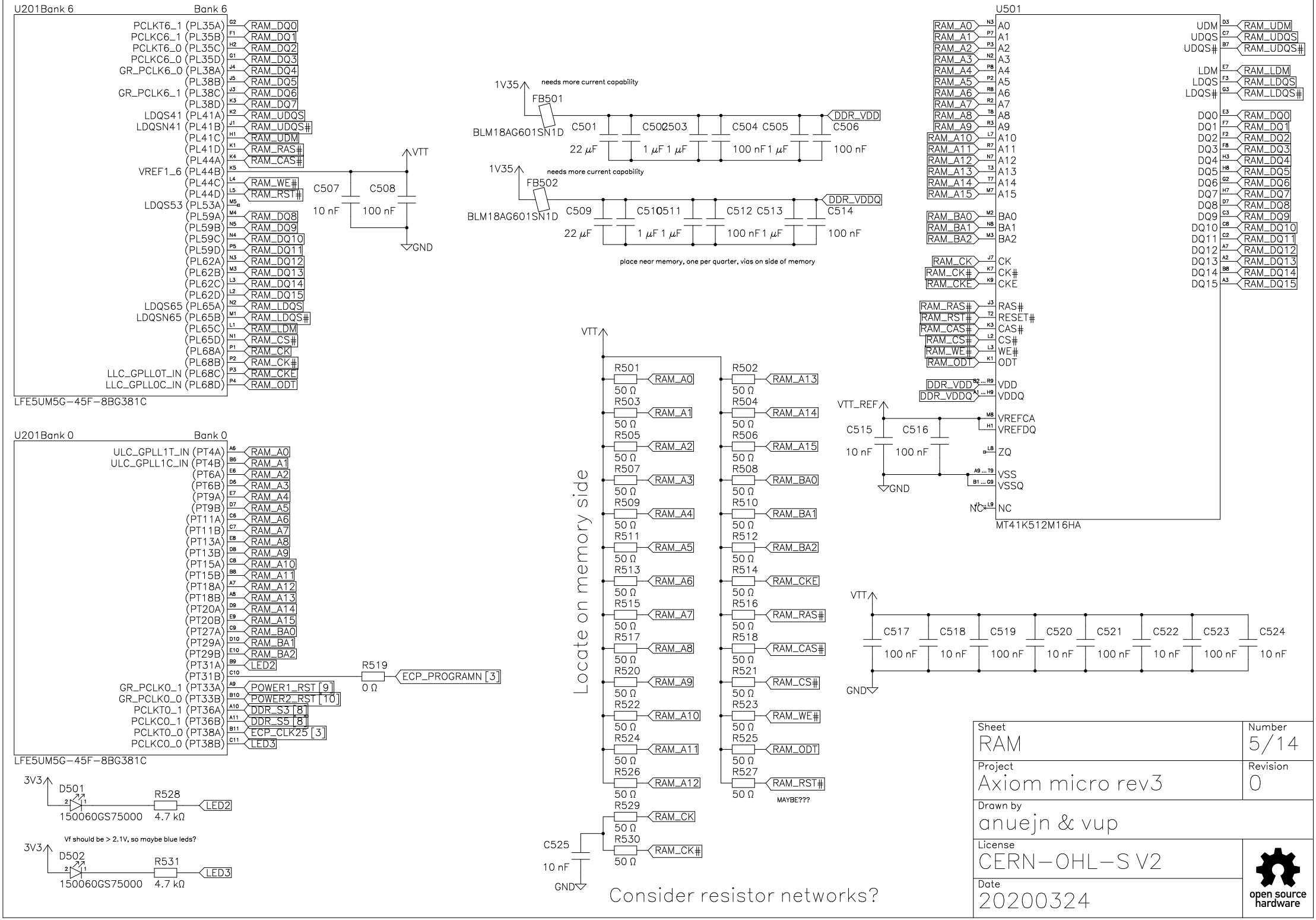



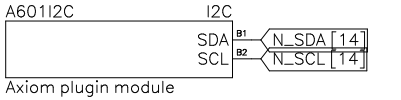



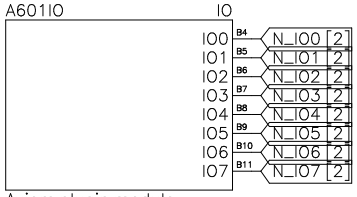

| | |
|---|---|
| Sheet: ecp power | Number: 4/14 |
| Project: Axiom micro rev3 | Revision: 0 |
| Drawn by: anuejn & vup | |
| License: CERN-OHL-S V2 | open source hardware |
| Date: 20200324 | |


U201Bank 6
Bank 6
PCLKT6_1 (PL35A)
PCLKC6_1 (PL35B)
PCLKT6_0 (PL35C)
PCLKC6_0 (PL35D)
GR_PCLK6_0 (PL38A)
(PL38B)
GR_PCLK6_1 (PL38C)
(PL38D)
LDQS41 (PL41A)
LDQSN41 (PL41B)
(PL41C)
(PL41D)
(PL44A)
VREF1_6 (PL44B)
(PL44C)
(PL44D)
LDQS53 (PL53A)
(PL59A)
(PL59B)
(PL59C)
(PL59D)
(PL62A)
(PL62B)
(PL62C)
(PL62D)
LDQS65 (PL65A)
LDQSN65 (PL65B)
(PL65C)
(PL65D)
(PL68A)
(PL68B)
LLC_GPLL0T_IN (PL68C)
LLC_GPLL0C_IN (PL68D)
RAM_DQ0
RAM_DQ1
RAM_DQ2
RAM_DQ3
RAM_DQ4
RAM_DQ5
RAM_DQ6
RAM_DQ7
RAM_UDQS
RAM_UDQS#
RAM_UDM
RAM_RAS#
RAM_CAS#
RAM_WE#
RAM_RST#
RAM_DQ8
RAM_DQ9
RAM_DQ10
RAM_DQ11
RAM_DQ12
RAM_DQ13
RAM_DQ14
RAM_DQ15
RAM_LDQS
RAM_LDQS#
RAM_LDM
RAM_CS#
RAM_CK
RAM_CK#
RAM_CKE
RAM_ODT
VTT
C507
10 nF
C508
100 nF
GND
LFE5UM5G−45F−8BG381C
1V35
needs more current capability
FB501
BLM18AG601SN1D
C501
22 µF
C502
C503
1 µF
1 µF
C504
C505
100 nF
1 µF
C506
100 nF
DDR_VDD
1V35
needs more current capability
FB502
BLM18AG601SN1D
C509
22 µF
C510
C511
1 µF
1 µF
C512
C513
100 nF
1 µF
C514
100 nF
DDR_VDDQ
place near memory, one per quarter, vias on side of memory
U501
RAM_A0
RAM_A1
RAM_A2
RAM_A3
RAM_A4
RAM_A5
RAM_A6
RAM_A7
RAM_A8
RAM_A9
RAM_A10
RAM_A11
RAM_A12
RAM_A13
RAM_A14
RAM_A15
RAM_BA0
RAM_BA1
RAM_BA2
RAM_CK
RAM_CK#
RAM_CKE
RAM_RAS#
RAM_RST#
RAM_CAS#
RAM_CS#
RAM_WE#
RAM_ODT
DDR_VDD
DDR_VDDQ
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
BA0
BA1
BA2
CK
CK#
CKE
RAS#
RESET#
CAS#
CS#
WE#
ODT
VDD
VDDQ
VREFCA
VREFDQ
ZQ
VSS
VSSQ
NC
UDM
UDQS
UDQS#
LDM
LDQS
LDQS#
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
RAM_UDM
RAM_UDQS
RAM_UDQS#
RAM_LDM
RAM_LDQS
RAM_LDQS#
RAM_DQ0
RAM_DQ1
RAM_DQ2
RAM_DQ3
RAM_DQ4
RAM_DQ5
RAM_DQ6
RAM_DQ7
RAM_DQ8
RAM_DQ9
RAM_DQ10
RAM_DQ11
RAM_DQ12
RAM_DQ13
RAM_DQ14
RAM_DQ15
MT41K512M16HA
VTT_REF
C515
10 nF
C516
100 nF
GND
U201Bank 0
Bank 0
ULC_GPLL1T_IN (PT4A)
ULC_GPLL1C_IN (PT4B)
(PT6A)
(PT6B)
(PT9A)
(PT9B)
(PT11A)
(PT11B)
(PT13A)
(PT13B)
(PT15A)
(PT15B)
(PT18A)
(PT18B)
(PT20A)
(PT20B)
(PT27A)
(PT29A)
(PT29B)
(PT31A)
(PT31B)
GR_PCLK0_1 (PT33A)
GR_PCLK0_0 (PT33B)
PCLKT0_1 (PT36A)
PCLKC0_1 (PT36B)
PCLKT0_0 (PT38A)
PCLKC0_0 (PT38B)
RAM_A0
RAM_A1
RAM_A2
RAM_A3
RAM_A4
RAM_A5
RAM_A6
RAM_A7
RAM_A8
RAM_A9
RAM_A10
RAM_A11
RAM_A12
RAM_A13
RAM_A14
RAM_A15
RAM_BA0
RAM_BA1
RAM_BA2
LED2
R519
0 Ω
ECP_PROGRAMN [3]
POWER1_RST [9]
POWER2_RST [10]
DDR_S3 [8]
DDR_S5 [8]
ECP_CLK25 [3]
LED3
LFE5UM5G−45F−8BG381C
3V3
D501
150060GS75000
R528
4.7 kΩ
LED2
Vf should be > 2.1V, so maybe blue leds?
3V3
D502
150060GS75000
R531
4.7 kΩ
LED3
Locate on memory side
VTT
R501
50 Ω
RAM_A0
R502
50 Ω
RAM_A13
R503
50 Ω
RAM_A1
R504
50 Ω
RAM_A14
R505
50 Ω
RAM_A2
R506
50 Ω
RAM_A15
R507
50 Ω
RAM_A3
R508
50 Ω
RAM_BA0
R509
50 Ω
RAM_A4
R510
50 Ω
RAM_BA1
R511
50 Ω
RAM_A5
R512
50 Ω
RAM_BA2
R513
50 Ω
RAM_A6
R514
50 Ω
RAM_CKE
R515
50 Ω
RAM_A7
R516
50 Ω
RAM_RAS#
R517
50 Ω
RAM_A8
R518
50 Ω
RAM_CAS#
R520
50 Ω
RAM_A9
R521
50 Ω
RAM_CS#
R522
50 Ω
RAM_A10
R523
50 Ω
RAM_WE#
R524
50 Ω
RAM_A11
R525
50 Ω
RAM_ODT
R526
50 Ω
RAM_A12
R527
50 Ω
RAM_RST#
MAYBE???
R529
50 Ω
RAM_CK
R530
50 Ω
RAM_CK#
C525
10 nF
GND
Consider resistor networks?
VTT
C517
100 nF
C518
10 nF
C519
100 nF
C520
10 nF
C521
100 nF
C522
10 nF
C523
100 nF
C524
10 nF
GND
Sheet
RAM
Number
5/14
Project
Axiom micro rev3
Revision
0
Drawn by
anuejn & vup
License
CERN−OHL−S V2
Date
20200324
open source hardware

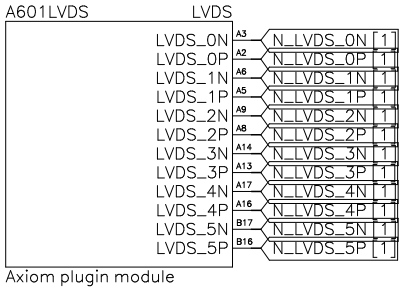
## plugin north



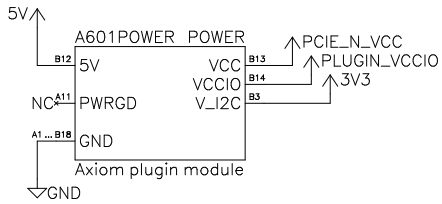

Axiom plugin module



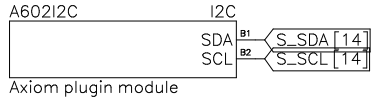

Axiom plugin module



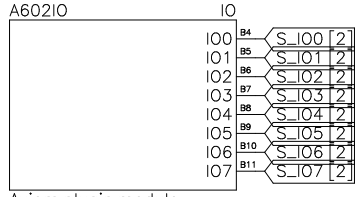

Axiom plugin module



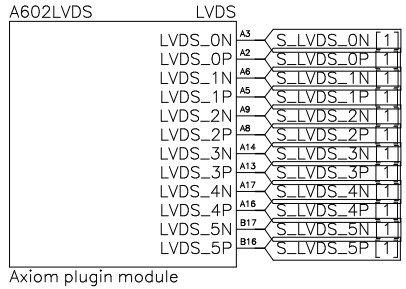

## plugin south



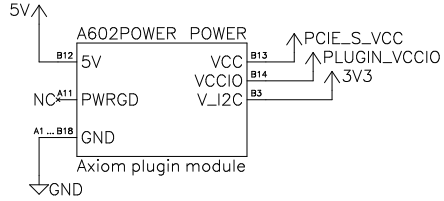

Axiom plugin module



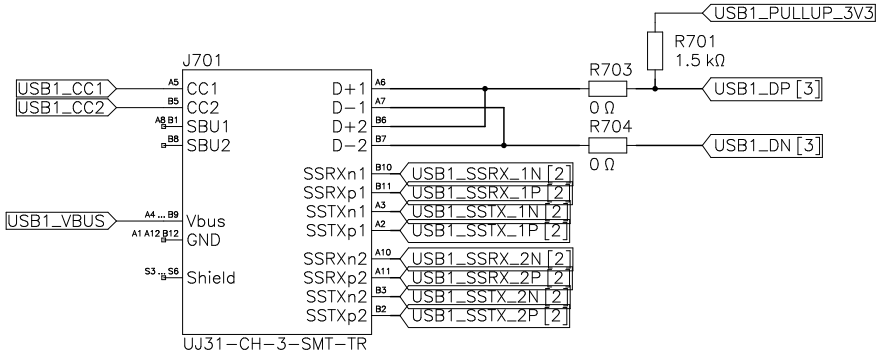

Axiom plugin module

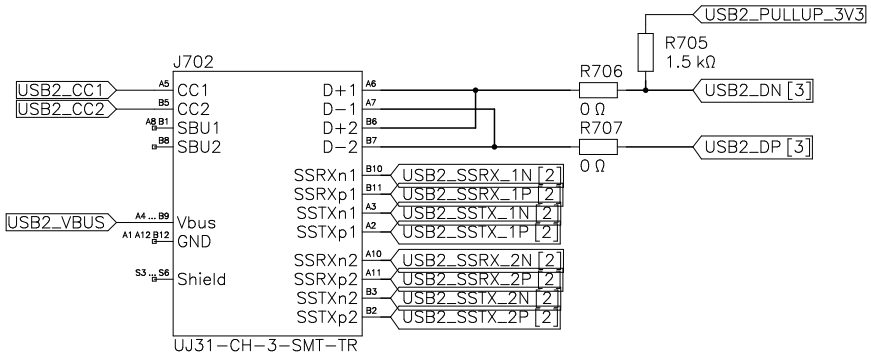


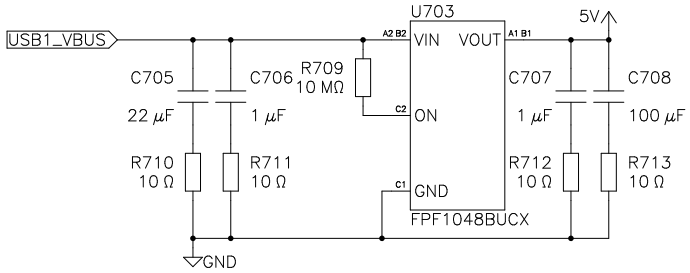

Axiom plugin module

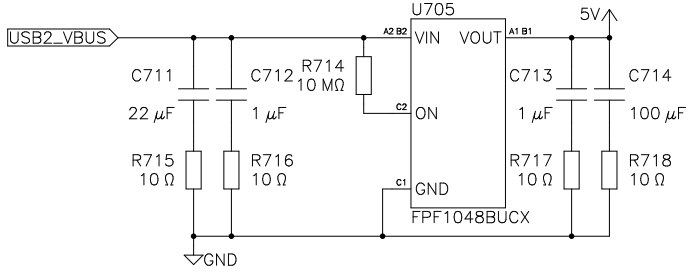


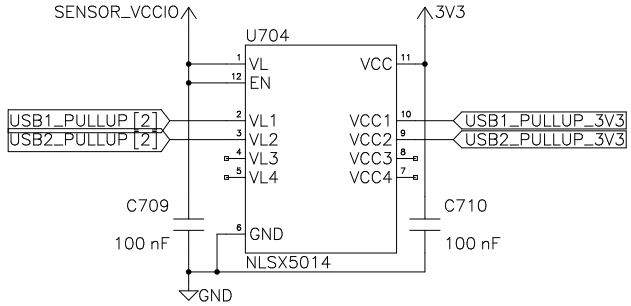

| | |
|---|---|
| Sheet<br>plugin | Number<br>6/14 |
| Project<br>Axiom micro rev3 | Revision<br>0 |
| Drawn by<br>anuejn & vup | |
| License<br>CERN-OHL-S V2 | open source hardware |
| Date<br>20200324 | |

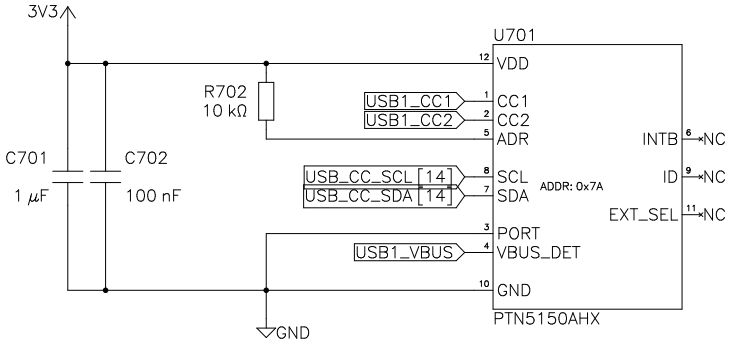


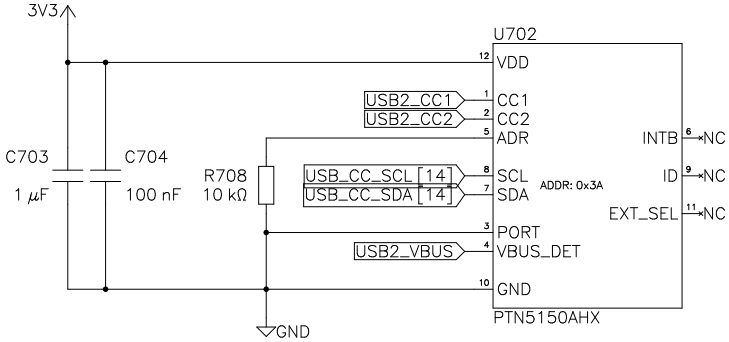



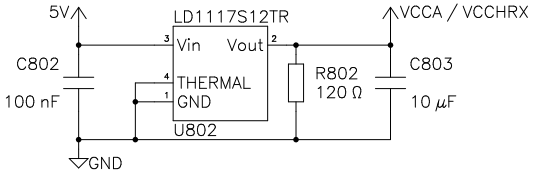



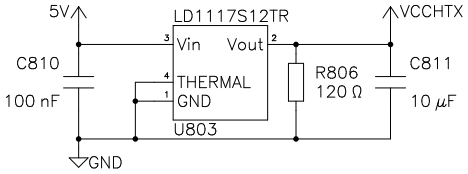

PORT= VDD: DFP mode ($R_D$ = 80uA power default for non−I2C mode).
PORT = Mid (or floating): DRP mode
PORT=GND: UFP mode

Trinary GPIO Input ADR pin run from VDD
– ADR pull up to VDD with 10 kΩ resistor (I2C Enabled with ADDR bit 6 equal to 1, I2C Address 0x7A)
– ADR pull down to GND with 10 kΩ resistor. (I2C Enabled with ADDR bit 6 equal to 0, I2C Address 0x3A)
– ADR = Mid or floating (Pin 6/7/8) configured as OUT1/2/3 in non−I2C mode

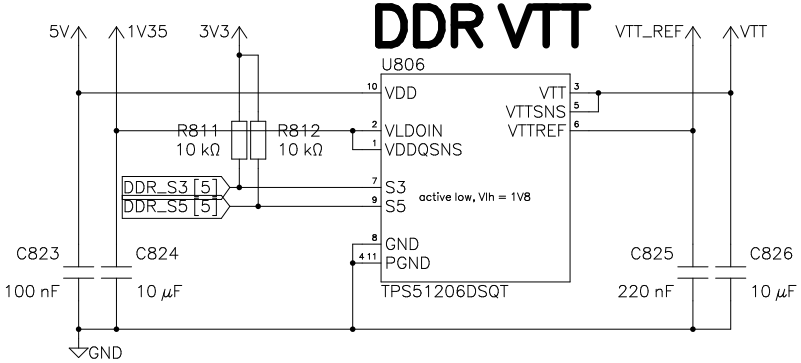
| | |
|---|---|
| Sheet: USB | Number: 7/14 |
| Project: Axiom micro rev3 | Revision: 0 |
| Drawn by: anuejn & vup | |
| License: CERN−OHL−S V2 | |
| Date: 20200324 | open source hardware |



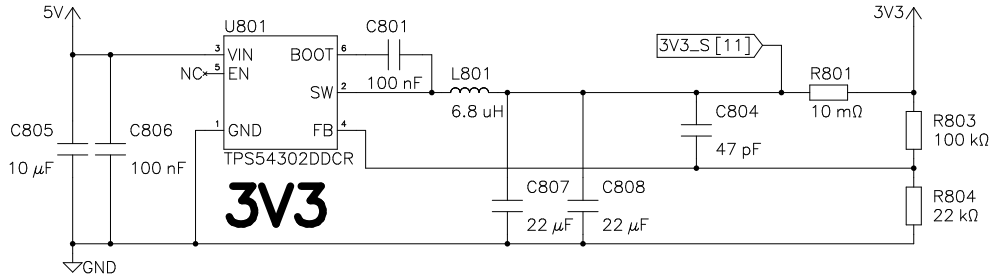

# 1V2 VCCA / VCCHRX

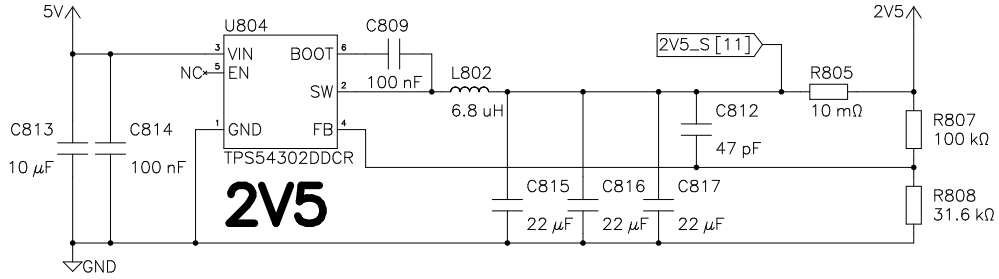


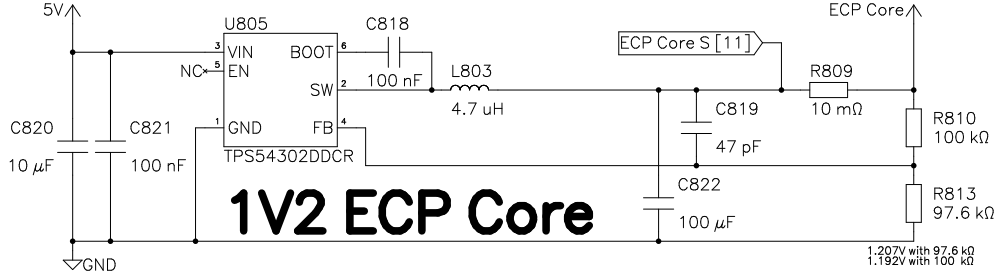

# 1V2 VCCHTX




positive terminal of the VTT pin output capacitor(s) as a separate trace from the high–current path from VTT. Consider adding a low–pass R–C filter at the VTTSNS pin in case the ESR of the VTT output capacitor(s) is larger than 2 mΩ. The R–C filter time constant should be approximately the same or slightly lower than the time constant of the VTT output capacitance and ESR.




| | |
|---|---|
| Sheet: power fixed | Number: 8/14 |
| Project: Axiom micro rev3 | Revision: 0 |
| Drawn by: anuejn & vup | |
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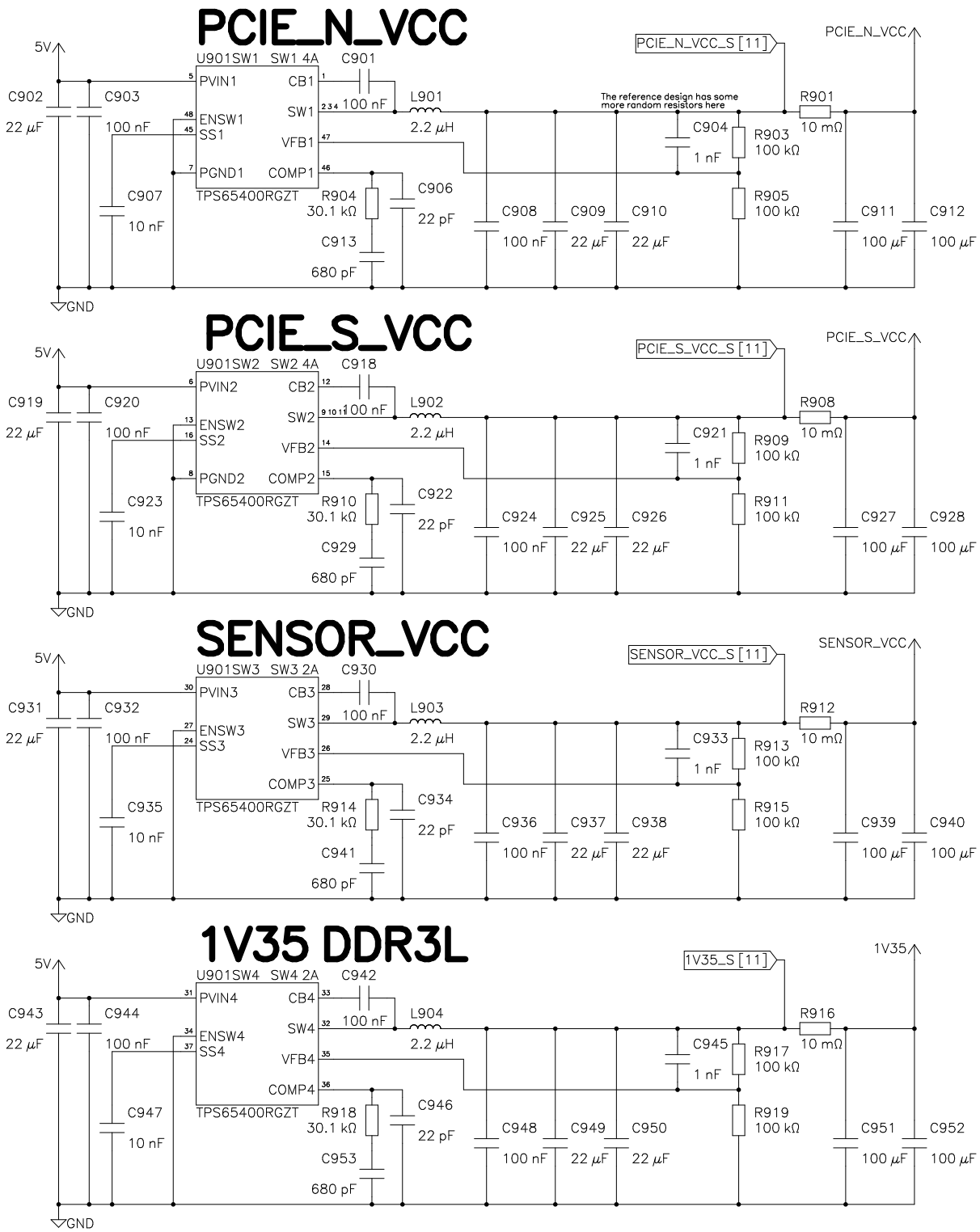
PCIE_N_VCC
5V
U901SW1 SW1 4A
PVIN1
ENSW1
SS1
PGND1
CB1
SW1
VFB1
COMP1
TPS65400RGZT
C901
100 nF
L901
2.2 µH
PCIE_N_VCC_S [11]
PCIE_N_VCC
The reference design has some more random resistors here
R901
10 mΩ
C902
22 µF
C903
100 nF
C904
1 nF
R903
100 kΩ
R905
100 kΩ
C907
10 nF
R904
30.1 kΩ
C906
22 pF
C913
680 pF
C908
100 nF
C909
22 µF
C910
22 µF
C911
100 µF
C912
100 µF
GND
PCIE_S_VCC
U901SW2 SW2 4A
PVIN2
ENSW2
SS2
PGND2
CB2
SW2
VFB2
COMP2
TPS65400RGZT
C918
100 nF
L902
2.2 µH
PCIE_S_VCC_S [11]
PCIE_S_VCC
R908
10 mΩ
C919
22 µF
C920
100 nF
C921
1 nF
R909
100 kΩ
R911
100 kΩ
C923
10 nF
R910
30.1 kΩ
C922
22 pF
C929
680 pF
C924
100 nF
C925
22 µF
C926
22 µF
C927
100 µF
C928
100 µF
SENSOR_VCC
U901SW3 SW3 2A
PVIN3
ENSW3
SS3
CB3
SW3
VFB3
COMP3
TPS65400RGZT
C930
100 nF
L903
2.2 µH
SENSOR_VCC_S [11]
SENSOR_VCC
R912
10 mΩ
C931
22 µF
C932
100 nF
C933
1 nF
R913
100 kΩ
R915
100 kΩ
C935
10 nF
R914
30.1 kΩ
C934
22 pF
C941
680 pF
C936
100 nF
C937
22 µF
C938
22 µF
C939
100 µF
C940
100 µF
1V35 DDR3L
U901SW4 SW4 2A
PVIN4
ENSW4
SS4
CB4
SW4
VFB4
COMP4
TPS65400RGZT
C942
100 nF
L904
2.2 µH
1V35_S [11]
1V35
R916
10 mΩ
C943
22 µF
C944
100 nF
C945
1 nF
R917
100 kΩ
R919
100 kΩ
C947
10 nF
R918
30.1 kΩ
C946
22 pF
C953
680 pF
C948
100 nF
C949
22 µF
C950
22 µF
C951
100 µF
C952
100 µF
GND
this is a active low reset, so we can pull it low with a arbitrary fpga pin and pull it up with a pullup resistor, the fpga pin should be Hi-Z if we are not pulling reset low
POWER1_RST [5]
R902
10 kΩ
5V
U901Main
VIN
RST#
CE has internal pullup
RCLOCK_SYNC
I2CADDR
PGND
AGND
VDDA
VDDD
VDDG
SCL
SDA
ADDR: 0x6A
CLK_OUT
PGOOD
I2CALERT
TPS65400RGZT
POWER_SCL [10,14]
POWER_SDA [10,14]
C905
1 µF
R906
22 kΩ
R907
82.5 kΩ
Fsw ~ 2MHz
C914
4.7 µF
C915
4.7 µF
C916
4.7 µF
C917
4.7 µF
GND
all rails apart from the one use for jtag are disabled by default (as we need to setup the voltages on the first start)
soft start caps: 10nF / 5uA * 0.8V = 1.6ms
for ECP: max 10V/ms slew rate
TODO:
– more bulk capacitance?
(for 1V2 the reference schematic has 470uF additionally)
– soft start capacitors
– current limiting resistor for feed forward capacitor
– think about the compensation netwok
– If the input supply is located more than a few inches from the TPS65400 converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An
electrolytic capacitor with a value of 47 µF is a typical choice.
Sheet
power adjustable 1
Number
9/14
Project
Axiom micro rev3
Revision
0
Drawn by
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License
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Date
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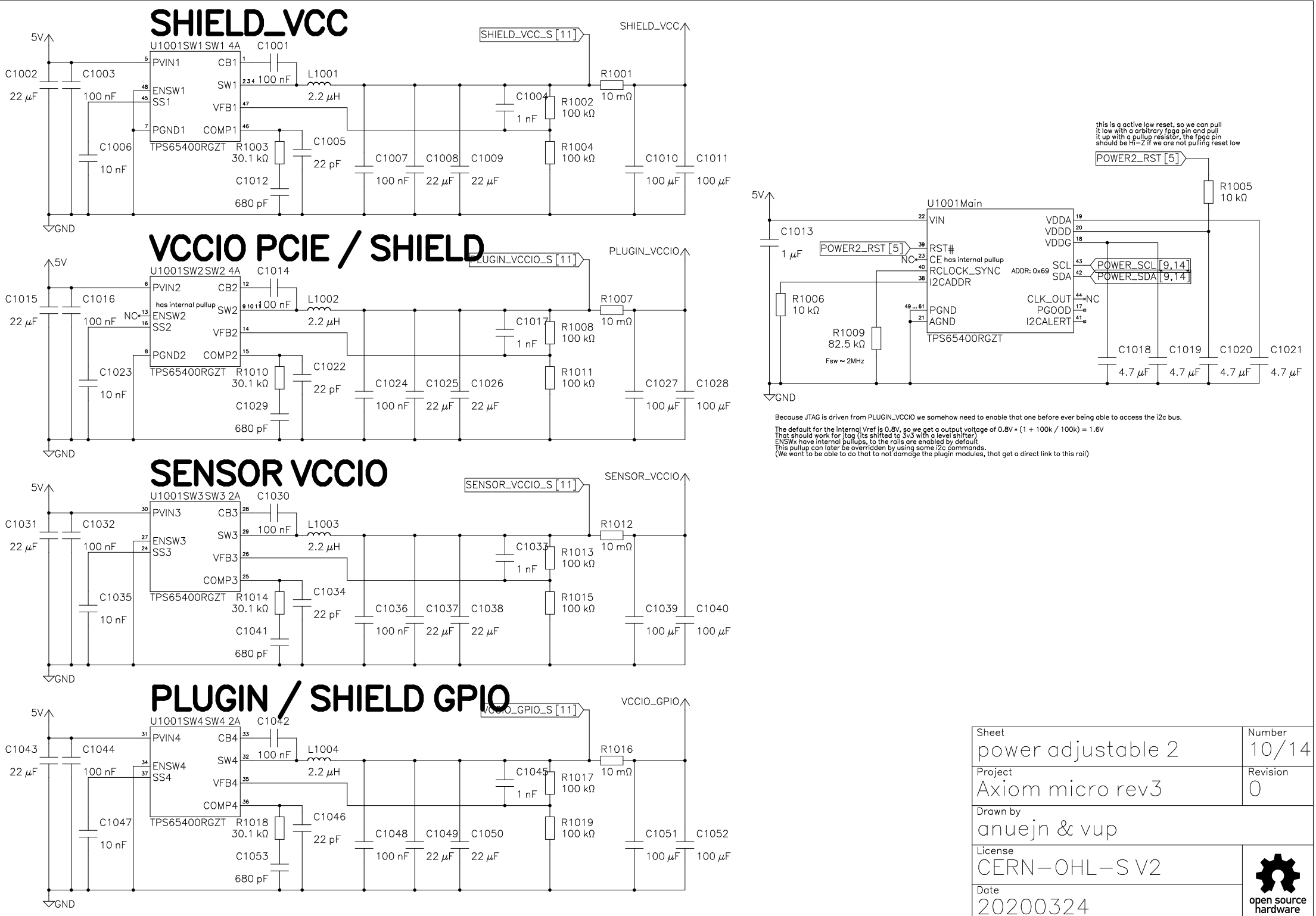
SHIELD_VCC
5V
U1001SW1 SW1 4A
PVIN1
CB1
SW1
ENSW1
SS1
VFB1
PGND1
COMP1
TPS65400RGZT
C1001
100 nF
L1001
2.2 µH
C1002
22 µF
C1003
100 nF
C1006
10 nF
R1003
30.1 kΩ
C1005
22 pF
C1012
680 pF
C1004
1 nF
R1002
100 kΩ
R1004
100 kΩ
R1001
10 mΩ
C1007
100 nF
C1008
22 µF
C1009
22 µF
C1010
100 µF
C1011
100 µF
SHIELD_VCC_S [11]
SHIELD_VCC
GND
VCCIO PCIE / SHIELD
U1001SW2 SW2 4A
PVIN2
CB2
SW2
ENSW2
SS2
VFB2
PGND2
COMP2
has internal pullup
NC
TPS65400RGZT
C1014
100 nF
L1002
2.2 µH
C1015
22 µF
C1016
100 nF
C1023
10 nF
R1010
30.1 kΩ
C1022
22 pF
C1029
680 pF
C1017
1 nF
R1008
100 kΩ
R1011
100 kΩ
R1007
10 mΩ
C1024
100 nF
C1025
22 µF
C1026
22 µF
C1027
100 µF
C1028
100 µF
PLUGIN_VCCIO_S [11]
PLUGIN_VCCIO
SENSOR_VCCIO
U1001SW3 SW3 2A
PVIN3
CB3
SW3
ENSW3
SS3
VFB3
COMP3
TPS65400RGZT
C1030
100 nF
L1003
2.2 µH
C1031
22 µF
C1032
100 nF
C1035
10 nF
R1014
30.1 kΩ
C1034
22 pF
C1041
680 pF
C1033
1 nF
R1013
100 kΩ
R1015
100 kΩ
R1012
10 mΩ
C1036
100 nF
C1037
22 µF
C1038
22 µF
C1039
100 µF
C1040
100 µF
SENSOR_VCCIO_S [11]
SENSOR_VCCIO
PLUGIN / SHIELD GPIO
U1001SW4 SW4 2A
PVIN4
CB4
SW4
ENSW4
SS4
VFB4
COMP4
TPS65400RGZT
C1042
100 nF
L1004
2.2 µH
C1043
22 µF
C1044
100 nF
C1047
10 nF
R1018
30.1 kΩ
C1046
22 pF
C1053
680 pF
C1045
1 nF
R1017
100 kΩ
R1019
100 kΩ
R1016
10 mΩ
C1048
100 nF
C1049
22 µF
C1050
22 µF
C1051
100 µF
C1052
100 µF
VCCIO_GPIO_S [11]
VCCIO_GPIO
this is a active low reset, so we can pull it low with a arbitrary fpga pin and pull it up with a pullup resistor, the fpga pin should be Hi-Z if we are not pulling reset low
POWER2_RST [5]
R1005
10 kΩ
U1001Main
VIN
RST#
CE has internal pullup
RCLOCK_SYNC
I2CADDR
PGND
AGND
VDDA
VDDD
VDDG
SCL
SDA
ADDR: 0x69
CLK_OUT
PGOOD
I2CALERT
TPS65400RGZT
POWER_SCL [9,14]
POWER_SDA [9,14]
C1013
1 µF
R1006
10 kΩ
R1009
82.5 kΩ
Fsw ~ 2MHz
C1018
4.7 µF
C1019
4.7 µF
C1020
4.7 µF
C1021
4.7 µF
Because JTAG is driven from PLUGIN_VCCIO we somehow need to enable that one before ever being able to access the i2c bus.
The default for the internal Vref is 0.8V, so we get a output voltage of 0.8V * (1 + 100k / 100k) = 1.6V
That should work for jtag (its shifted to 3v3 with a level shifter)
ENSWx have internal pullups, to the rails are enabled by default
This pullup can later be overridden by using some i2c commands.
(We want to be able to do that to not damage the plugin modules, that get a direct link to this rail)
Sheet
power adjustable 2
Number
10/14
Project
Axiom micro rev3
Revision
0
Drawn by
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Date
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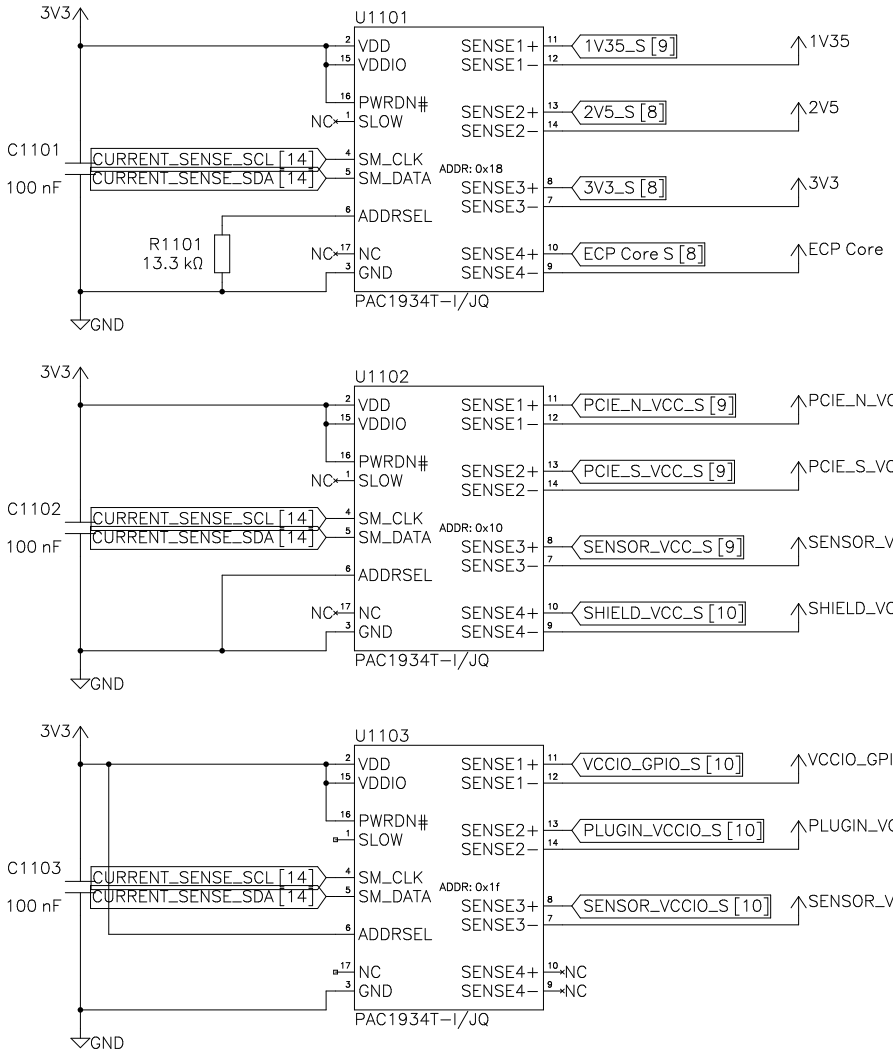
current sense resistors: 0805W8F100MT5E or CS05W8F100MT5E




| | |
|---|---|
| Sheet: current sense | Number: 11/14 |
| Project: Axiom micro rev3 | Revision: 0 |
| Drawn by: anuejn & vup | |
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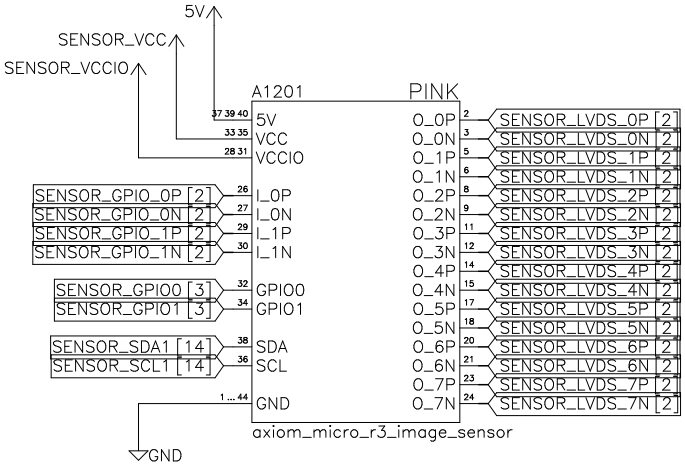
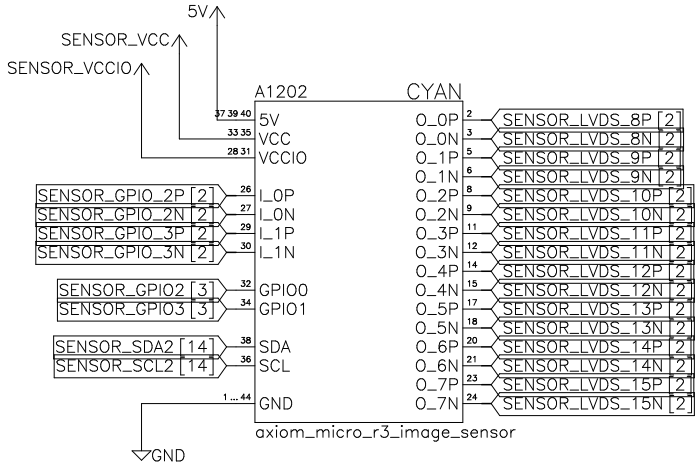
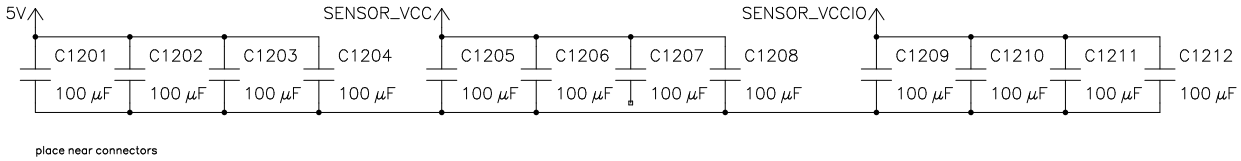
| Date: 20200324 | |




| | |
|---|---|
| Sheet: image sensor | Number: 12/14 |
| Project: Axiom micro rev3 | Revision: 0 |
| Drawn by: anuejn & vup | |
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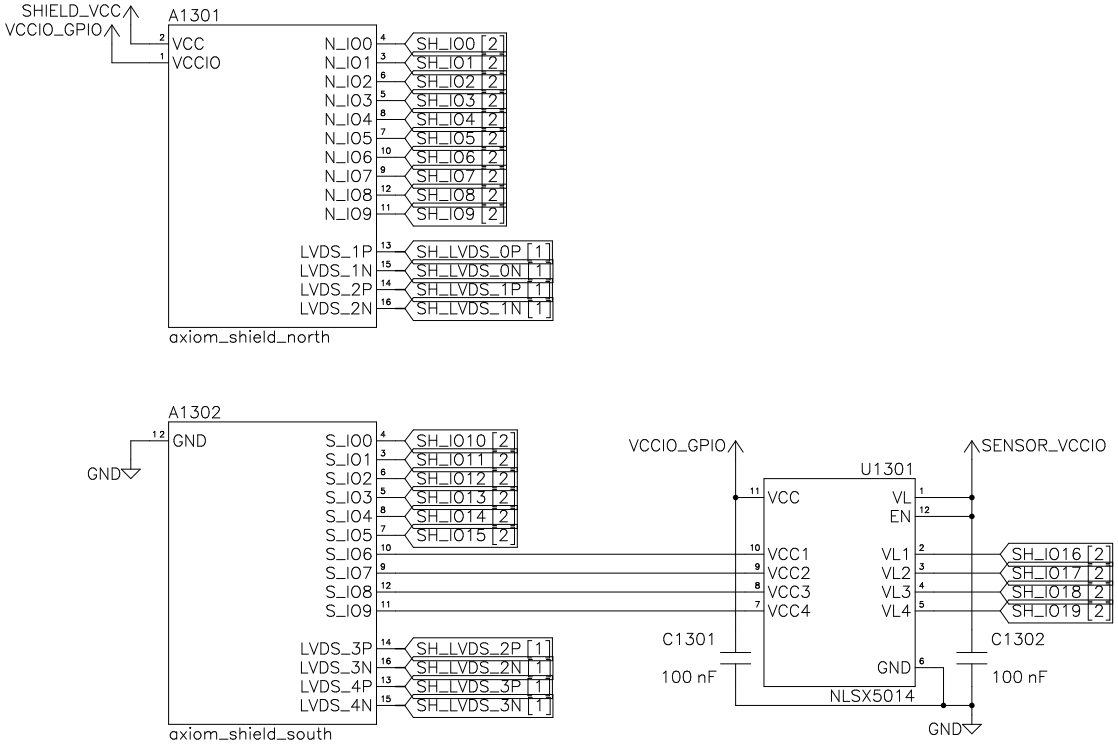
| Date: 20200324 | |




| | |
|---|---|
| Sheet: shield | Number: 13/14 |
| Project: Axiom micro rev3 | Revision: 0 |
| Drawn by: anuejn & vup | |
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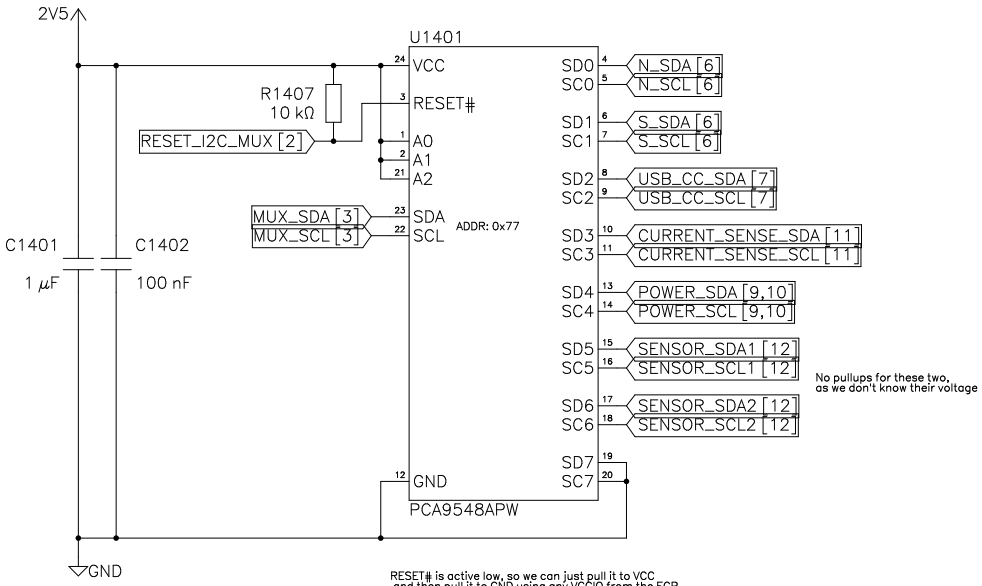
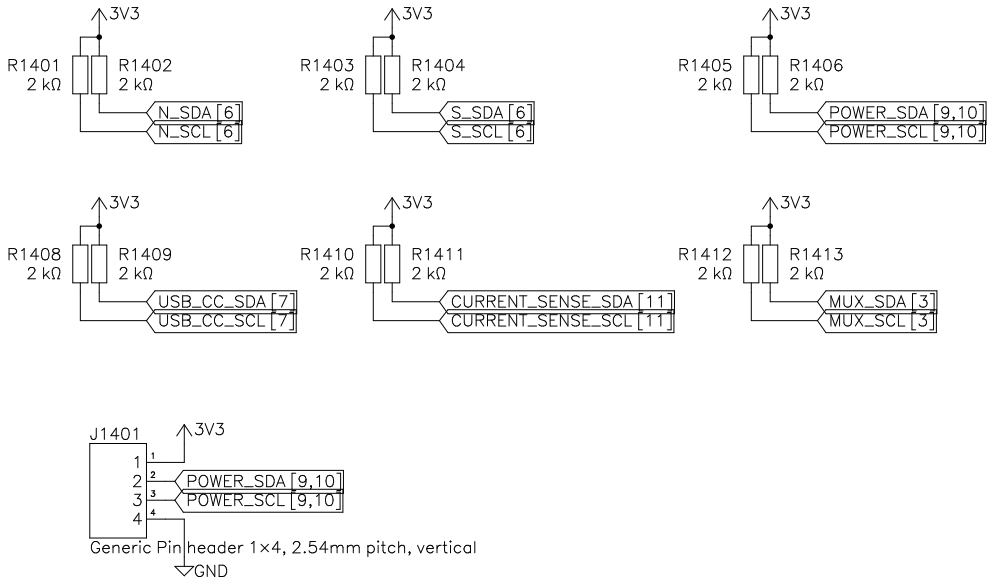
| Date: 20200324 | |




RESET# is active low, so we can just pull it to VCC
and then pull it to GND using any VCCIO from the ECP,
attention has to be paid to not make RESET# get over VCC,
as otherwise current flows from the RESET pin to the VCC pin,
this should be accomplishable by just making the fpga output Hi-Z
if it is not pullen low

2V5 VCC means about 1V8 voltage clamping by the pass through transistors
That sholud work for most applications, we just need to be careful with nothing with 1V2 is on the bus

Unused channels have to be tied to GND or VCC




| | |
|---|---|
| Sheet: i2c mux | Number: 14/14 |
| Project: Axiom micro rev3 | Revision: 0 |
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