
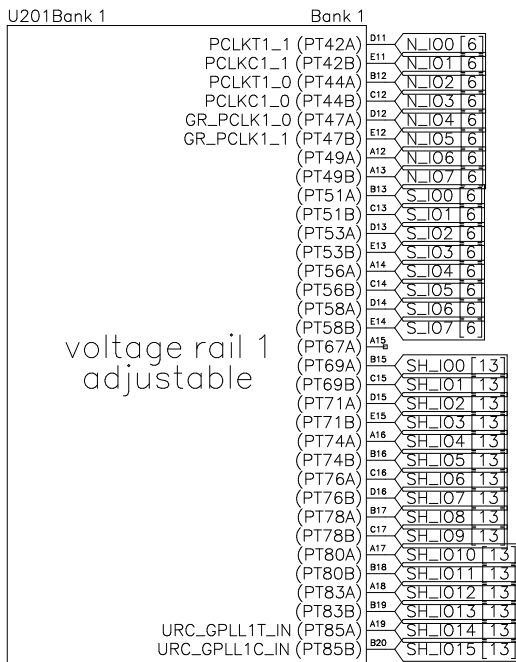
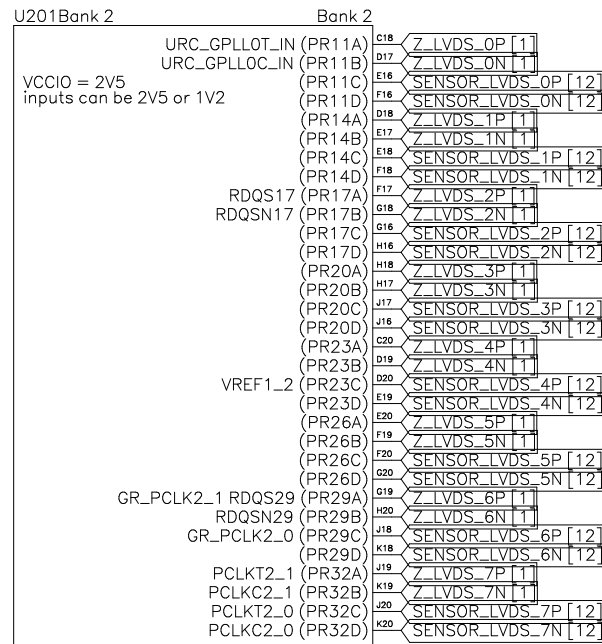


Sheet	zturn lite	Number	1/14
Project	Axiom micro rev3	Revision	0
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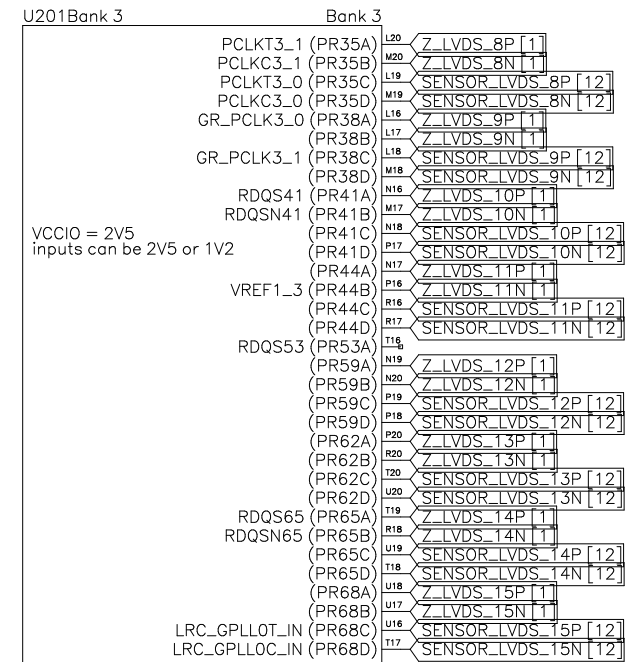


voltage rail 1
adjustable

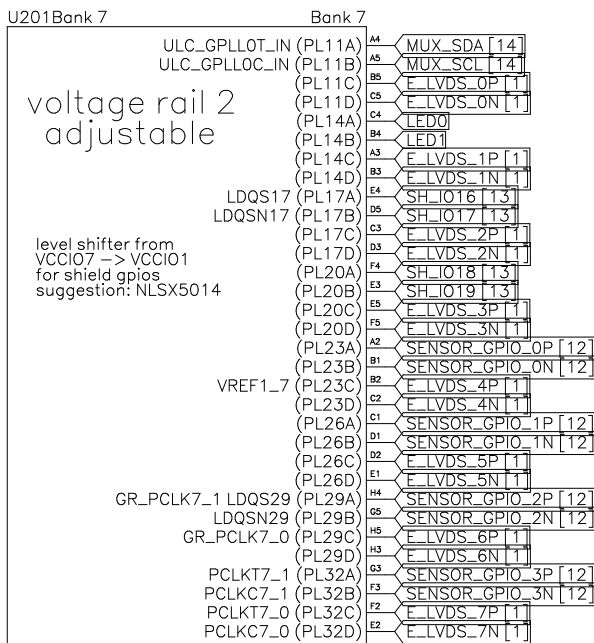
LFE5UM5G-45F-8BG381C



LFE5UM5G-45F-8BG381C



LFE5UM5G-45F-8BG381C

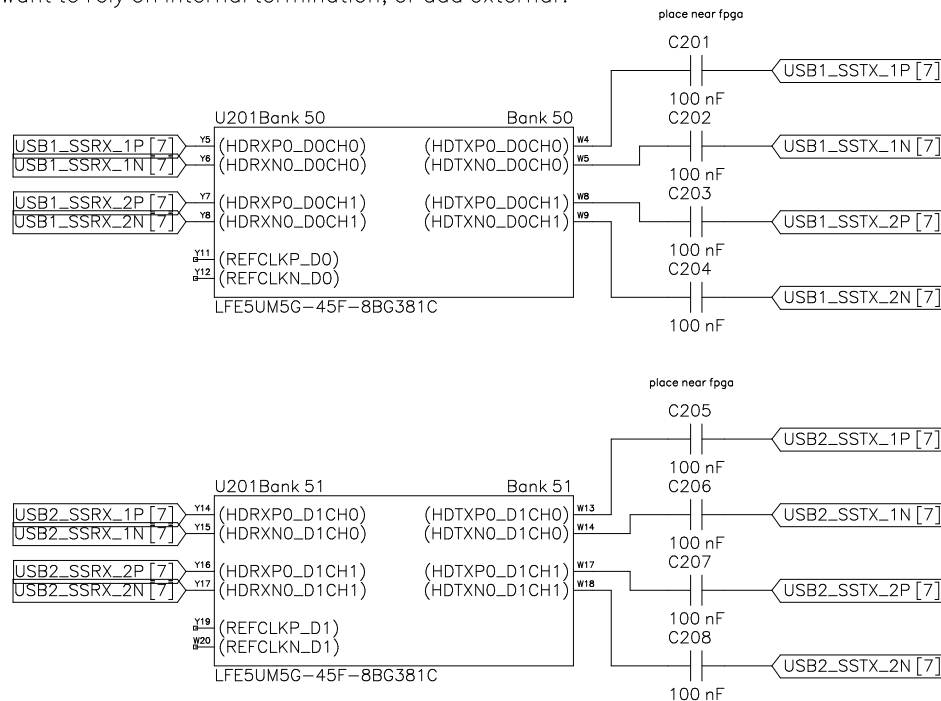


voltage rail 2
adjustable

level shifter from
VCCIO7 -> VCCIO1
for shield gpio's
suggestion: NLSX5014

LFE5UM5G-45F-8BG381C

Do we want to rely on internal termination, or add external?



Z_LVDS goes from ECP to ZYNQ
F_LVDS goes from ZYNQ to ECP
SENSOR_LVDS goes from sensor board to ECP

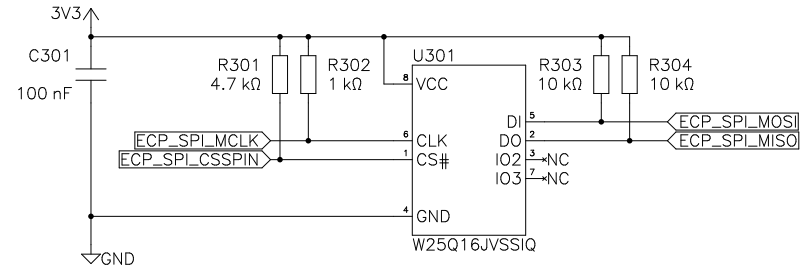
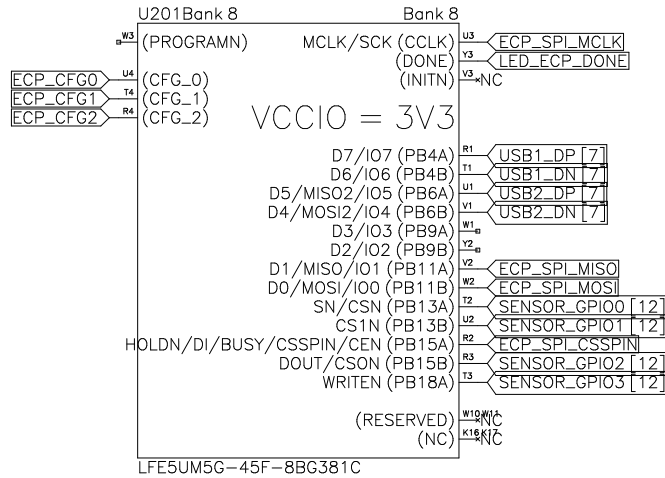
Sheet	Number
ecp	2/14
Project	Revision
Axiom micro rev3	0
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PROGRAMN

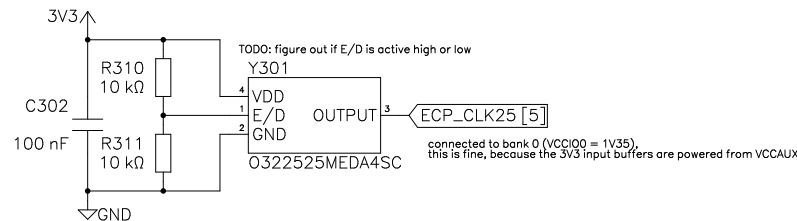
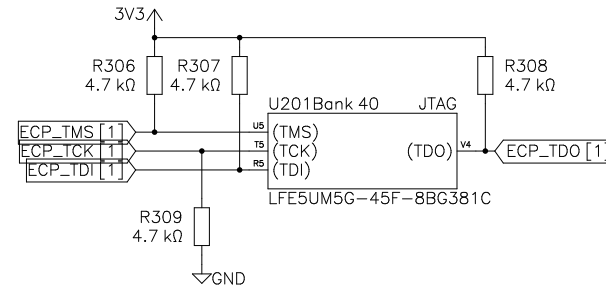
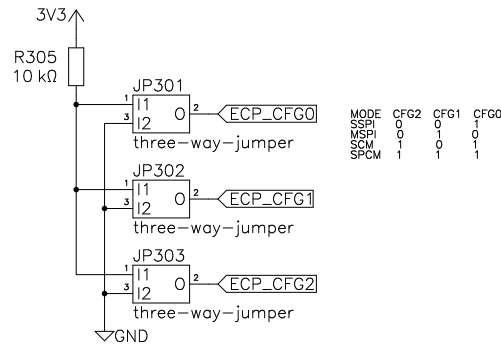
Maybe button for reset,
or somehow connect to trigger reset?

Also has internal pullup during configuration, but maybe we want an external pullup to prevent floating?



The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI operation. When the QE bit is set to a 0 state (factory default for part numbers with ordering options **TIMT**), the /WP pin and /HOLD are enabled. When the QE bit is set to a 1 (factory default for Quad Enabled part numbers with ordering option **TIGT**), the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled.

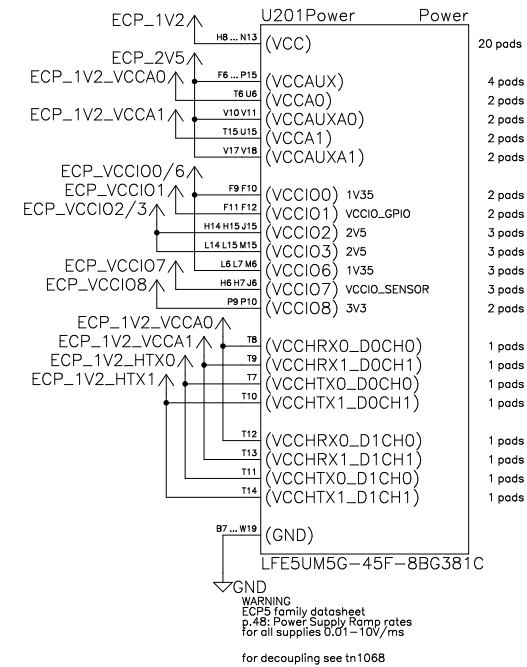
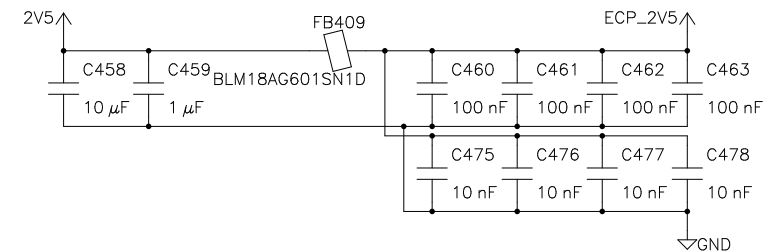
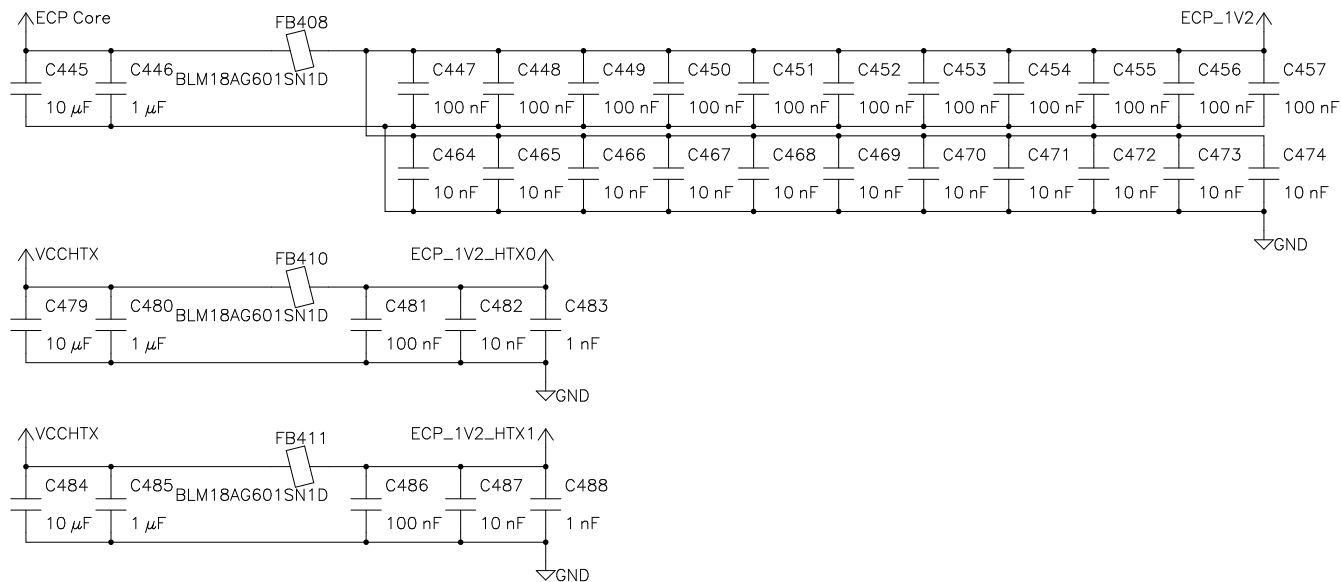
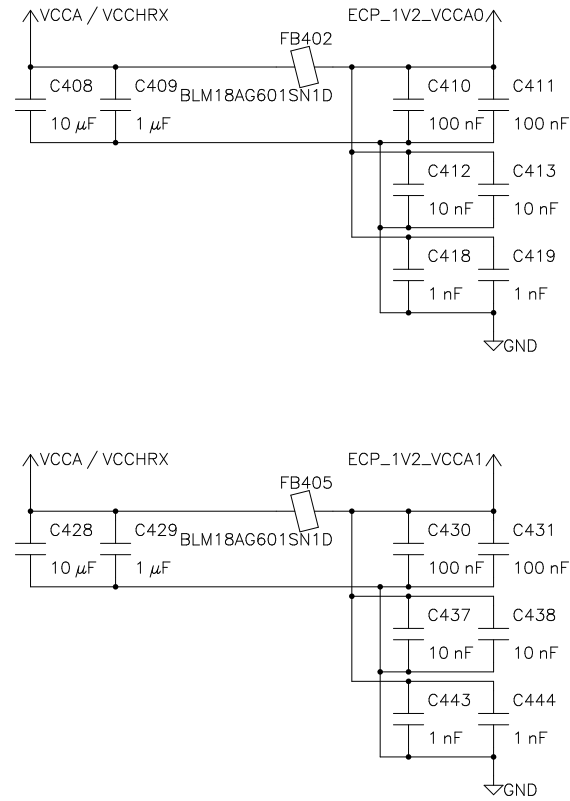
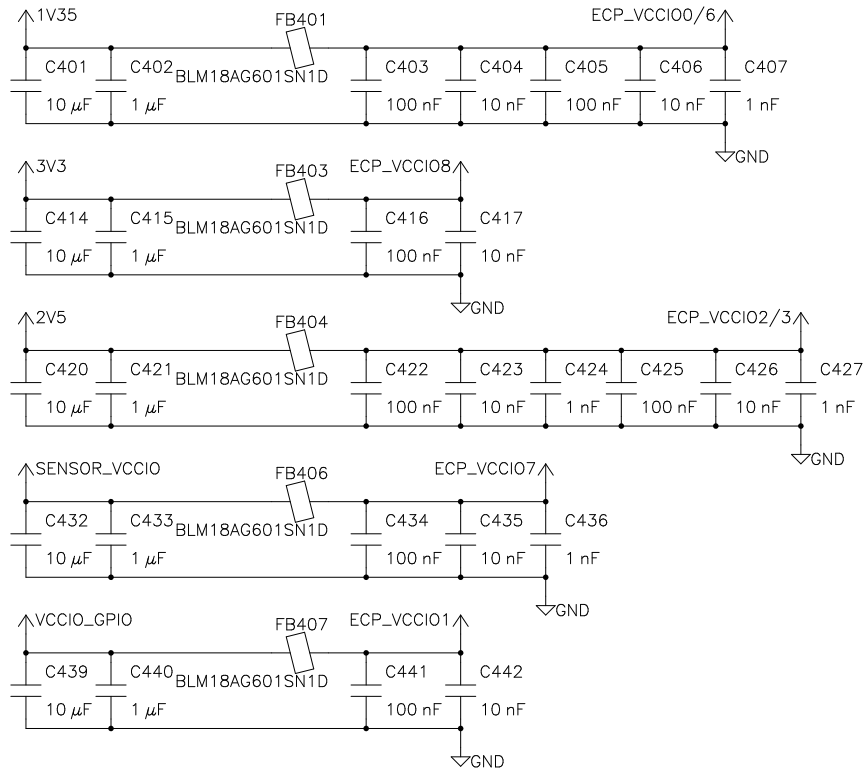
/CS must track VCC during VCC Ramp Up/Down



Sheet	Number
ecp config	3/14
Project	Revision
Axiom micro rev3	0
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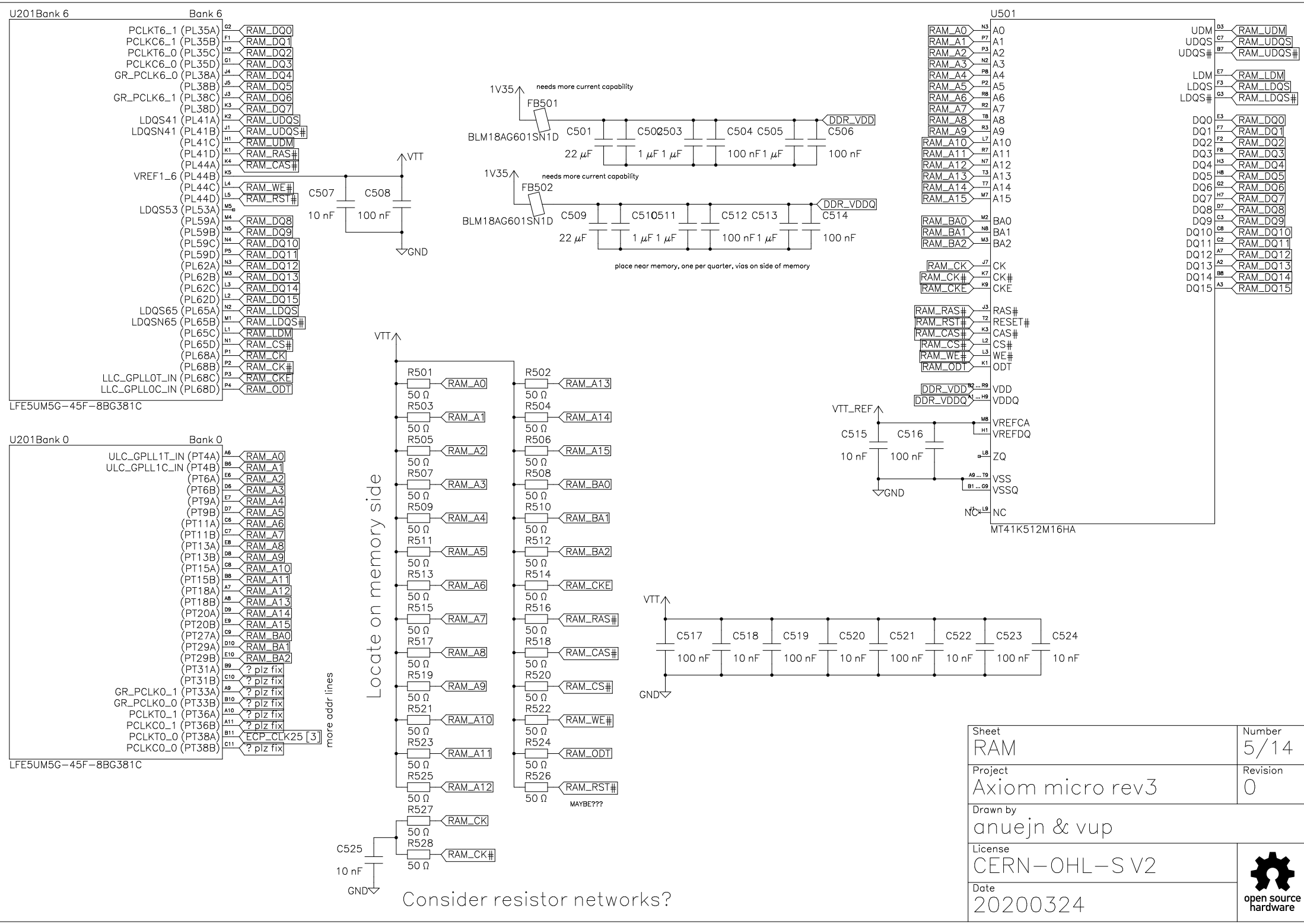


Place decoupling near FPGA, alternate 100n and 10n per pad per rail



Sheet	Number
ecp power	4/14
Project	Revision
Axiom micro rev3	0
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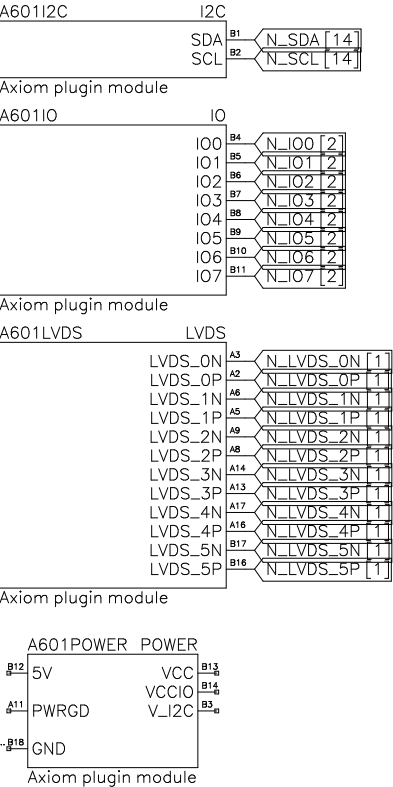




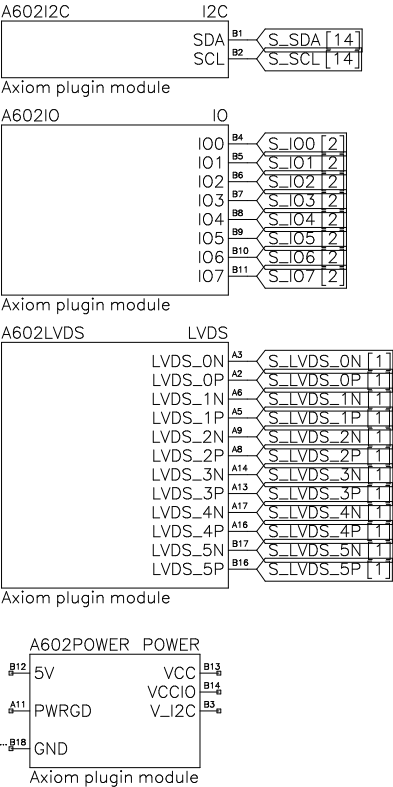
Sheet	RAM	Number	5/14
Project	Axiom micro rev3	Revision	0
Drawn by	anuejn & vup		
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Date	20200324		




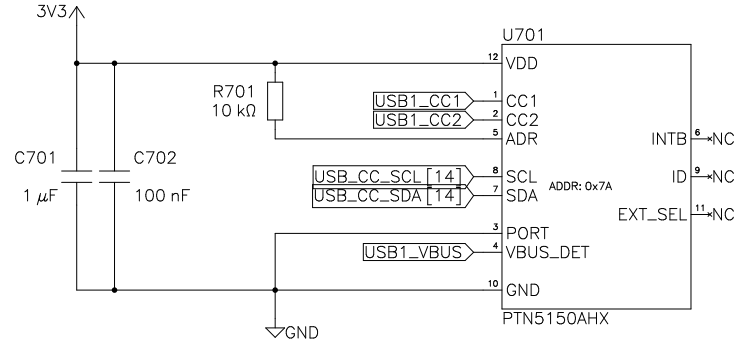
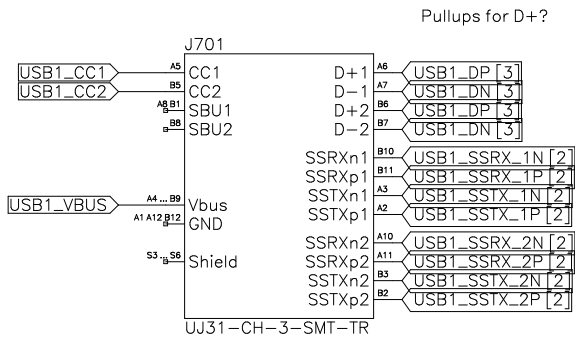
plugin north



plugin south

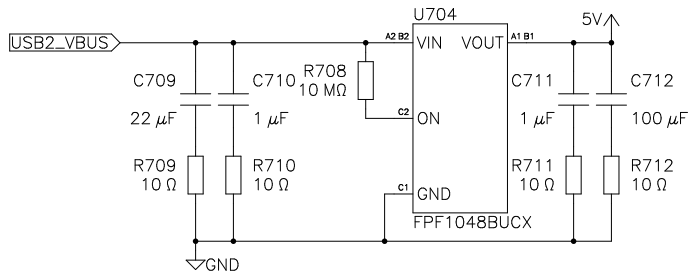
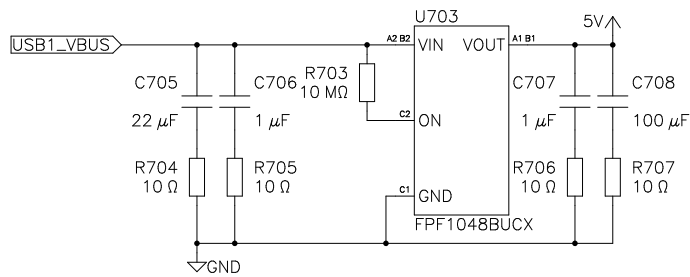
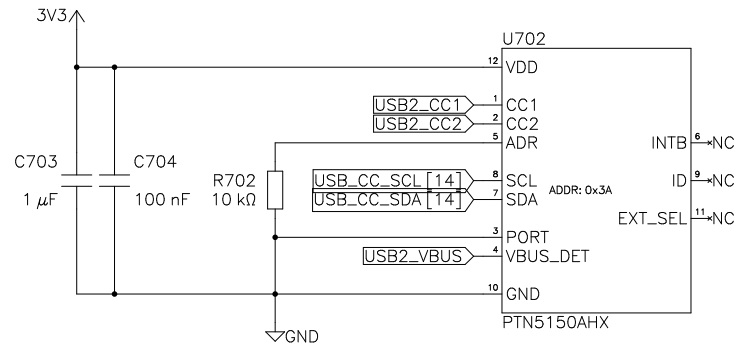
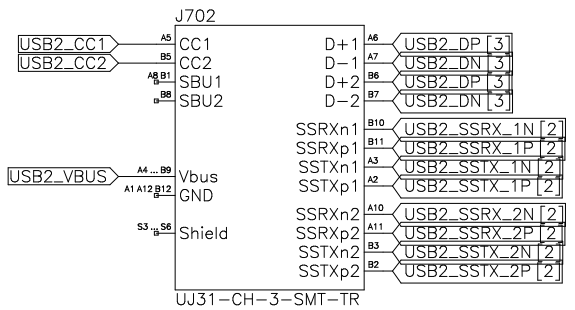



Sheet	Number
plugin	6/14
Project	Revision
Axiom micro rev3	0
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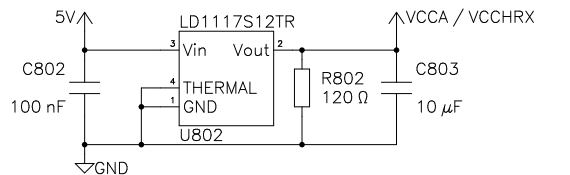


PORT= VDD; DFP mode ($R_p = 80\mu A$ power default for non-I2C mode).
 PORT= Mid (or floating); DRP mode
 PORT=GND; UFP mode

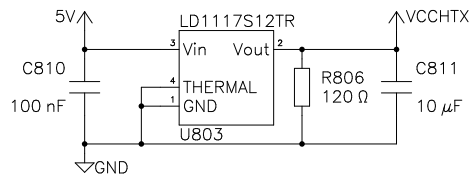
Trinary GPIO Input ADDR pin run from VDD.
 - ADDR pull up to VDD with $10k\uparrow$ resistor (I2C Enabled with ADDR bit 6 equal to 1, I2C Address 0x7A)
 - ADDR pull down to GND with $10k\uparrow$ resistor. (I2C Enabled with ADDR bit 6 equal to 0, I2C Address 0x3A)
 - ADDR = Mid or floating (Pin 6/7/8) configured as OUT1/2/3 in non-I2C mode



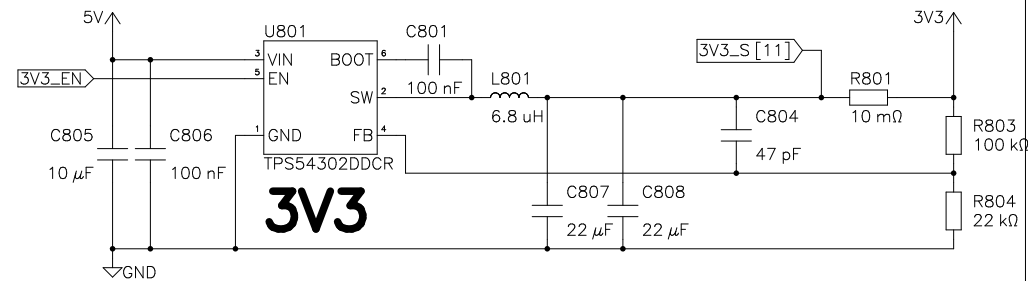
Sheet USB	Number 7/14
Project Axiom micro rev3	Revision 0
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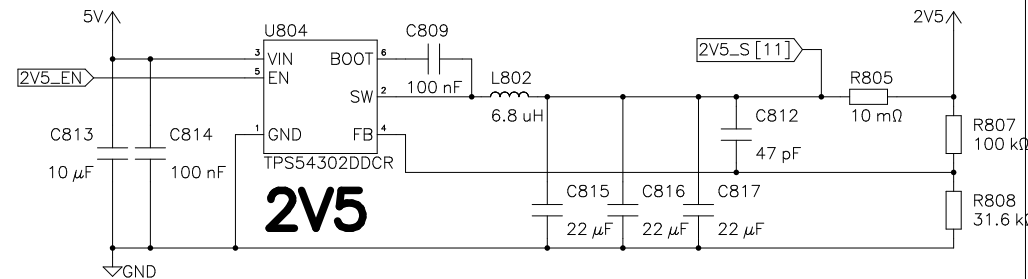
1V2 VCCA / VCCHRX



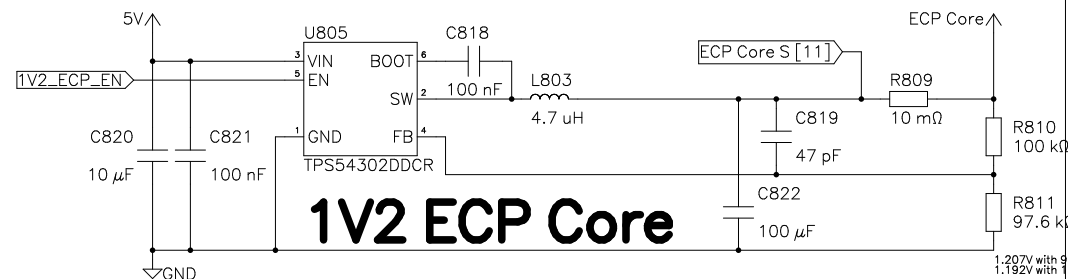
1V2 VCCHTX



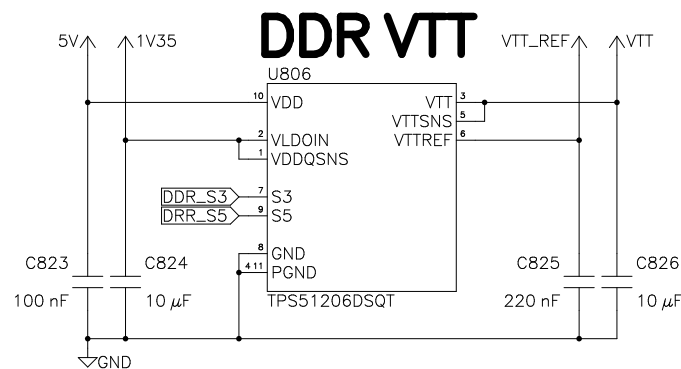
3V3



2V5



1V2 ECP Core



DDR VTT

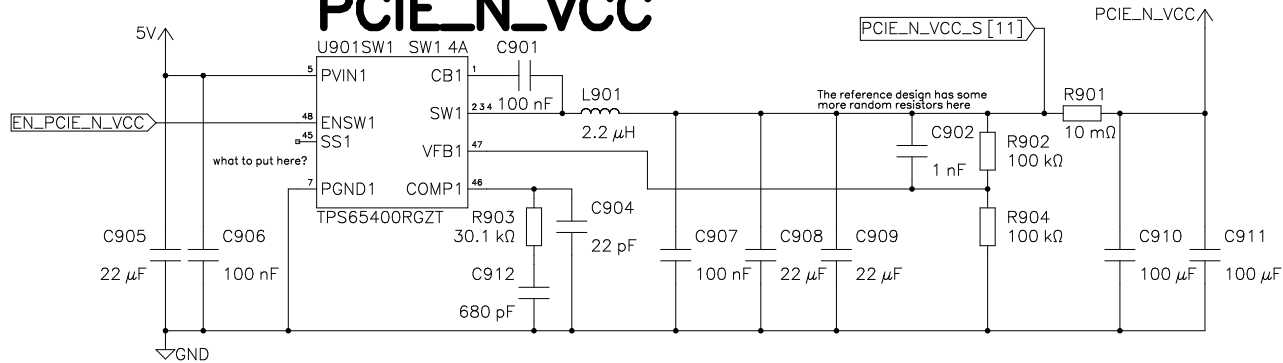
positive terminal of the VTT pin output capacitor(s) as a separate trace from the high-current path from VTT. Consider adding a low-pass R-C filter at the VTTSNS pin in case the ESR of the VTT output capacitor(s) is larger than 2 mΩ. The R-C filter time constant should be approximately the same or slightly lower than the time constant of the VTT output capacitance and ESR.

Sheet	Number
power fixed	8/14
Project	Revision
Axiom micro rev3	0
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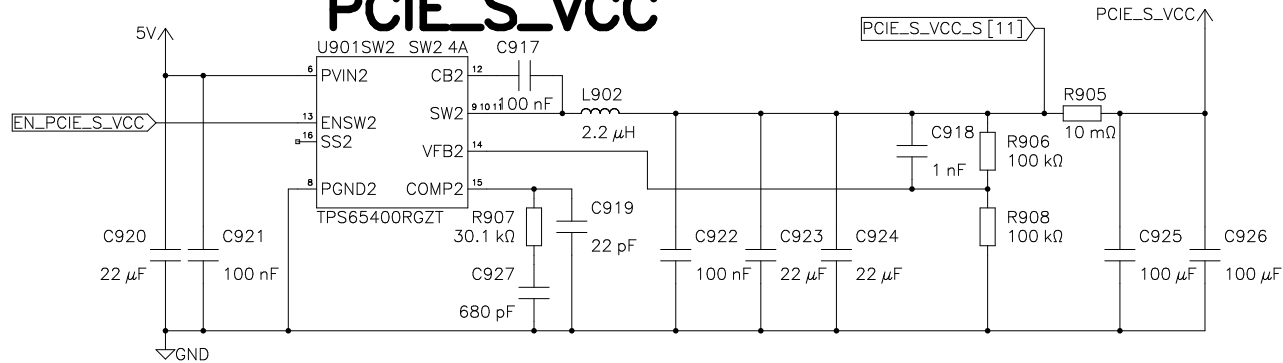


open source hardware

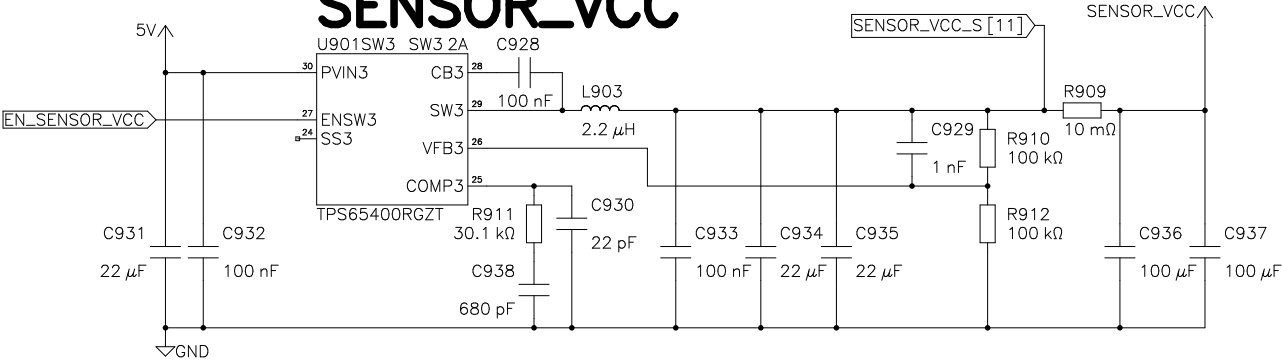
PCIE_N_VCC



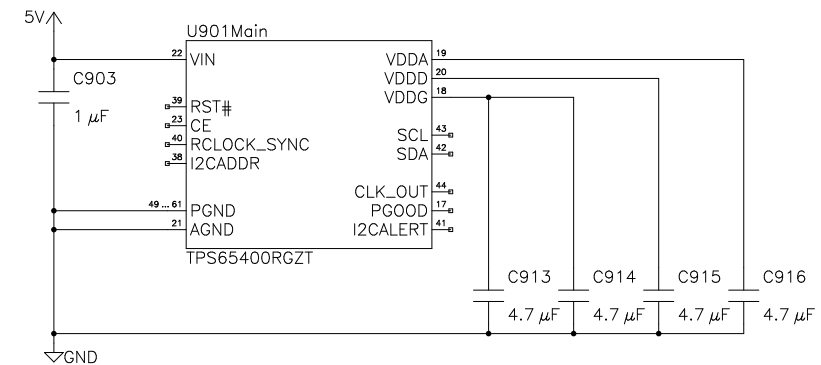
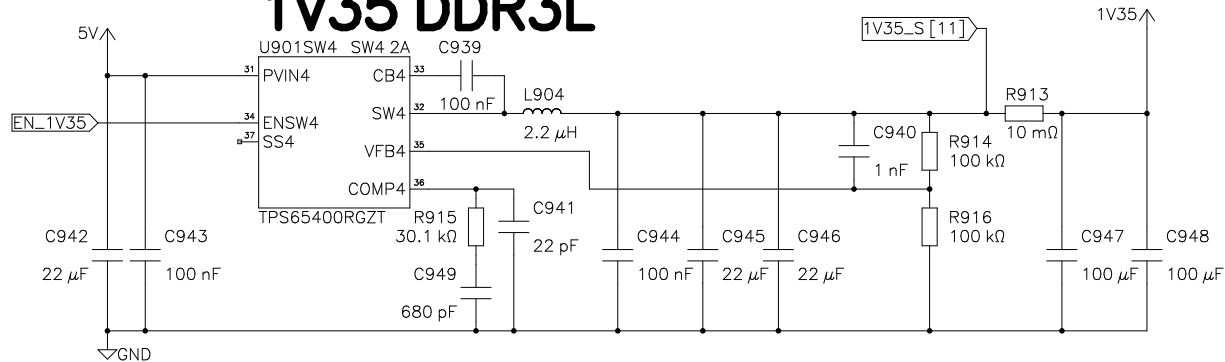
PCIE_S_VCC



SENSOR_VCC



1V35 DDR3L



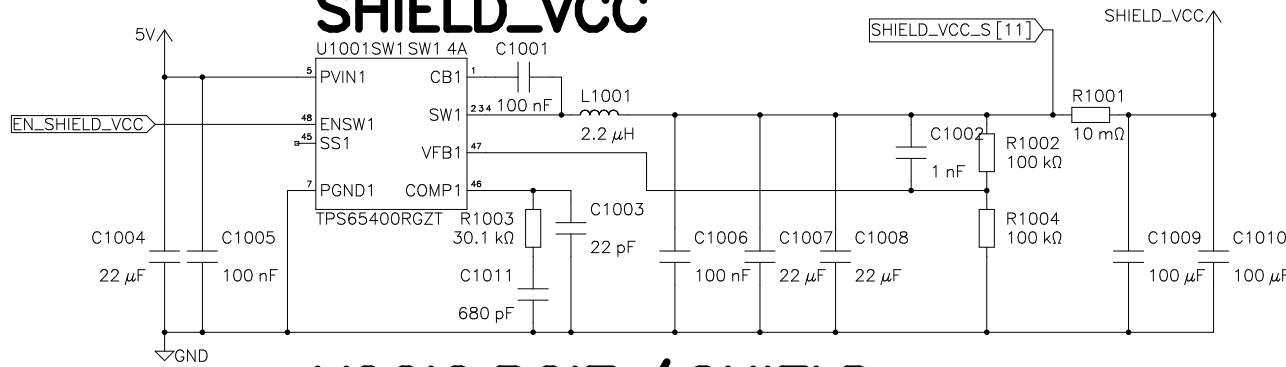
TODO:

- more bulk capacitance?
(for 1V2 the reference schematic has 470uF additionally)
- soft start capacitors
- current limiting resistor for feed forward capacitor
- think about the compensation network
- If the input supply is located more than a few inches from the TPS65400 converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

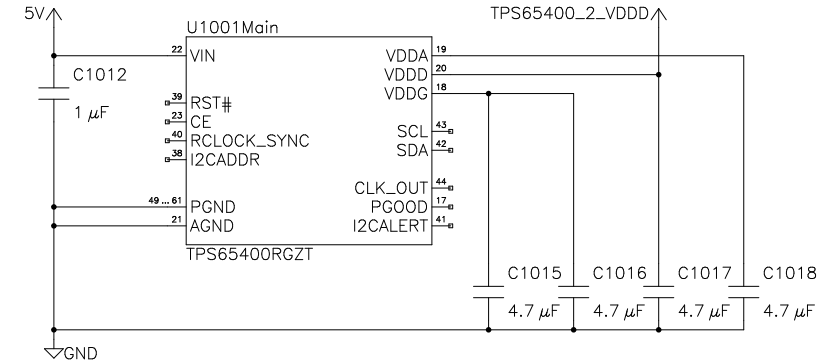
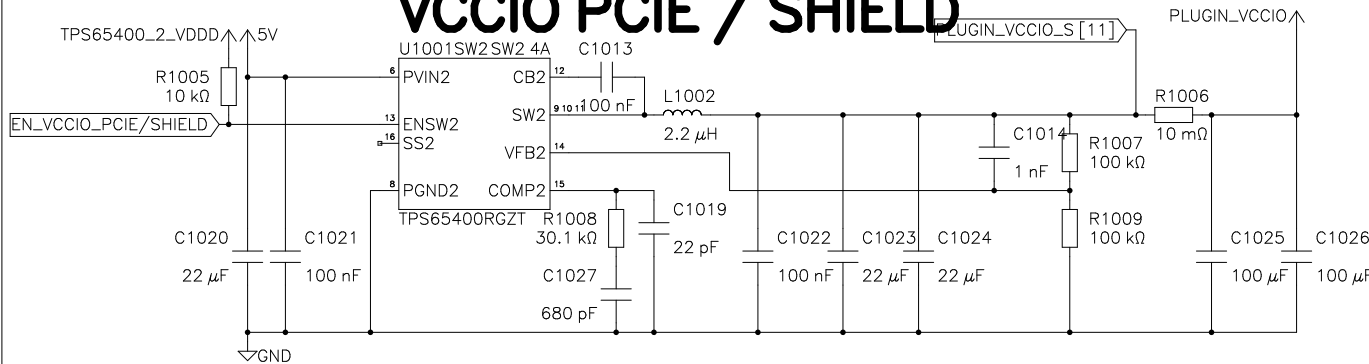
Sheet	power adjustable 1	Number	9/14
Project	Axiom micro rev3	Revision	0
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SHIELD_VCC



VCCIO PCIE / SHIELD

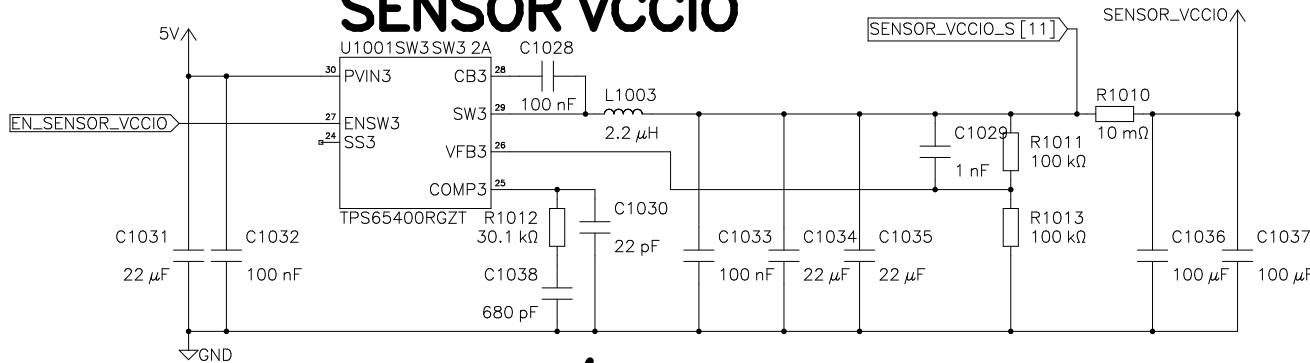


Because JTAG is driven from PLUGIN_VCCIO we somehow need to enable that one before ever being able to access the i2c bus.

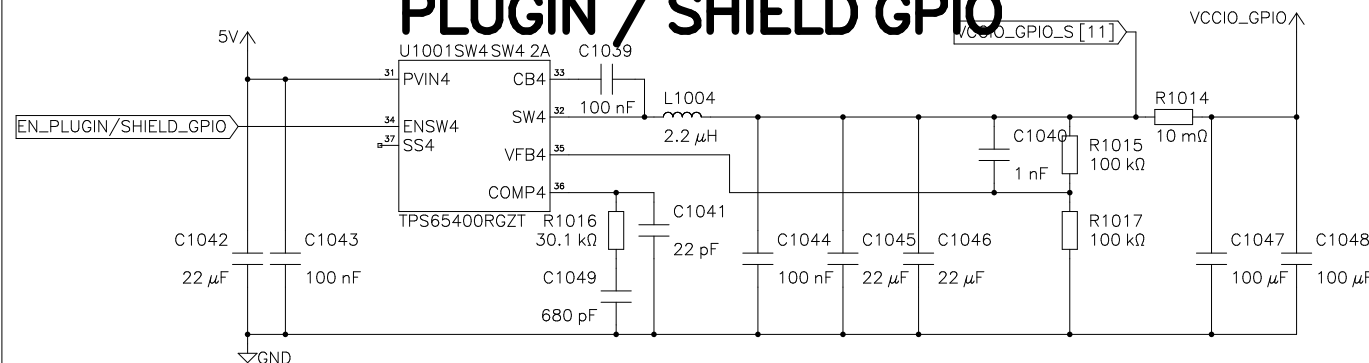
The default for the internal Vref is 0.8V, so we get a output voltage of $0.8V * (1 + 100k / 100k) = 1.6V$. That should work for Jtag (its shifted to 3v3 with a level shifter). To enable the rail, we also add a pullup to EN_VCCIO_PCIE/SHIELD. This pullup can later be overridden by using some i2c commands. (We want to be able to do that to not damage the plugin modules, that get a direct link to this rail)

TODO(robin):
- which rail do we want to pull to? VDDD or maybe 3V3?
- how big should the pullup be?

SENSOR VCCIO



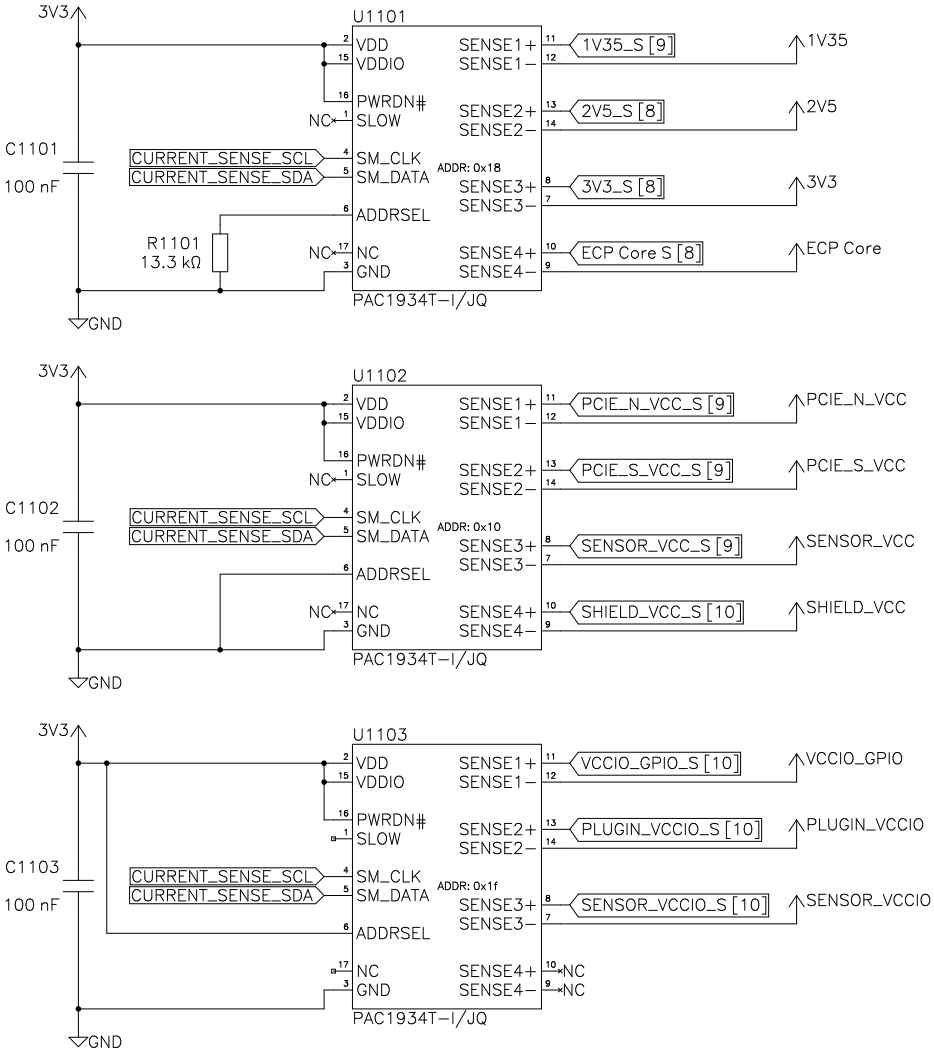
PLUGIN / SHIELD GPIO



Sheet	power adjustable 2	Number	10/14
Project	Axiom micro rev3	Revision	0
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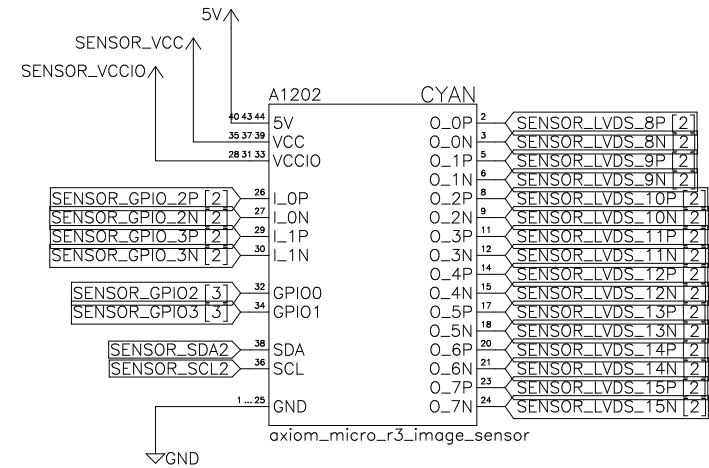
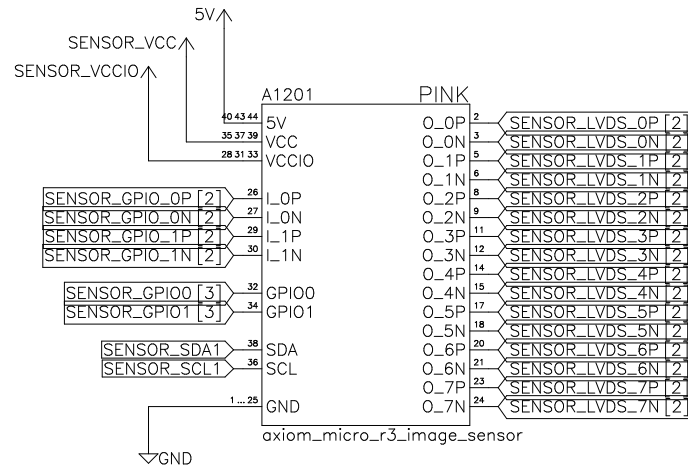


current sense resistors: 0805W8F100MT5E or CS05W8F100MT5E




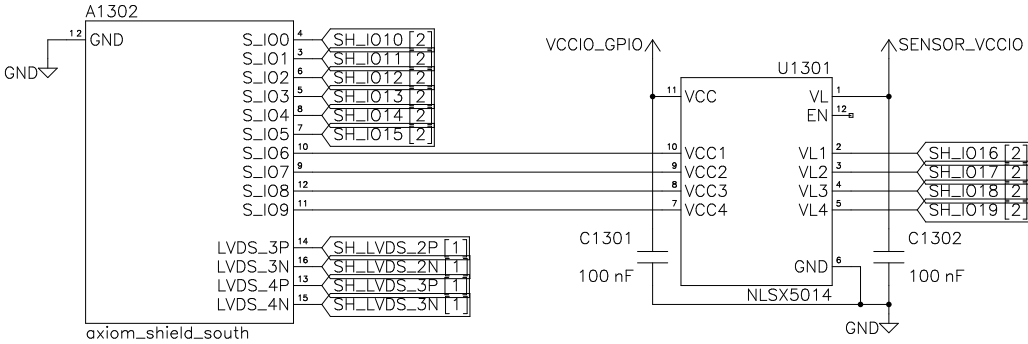
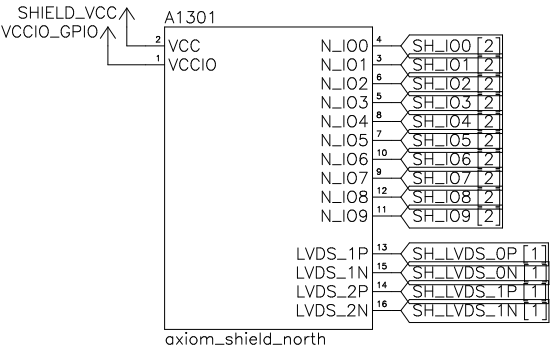
Sheet	Number
current sense	11/14
Project	Revision
Axiom micro rev3	0
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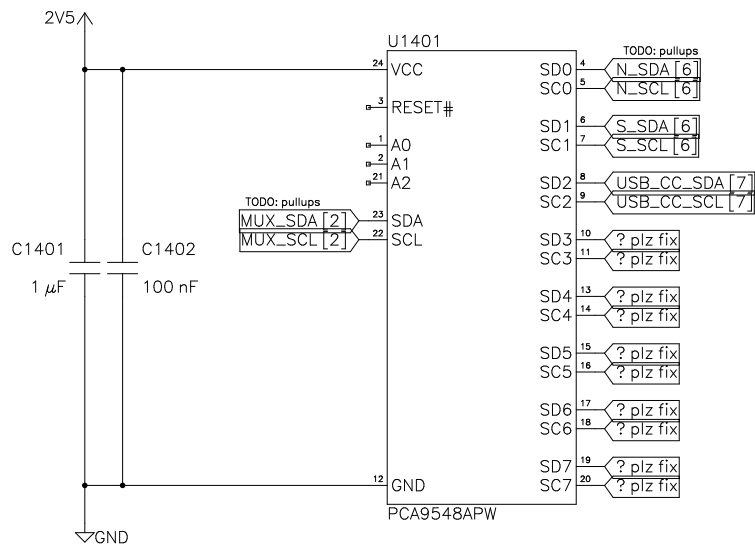
Bulk capacitance for sensor? (0(100uF))

Sheet	image_sensor	Number	12/14
Project	Axiom micro rev3	Revision	0
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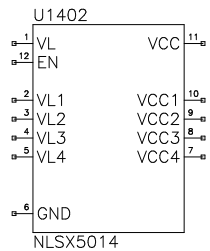



Sheet	shield	Number	13/14
Project	Axiom micro rev3	Revision	0
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2V5 VCC means about 1V8 voltage clamping by the pass through transistors
That shold work for most applications, we just need to be careful with nothing with 1V2 is on the bus



Stuff we want to hang of the i2c mux:
plugin modules
pmic
probably gpio expander for power stuff
????



Sheet misc	Number 14/14
Project Axiom micro rev3	Revision 0
Drawn by anuejn & vup	
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