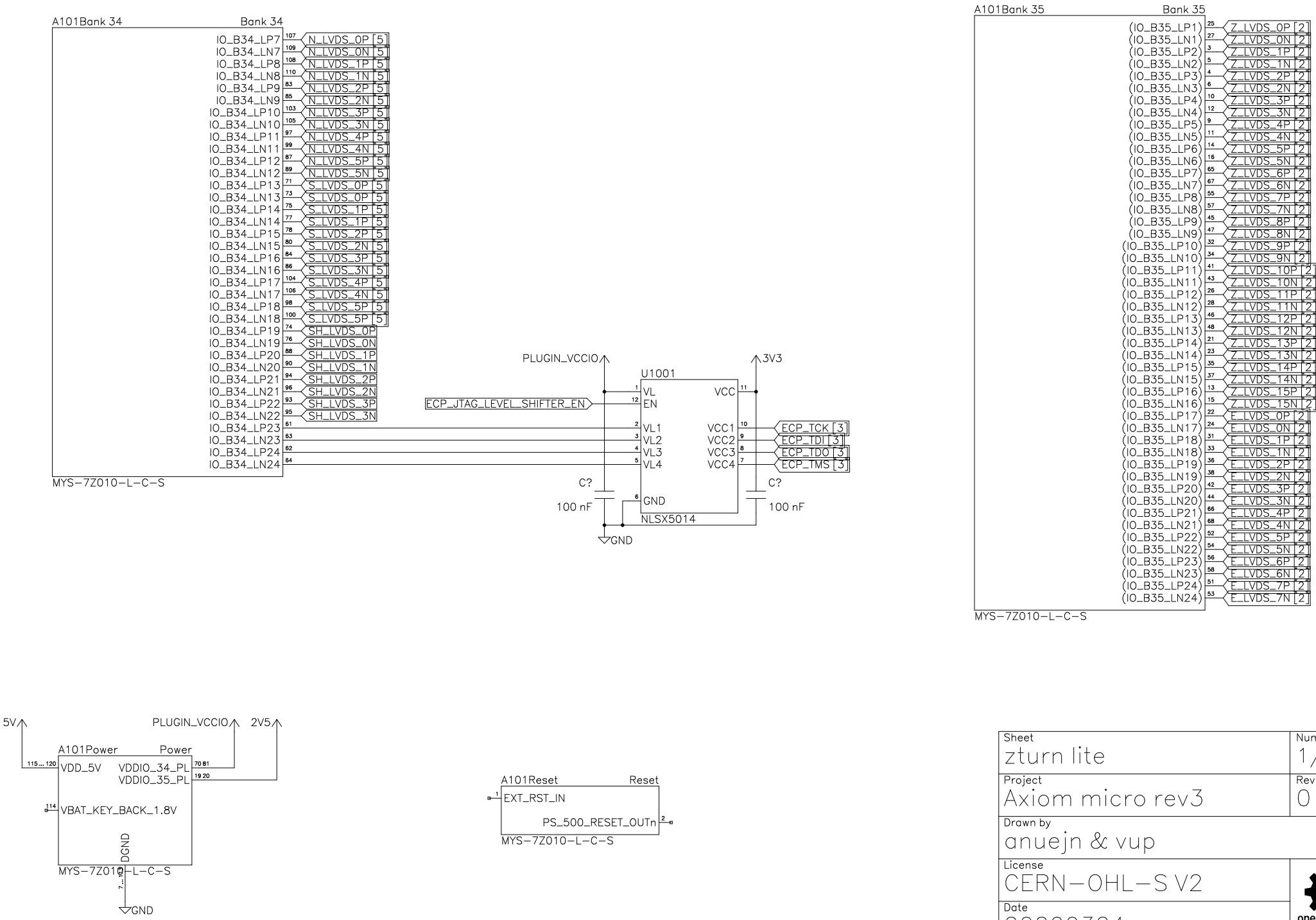
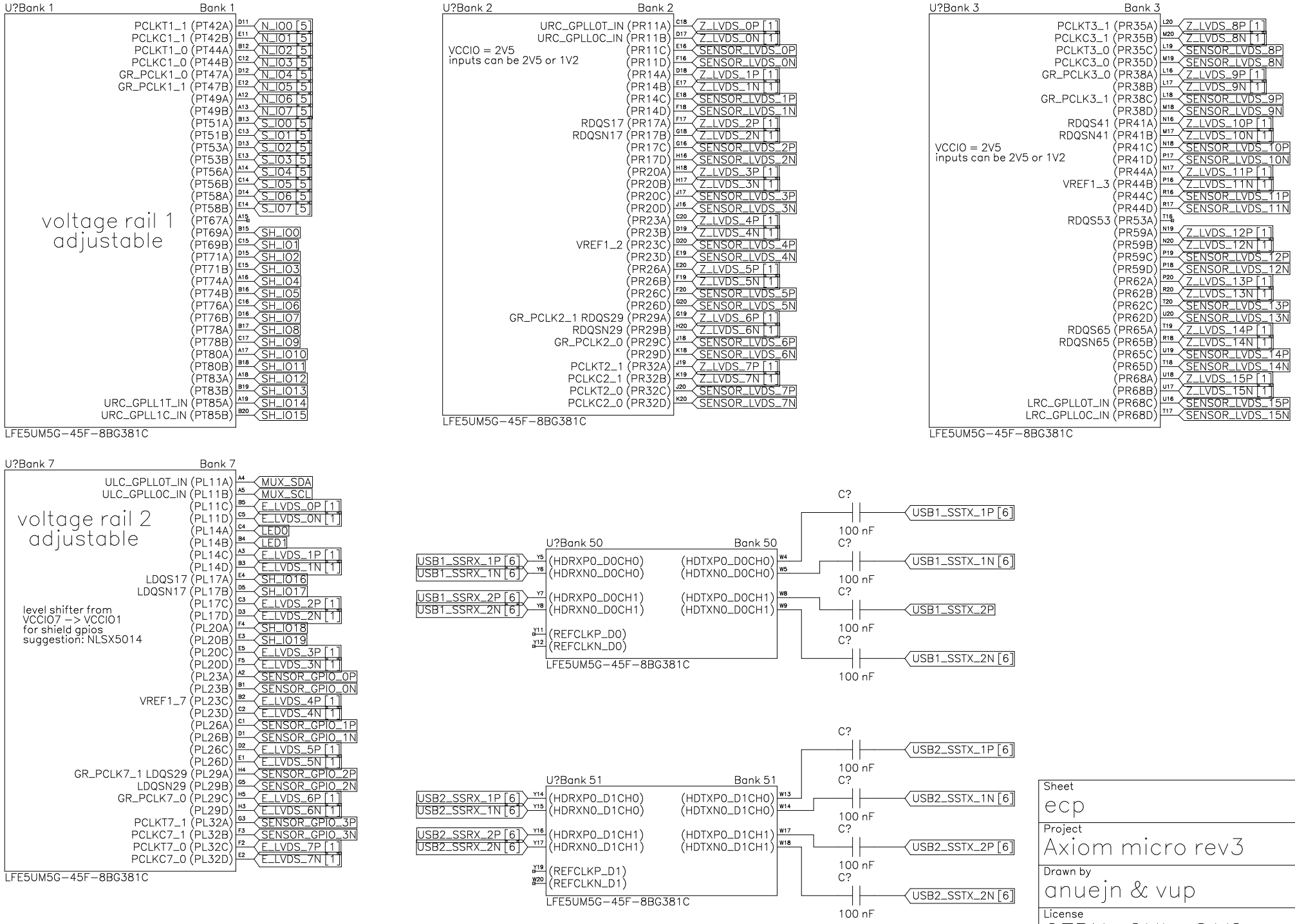


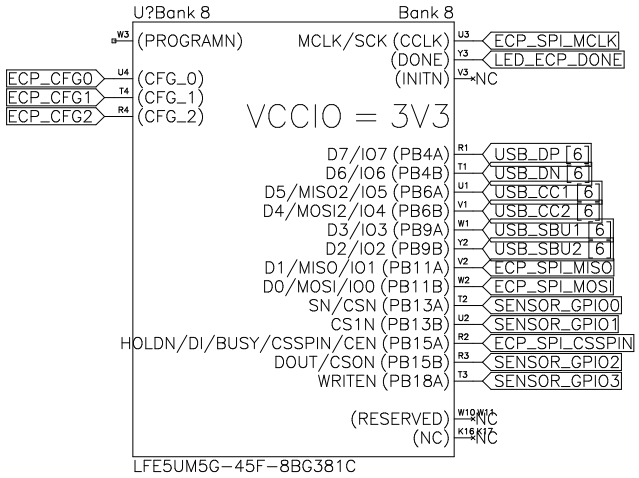
Sheet: zturn lite	Number: 1/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	open source hardware
Date: 20200324	

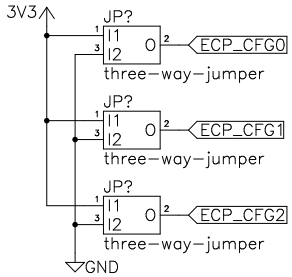

U?Bank 1
Bank 1
PCLKT1_1 (PT42A)
PCLKC1_1 (PT42B)
PCLKT1_0 (PT44A)
PCLKC1_0 (PT44B)
GR_PCLK1_0 (PT47A)
GR_PCLK1_1 (PT47B)
(PT49A)
(PT49B)
(PT51A)
(PT51B)
(PT53A)
(PT53B)
(PT56A)
(PT56B)
(PT58A)
(PT58B)
(PT67A)
(PT69A)
(PT69B)
(PT71A)
(PT71B)
(PT74A)
(PT74B)
(PT76A)
(PT76B)
(PT78A)
(PT78B)
(PT80A)
(PT80B)
(PT83A)
(PT83B)
URC_GPLL1T_IN (PT85A)
URC_GPLL1C_IN (PT85B)
N_IO0 [5]
N_IO1 [5]
N_IO2 [5]
N_IO3 [5]
N_IO4 [5]
N_IO5 [5]
N_IO6 [5]
N_IO7 [5]
S_IO0 [5]
S_IO1 [5]
S_IO2 [5]
S_IO3 [5]
S_IO4 [5]
S_IO5 [5]
S_IO6 [5]
S_IO7 [5]
voltage rail 1
adjustable
SH_IO0
SH_IO1
SH_IO2
SH_IO3
SH_IO4
SH_IO5
SH_IO6
SH_IO7
SH_IO8
SH_IO9
SH_IO10
SH_IO11
SH_IO12
SH_IO13
SH_IO14
SH_IO15
LFE5UM5G-45F-8BG381C
U?Bank 2
Bank 2
URC_GPLL0T_IN (PR11A)
URC_GPLL0C_IN (PR11B)
VCCIO = 2V5
inputs can be 2V5 or 1V2
(PR11C)
(PR11D)
(PR14A)
(PR14B)
(PR14C)
(PR14D)
RDQS17 (PR17A)
RDQSN17 (PR17B)
(PR17C)
(PR17D)
(PR20A)
(PR20B)
(PR20C)
(PR20D)
(PR23A)
(PR23B)
VREF1_2 (PR23C)
(PR23D)
(PR26A)
(PR26B)
(PR26C)
(PR26D)
GR_PCLK2_1 RDQS29 (PR29A)
RDQSN29 (PR29B)
GR_PCLK2_0 (PR29C)
(PR29D)
PCLKT2_1 (PR32A)
PCLKC2_1 (PR32B)
PCLKT2_0 (PR32C)
PCLKC2_0 (PR32D)
Z_LVDS_0P [1]
Z_LVDS_0N [1]
SENSOR_LVDS_0P
SENSOR_LVDS_0N
Z_LVDS_1P [1]
Z_LVDS_1N [1]
SENSOR_LVDS_1P
SENSOR_LVDS_1N
Z_LVDS_2P [1]
Z_LVDS_2N [1]
SENSOR_LVDS_2P
SENSOR_LVDS_2N
Z_LVDS_3P [1]
Z_LVDS_3N [1]
SENSOR_LVDS_3P
SENSOR_LVDS_3N
Z_LVDS_4P [1]
Z_LVDS_4N [1]
SENSOR_LVDS_4P
SENSOR_LVDS_4N
Z_LVDS_5P [1]
Z_LVDS_5N [1]
SENSOR_LVDS_5P
SENSOR_LVDS_5N
Z_LVDS_6P [1]
Z_LVDS_6N [1]
SENSOR_LVDS_6P
SENSOR_LVDS_6N
Z_LVDS_7P [1]
Z_LVDS_7N [1]
SENSOR_LVDS_7P
SENSOR_LVDS_7N
LFE5UM5G-45F-8BG381C
U?Bank 3
Bank 3
PCLKT3_1 (PR35A)
PCLKC3_1 (PR35B)
PCLKT3_0 (PR35C)
PCLKC3_0 (PR35D)
GR_PCLK3_0 (PR38A)
(PR38B)
GR_PCLK3_1 (PR38C)
(PR38D)
RDQS41 (PR41A)
RDQSN41 (PR41B)
VCCIO = 2V5
inputs can be 2V5 or 1V2
(PR41C)
(PR41D)
(PR44A)
VREF1_3 (PR44B)
(PR44C)
(PR44D)
RDQS53 (PR53A)
(PR59A)
(PR59B)
(PR59C)
(PR59D)
(PR62A)
(PR62B)
(PR62C)
(PR62D)
RDQS65 (PR65A)
RDQSN65 (PR65B)
(PR65C)
(PR65D)
(PR68A)
(PR68B)
LRC_GPLL0T_IN (PR68C)
LRC_GPLL0C_IN (PR68D)
Z_LVDS_8P [1]
Z_LVDS_8N [1]
SENSOR_LVDS_8P
SENSOR_LVDS_8N
Z_LVDS_9P [1]
Z_LVDS_9N [1]
SENSOR_LVDS_9P
SENSOR_LVDS_9N
Z_LVDS_10P [1]
Z_LVDS_10N [1]
SENSOR_LVDS_10P
SENSOR_LVDS_10N
Z_LVDS_11P [1]
Z_LVDS_11N [1]
SENSOR_LVDS_11P
SENSOR_LVDS_11N
Z_LVDS_12P [1]
Z_LVDS_12N [1]
SENSOR_LVDS_12P
SENSOR_LVDS_12N
Z_LVDS_13P [1]
Z_LVDS_13N [1]
SENSOR_LVDS_13P
SENSOR_LVDS_13N
Z_LVDS_14P [1]
Z_LVDS_14N [1]
SENSOR_LVDS_14P
SENSOR_LVDS_14N
Z_LVDS_15P [1]
Z_LVDS_15N [1]
SENSOR_LVDS_15P
SENSOR_LVDS_15N
LFE5UM5G-45F-8BG381C
U?Bank 7
Bank 7
ULC_GPLL0T_IN (PL11A)
ULC_GPLL0C_IN (PL11B)
(PL11C)
(PL11D)
(PL14A)
(PL14B)
(PL14C)
(PL14D)
LDQS17 (PL17A)
LDQSN17 (PL17B)
(PL17C)
(PL17D)
(PL20A)
(PL20B)
(PL20C)
(PL20D)
(PL23A)
(PL23B)
VREF1_7 (PL23C)
(PL23D)
(PL26A)
(PL26B)
(PL26C)
(PL26D)
GR_PCLK7_1 LDQS29 (PL29A)
LDQSN29 (PL29B)
GR_PCLK7_0 (PL29C)
(PL29D)
PCLKT7_1 (PL32A)
PCLKC7_1 (PL32B)
PCLKT7_0 (PL32C)
PCLKC7_0 (PL32D)
MUX_SDA
MUX_SCL
E_LVDS_0P [1]
E_LVDS_0N [1]
LED0
LED1
E_LVDS_1P [1]
E_LVDS_1N [1]
SH_IO16
SH_IO17
E_LVDS_2P [1]
E_LVDS_2N [1]
SH_IO18
SH_IO19
E_LVDS_3P [1]
E_LVDS_3N [1]
SENSOR_GPIO_0P
SENSOR_GPIO_0N
E_LVDS_4P [1]
E_LVDS_4N [1]
SENSOR_GPIO_1P
SENSOR_GPIO_1N
E_LVDS_5P [1]
E_LVDS_5N [1]
SENSOR_GPIO_2P
SENSOR_GPIO_2N
E_LVDS_6P [1]
E_LVDS_6N [1]
SENSOR_GPIO_3P
SENSOR_GPIO_3N
E_LVDS_7P [1]
E_LVDS_7N [1]
voltage rail 2
adjustable
level shifter from
VCCIO7 -> VCCIO1
for shield gpios
suggestion: NLSX5014
LFE5UM5G-45F-8BG381C
U?Bank 50
Bank 50
USB1_SSRX_1P [6]
USB1_SSRX_1N [6]
USB1_SSRX_2P [6]
USB1_SSRX_2N [6]
(HDRXP0_D0CH0)
(HDRXN0_D0CH0)
(HDRXP0_D0CH1)
(HDRXN0_D0CH1)
(REFCLKP_D0)
(REFCLKN_D0)
(HDTXP0_D0CH0)
(HDTXN0_D0CH0)
(HDTXP0_D0CH1)
(HDTXN0_D0CH1)
C?
100 nF
USB1_SSTX_1P [6]
USB1_SSTX_1N [6]
USB1_SSTX_2P
USB1_SSTX_2N [6]
LFE5UM5G-45F-8BG381C
U?Bank 51
Bank 51
USB2_SSRX_1P [6]
USB2_SSRX_1N [6]
USB2_SSRX_2P [6]
USB2_SSRX_2N [6]
(HDRXP0_D1CH0)
(HDRXN0_D1CH0)
(HDRXP0_D1CH1)
(HDRXN0_D1CH1)
(REFCLKP_D1)
(REFCLKN_D1)
(HDTXP0_D1CH0)
(HDTXN0_D1CH0)
(HDTXP0_D1CH1)
(HDTXN0_D1CH1)
C?
100 nF
USB2_SSTX_1P [6]
USB2_SSTX_1N [6]
USB2_SSTX_2P [6]
USB2_SSTX_2N [6]
LFE5UM5G-45F-8BG381C
Sheet
ecp
Number
2/12
Project
Axiom micro rev3
Revision
0
Drawn by
anuejn & vup
License
CERN-OHL-S V2
Date
20200324
open source hardware

PROGRAMN

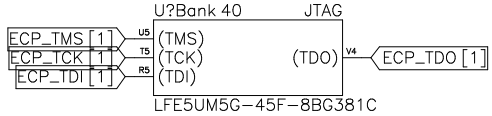
Maybe button for reset,
or somehow connect to trigger reset?

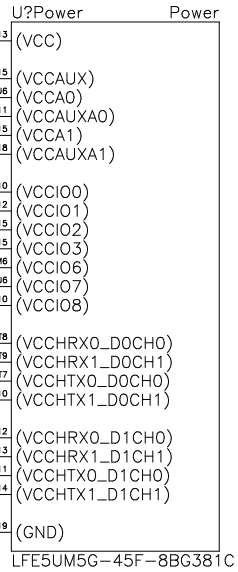
Also has internal pullup during configuration, but maybe we want a external pullup to prevent floating?

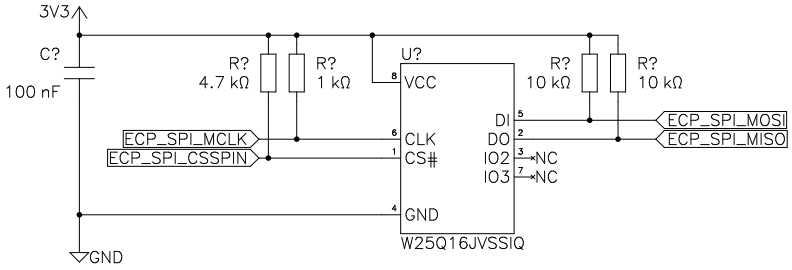




MODE	CFG2	CFG1	CFG0
SSPI	0	0	1
MSPI	0	1	0
SCM	1	0	1
SPCM	1	1	1



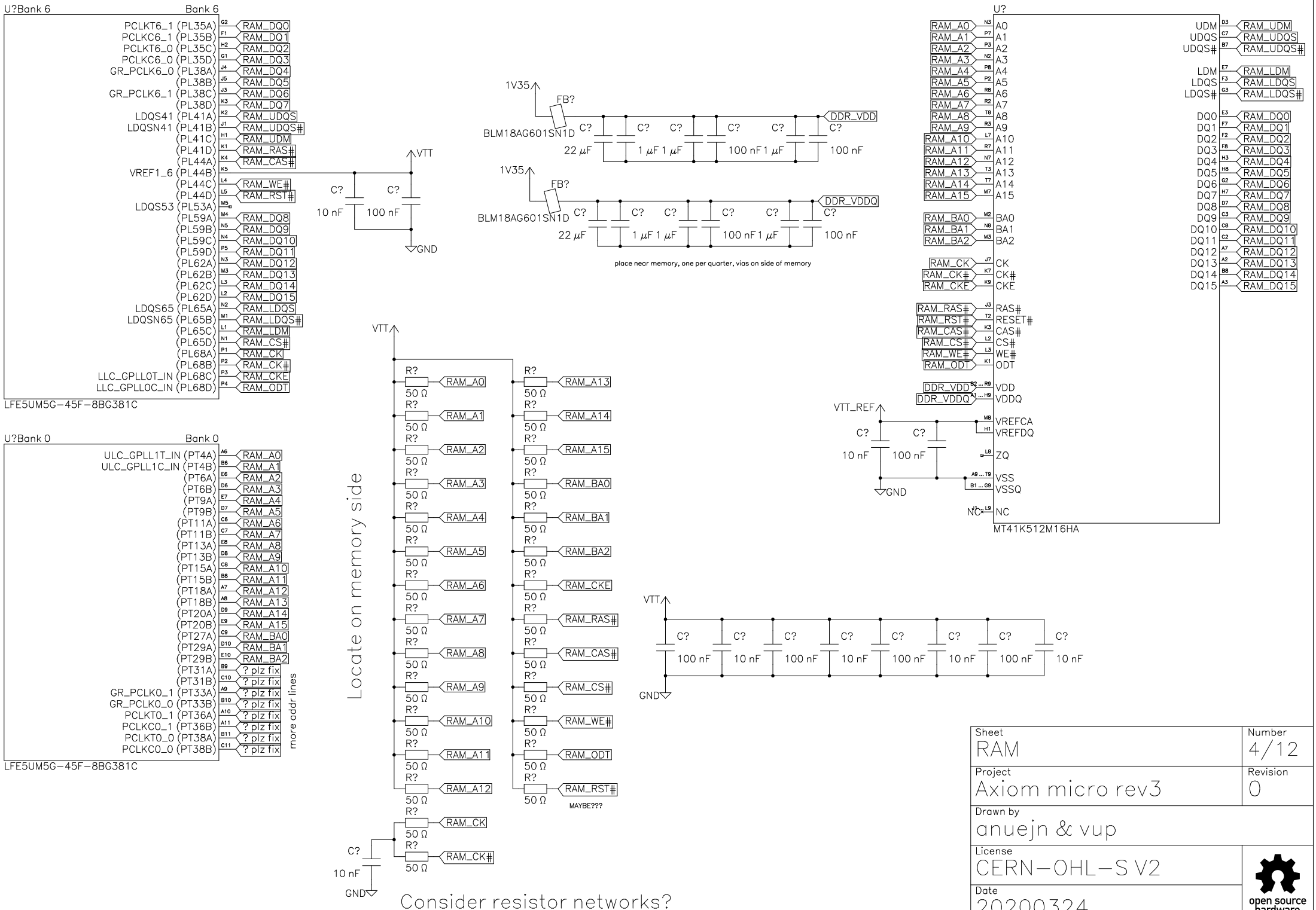




The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI operation. When the QE bit is set to a 0 state (factory default for part numbers with ordering options †IM†), the /WP pin and /HOLD are enabled. When the QE bit is set to a 1 (factory default for Quad Enabled part numbers with ordering option †IQ†), the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled

/CS must track VCC
during VCC Ramp Up/Down

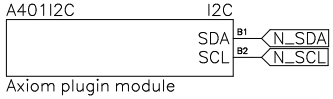
Sheet: ecp	Number: 2/11
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	open source hardware
Date: 20200324	



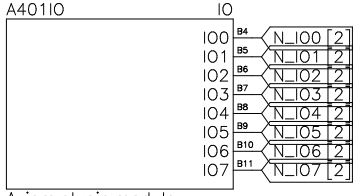
Sheet: RAM	Number: 4/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	
Date: 20200324	

open source hardware

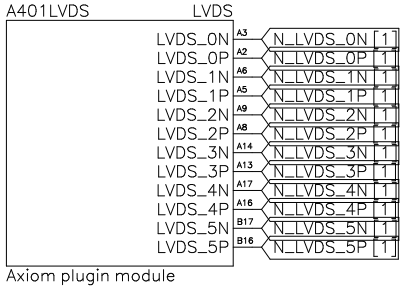
plugin north



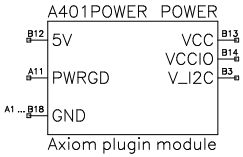
Axiom plugin module



Axiom plugin module

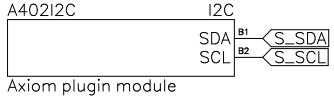


Axiom plugin module

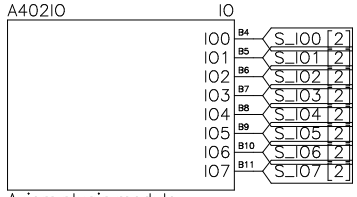


Axiom plugin module

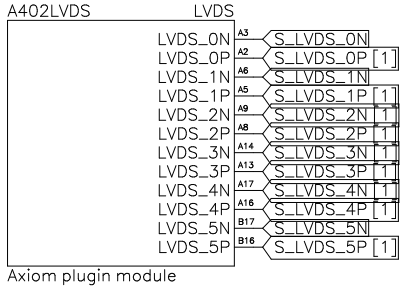
plugin south



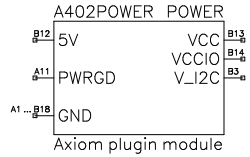
Axiom plugin module



Axiom plugin module



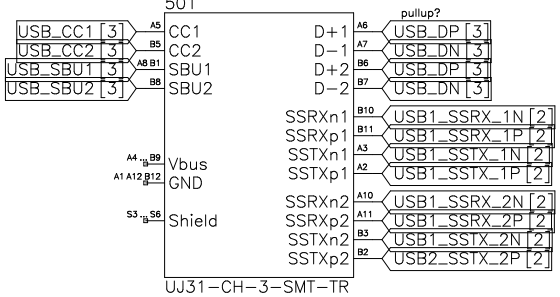
Axiom plugin module

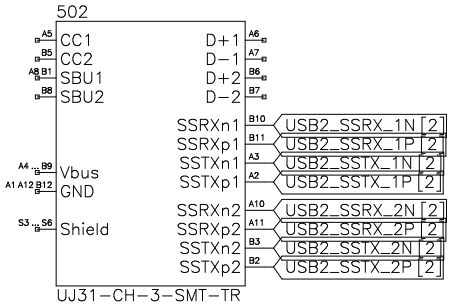


Axiom plugin module

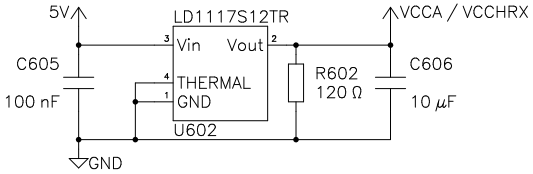
Sheet plugin	Number 5/12
Project Axiom micro rev3	Revision 0
Drawn by anuejn & vup	
License CERN-OHL-S V2	open source hardware
Date 20200324	

We probably want to be a upwards facing port?
CC1/2 need pullups / pulldowns

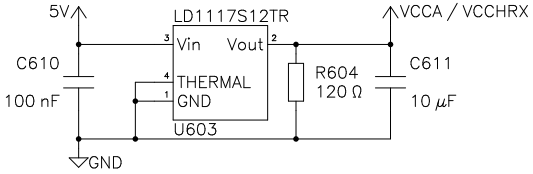




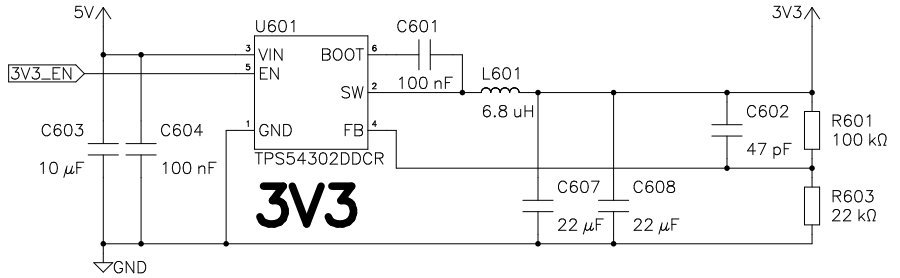
Sheet: USB	Number: 6/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN−OHL−S V2	open source hardware
Date: 20200324	



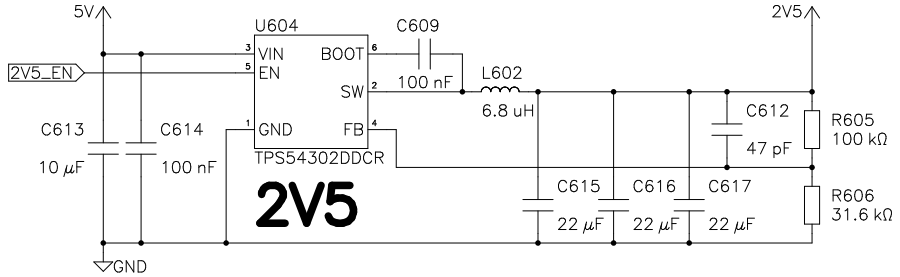
1V2 VCCA / VCCHRX



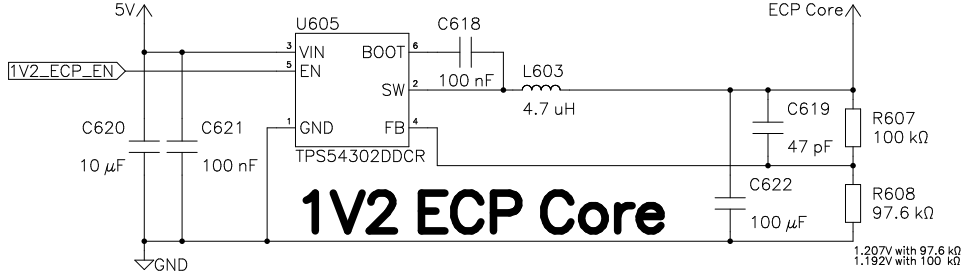
1V2 VCCHTX



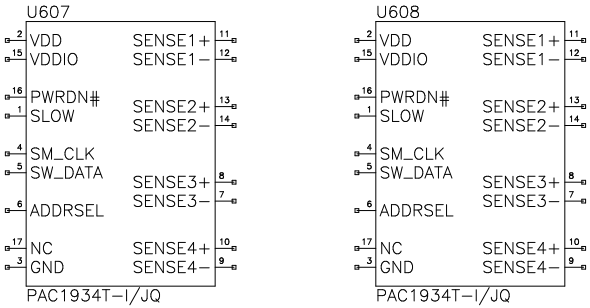
3V3

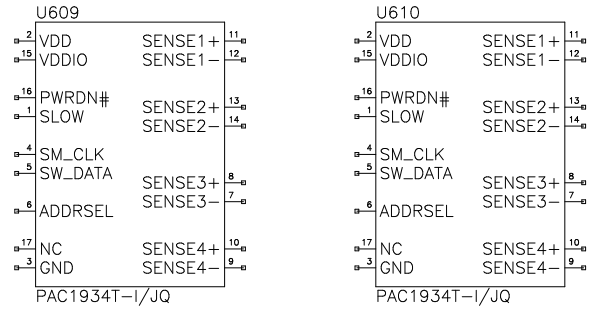


2V5

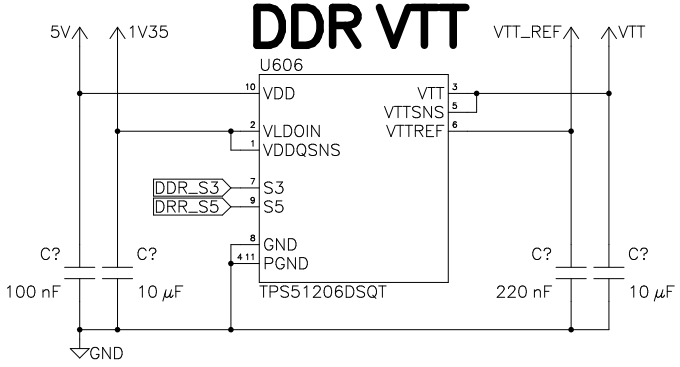


1V2 ECP Core



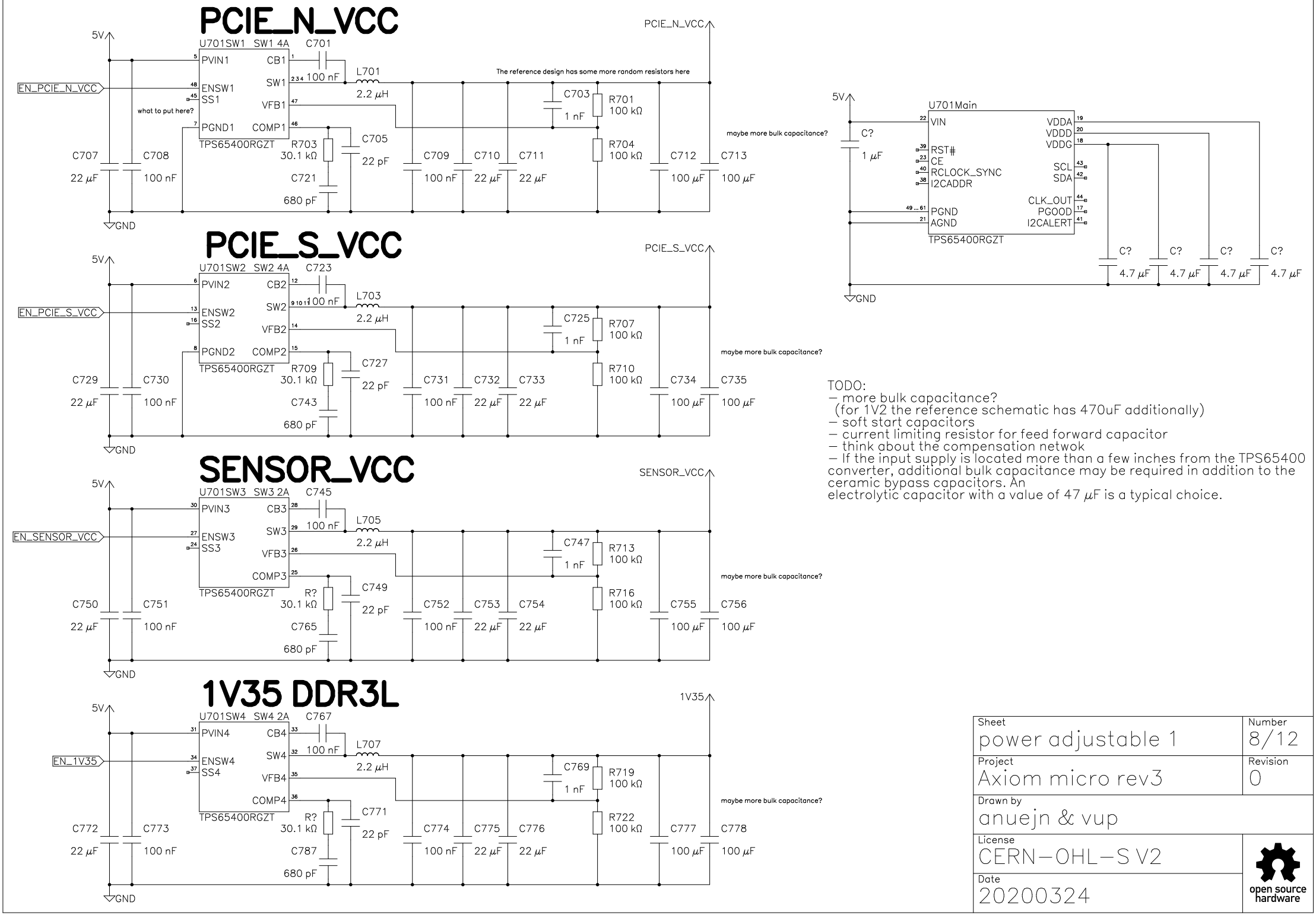


DDR VTT



positive terminal of the VTT pin output capacitor(s) as a separate trace from the high−current path from VTT. Consider adding a low−pass R−C filter at the VTTSNS pin in case the ESR of the VTT output capacitor(s) is larger than 2 mΩ. The R−C filter time constant should be approximately the same or slightly lower than the time constant of the VTT output capacitance and ESR.

Sheet: power fixed	Number: 7/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN−OHL−S V2	open source hardware
Date: 20200324	


PCIE_N_VCC
5V
U701SW1 SW1 4A
PVIN1
ENSW1
SS1
PGND1
CB1
SW1
VFB1
COMP1
TPS65400RGZT
EN_PCIE_N_VCC
what to put here?
C701
100 nF
L701
2.2 µH
The reference design has some more random resistors here
PCIE_N_VCC
C703
1 nF
R701
100 kΩ
R704
100 kΩ
maybe more bulk capacitance?
C707
22 µF
C708
100 nF
R703
30.1 kΩ
C721
680 pF
C705
22 pF
C709
100 nF
C710
22 µF
C711
22 µF
C712
100 µF
C713
100 µF
GND
PCIE_S_VCC
5V
U701SW2 SW2 4A
PVIN2
ENSW2
SS2
PGND2
CB2
SW2
VFB2
COMP2
TPS65400RGZT
EN_PCIE_S_VCC
C723
100 nF
L703
2.2 µH
PCIE_S_VCC
C725
1 nF
R707
100 kΩ
R710
100 kΩ
maybe more bulk capacitance?
C729
22 µF
C730
100 nF
R709
30.1 kΩ
C743
680 pF
C727
22 pF
C731
100 nF
C732
22 µF
C733
22 µF
C734
100 µF
C735
100 µF
GND
SENSOR_VCC
5V
U701SW3 SW3 2A
PVIN3
ENSW3
SS3
CB3
SW3
VFB3
COMP3
TPS65400RGZT
EN_SENSOR_VCC
C745
100 nF
L705
2.2 µH
SENSOR_VCC
C747
1 nF
R713
100 kΩ
R716
100 kΩ
maybe more bulk capacitance?
C750
22 µF
C751
100 nF
R?
30.1 kΩ
C765
680 pF
C749
22 pF
C752
100 nF
C753
22 µF
C754
22 µF
C755
100 µF
C756
100 µF
GND
1V35 DDR3L
5V
U701SW4 SW4 2A
PVIN4
ENSW4
SS4
CB4
SW4
VFB4
COMP4
TPS65400RGZT
EN_1V35
C767
100 nF
L707
2.2 µH
1V35
C769
1 nF
R719
100 kΩ
R722
100 kΩ
maybe more bulk capacitance?
C772
22 µF
C773
100 nF
R?
30.1 kΩ
C787
680 pF
C771
22 pF
C774
100 nF
C775
22 µF
C776
22 µF
C777
100 µF
C778
100 µF
GND
5V
U701Main
VIN
RST#
CE
RCLOCK_SYNC
I2CADDR
PGND
AGND
VDDA
VDDD
VDDG
SCL
SDA
CLK_OUT
PGOOD
I2CALERT
TPS65400RGZT
C?
1 µF
C?
4.7 µF
C?
4.7 µF
C?
4.7 µF
C?
4.7 µF
GND
TODO:
– more bulk capacitance?
(for 1V2 the reference schematic has 470uF additionally)
– soft start capacitors
– current limiting resistor for feed forward capacitor
– think about the compensation netwok
– If the input supply is located more than a few inches from the TPS65400 converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An
electrolytic capacitor with a value of 47 µF is a typical choice.
Sheet
power adjustable 1
Number
8/12
Project
Axiom micro rev3
Revision
0
Drawn by
anuejn & vup
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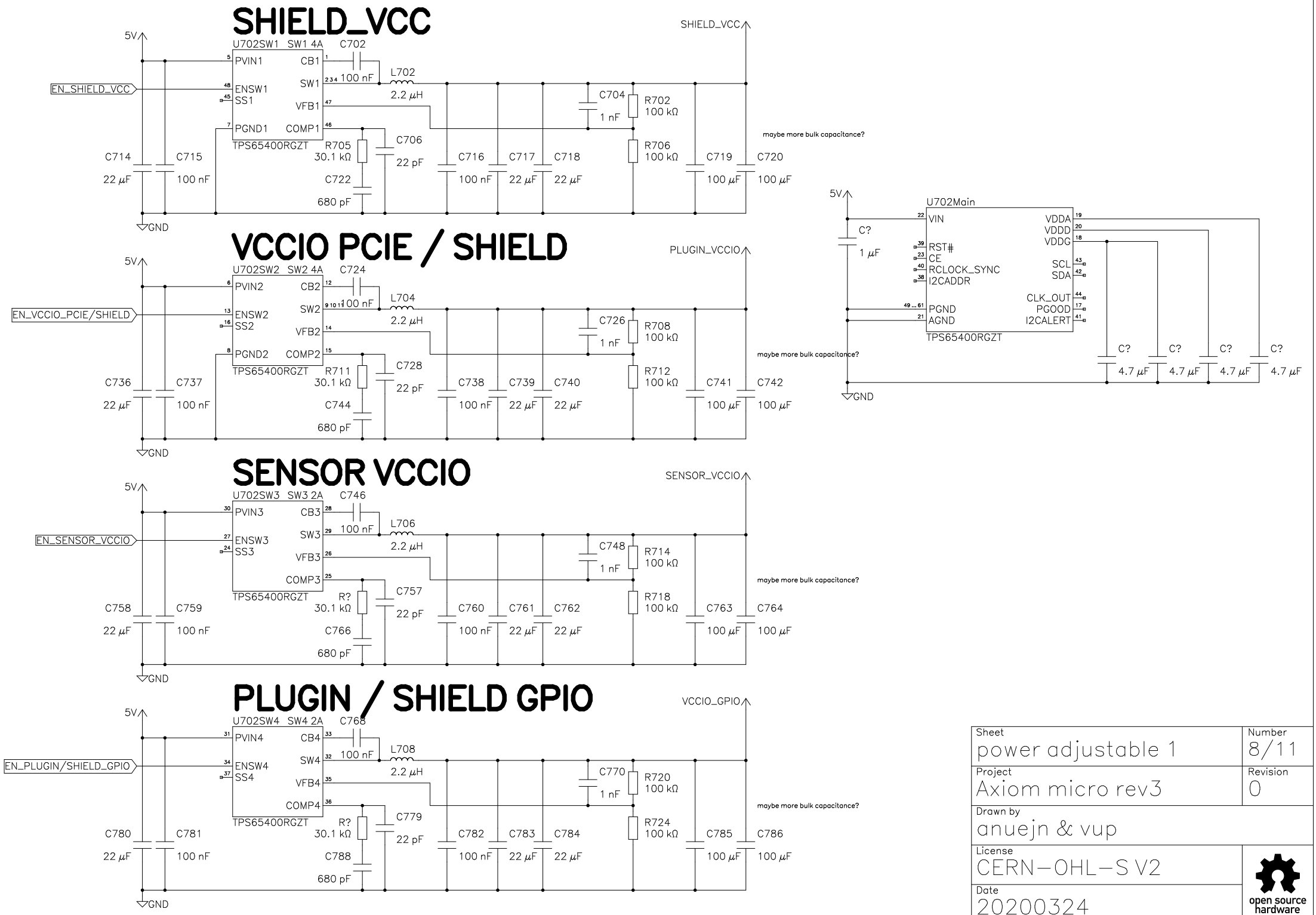

Sheet: power adjustable 1	Number: 8/11
Project: Axiom micro rev3	Revision: 0
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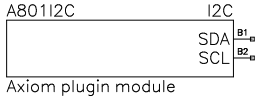

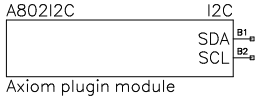

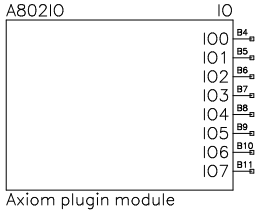

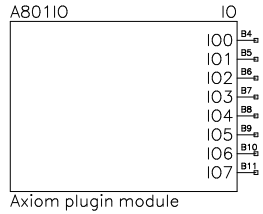

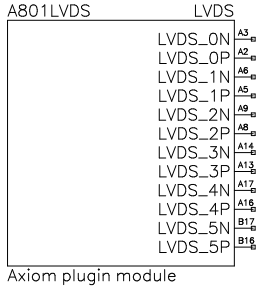

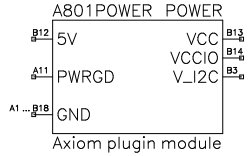

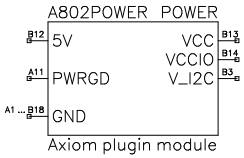

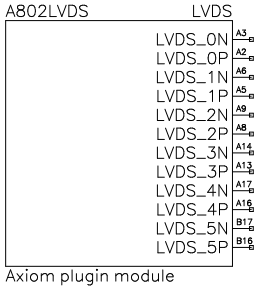

Sheet: image_sensor	Number: 10/12
Project: Axiom micro rev3	Revision: 0
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Sheet shield	Number 11/12
Project Axiom micro rev3	Revision 0
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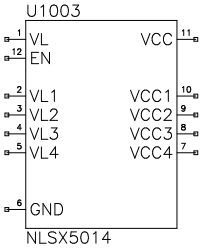

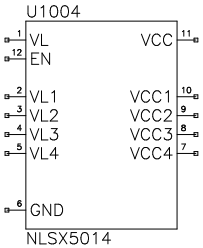

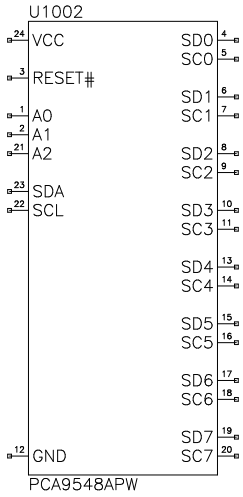

Stuff we want to hang of the i2c mux:
plugin modules
pmic
probably gpio expander for power stuff
????

Sheet: misc	Number: 12/12
Project: Axiom micro rev3	Revision: 0
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