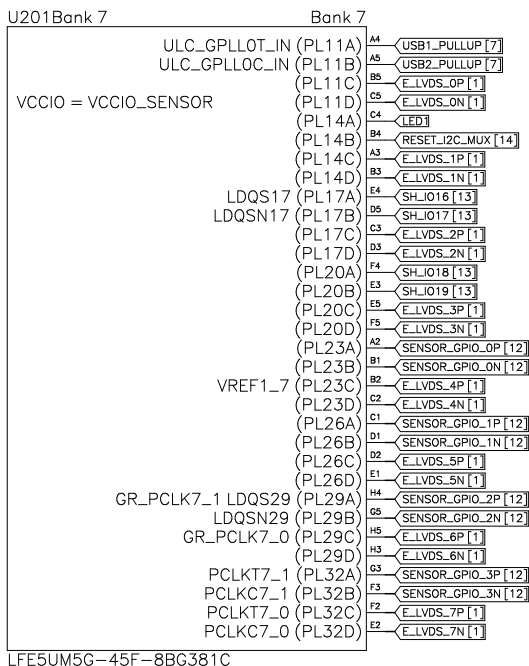
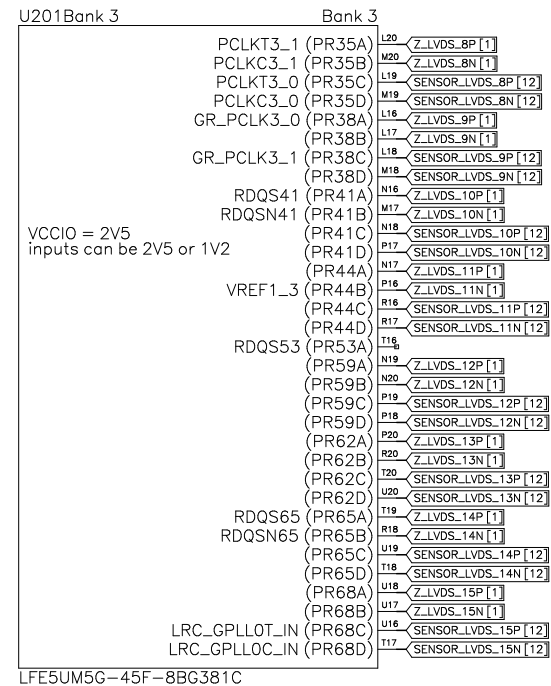
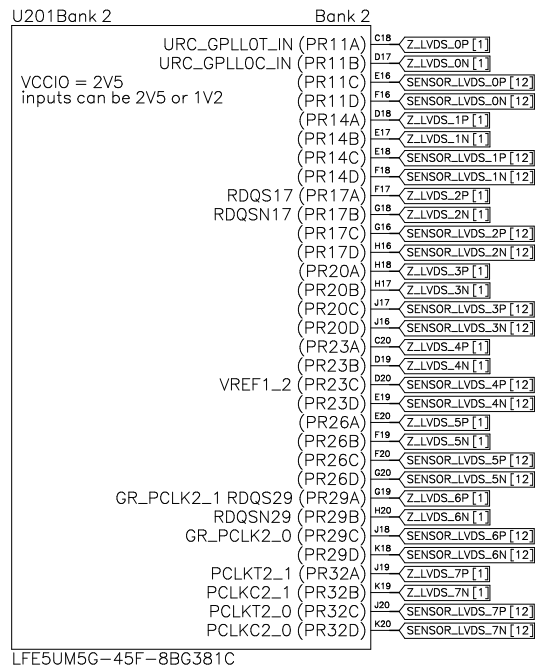
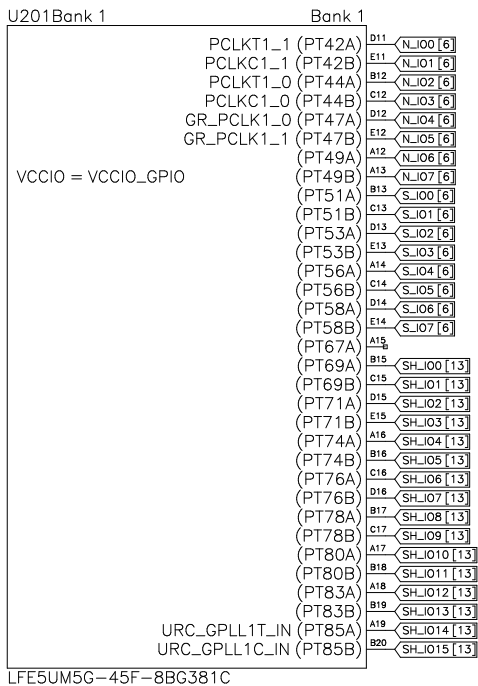
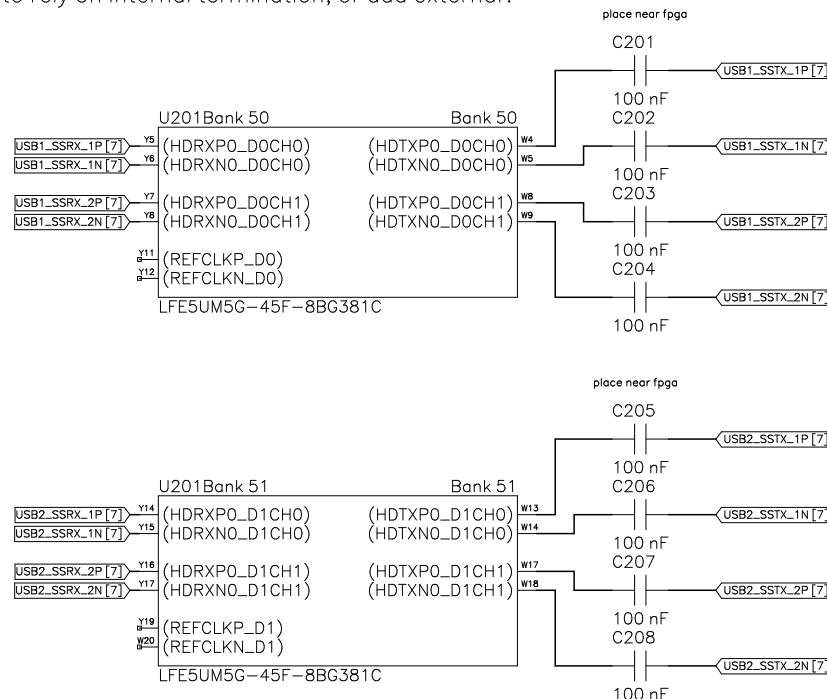


Sheet	Number
zturn lite	1/16
Project	Revision
Axiom micro rev3	0
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20200324	






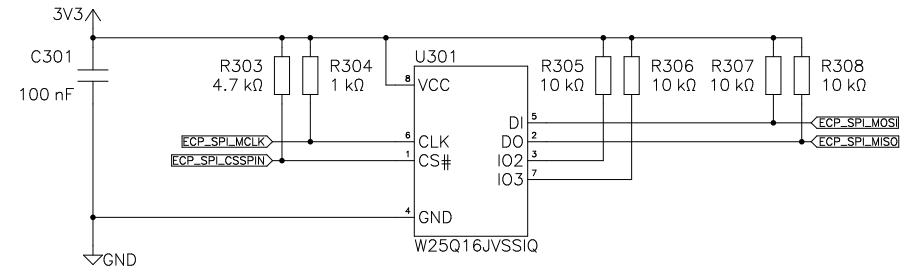
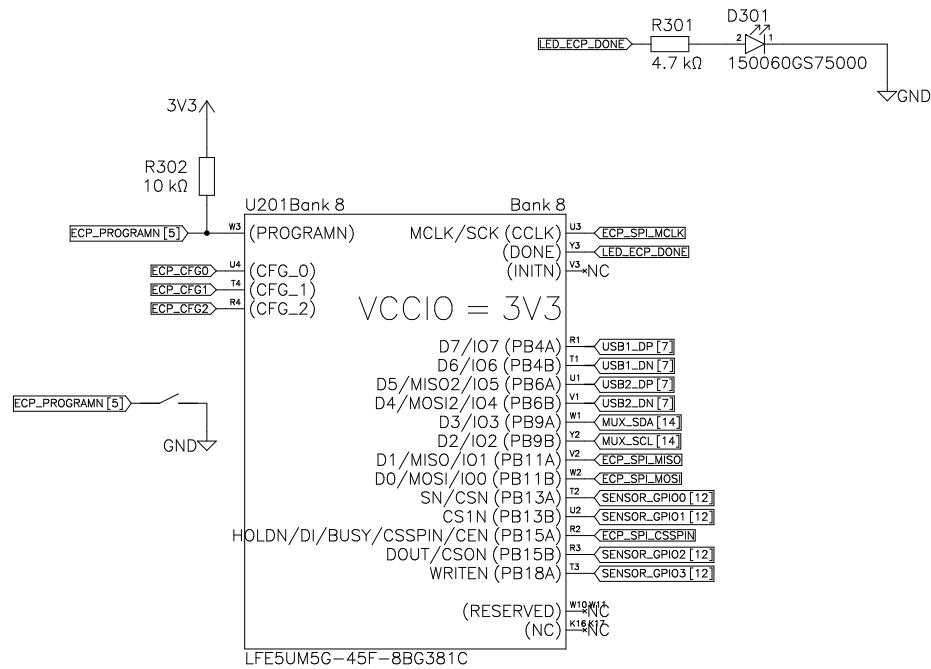
Do we want to rely on internal termination, or add external?



Z\_LVDS goes from ECP to ZYNQ  
E\_LVDS goes from ZYNQ to ECP  
SENSOR\_LVDS goes from sensor board to ECP

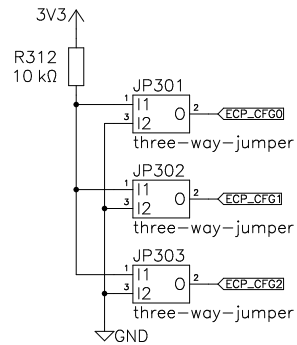


Sheet	Number
ecp	2/16
Project	Revision
Axiom micro rev3	0
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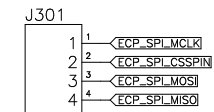
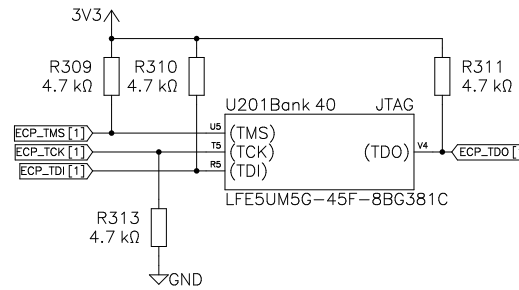


The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI operation. When the QE bit is set to a 0 state (factory default for part numbers with ordering options **TIMT**), the /WP pin and /HOLD are enabled. When the QE bit is set to a 1 (factory default for Quad Enabled part numbers with ordering option **TIOY**), the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled.

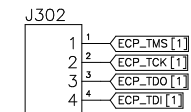
/CS must track VCC during VCC Ramp Up/Down



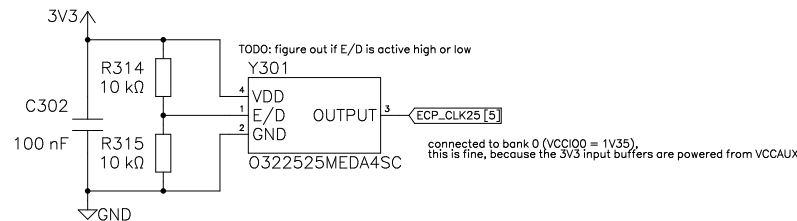
MODE CFG2 CFG1 CFG0  
SSPI 0 0 1 0  
MSPI 0 0 1 0  
SCM 1 1 1 1  
SPCM 1 1 1 1



Generic Pin header 1x4, 2.54mm pitch, vertical



Generic Pin header 1x4, 2.54mm pitch, vertical

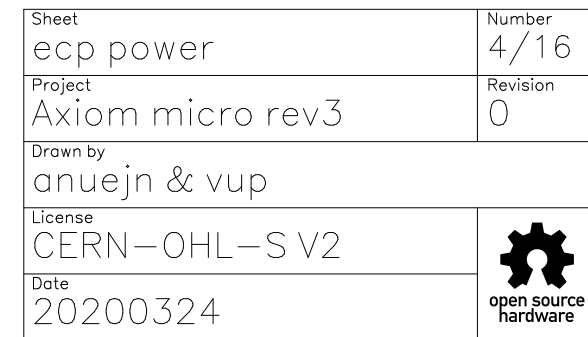
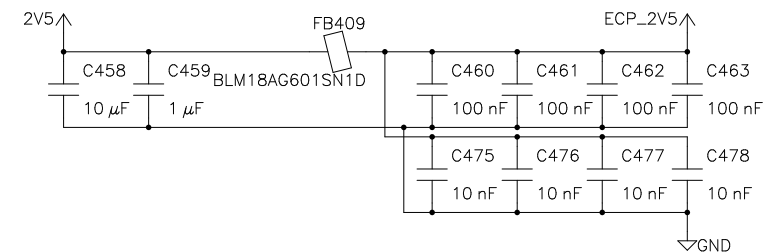
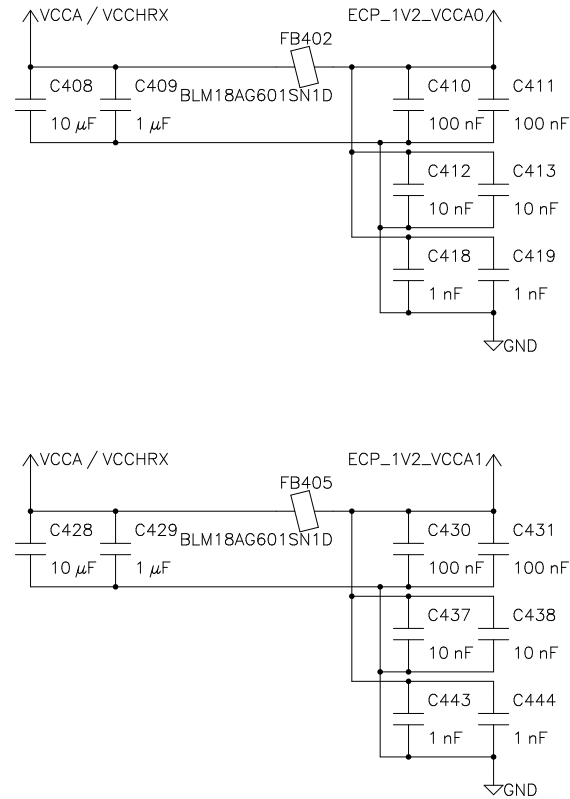
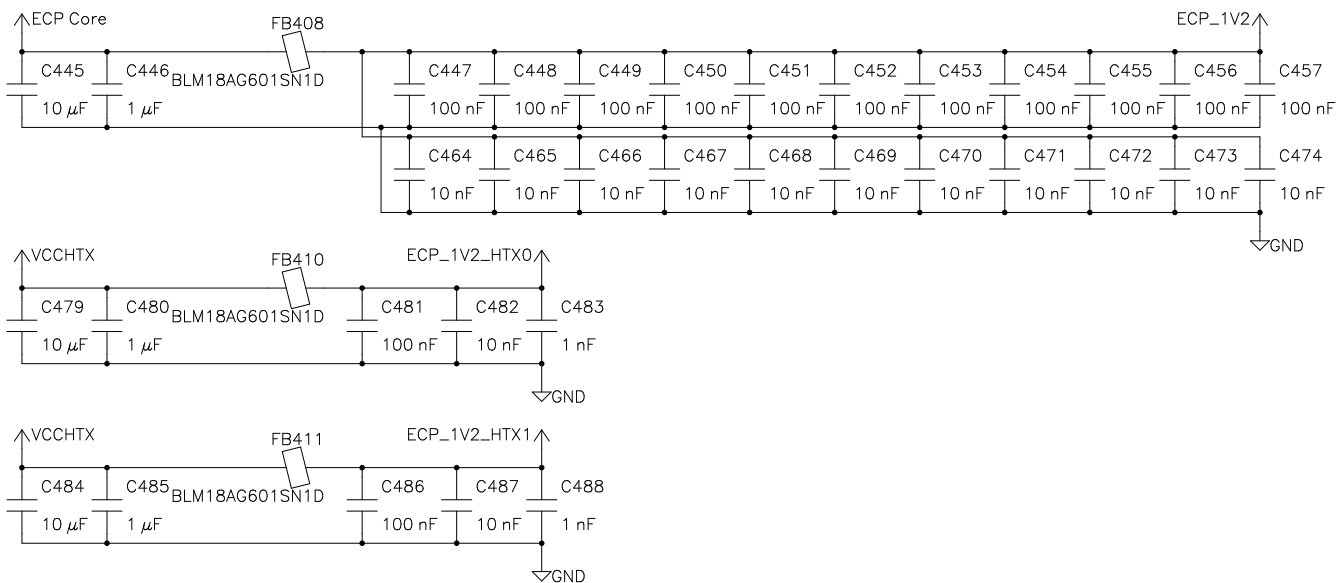


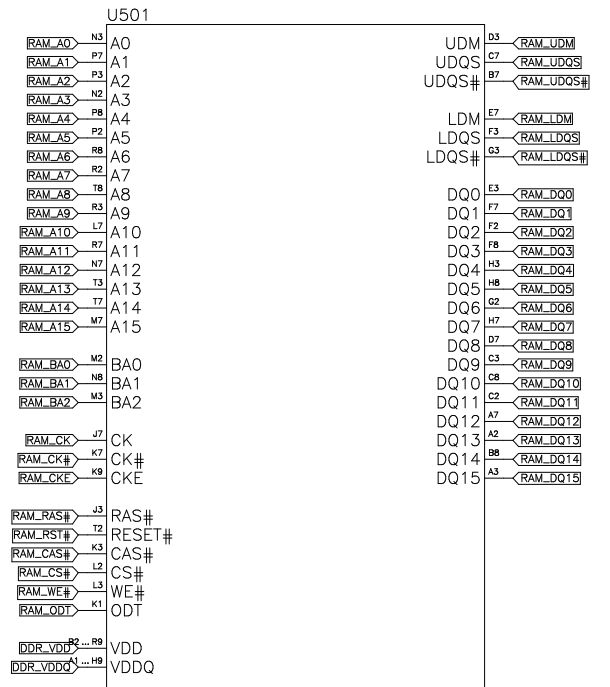
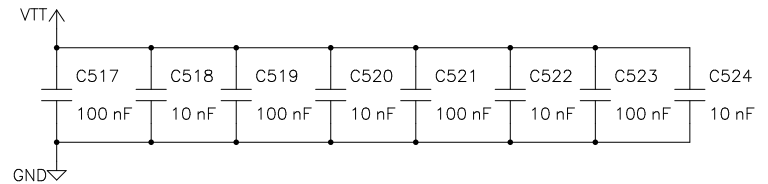
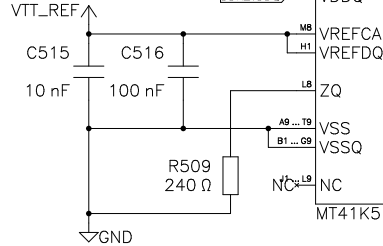
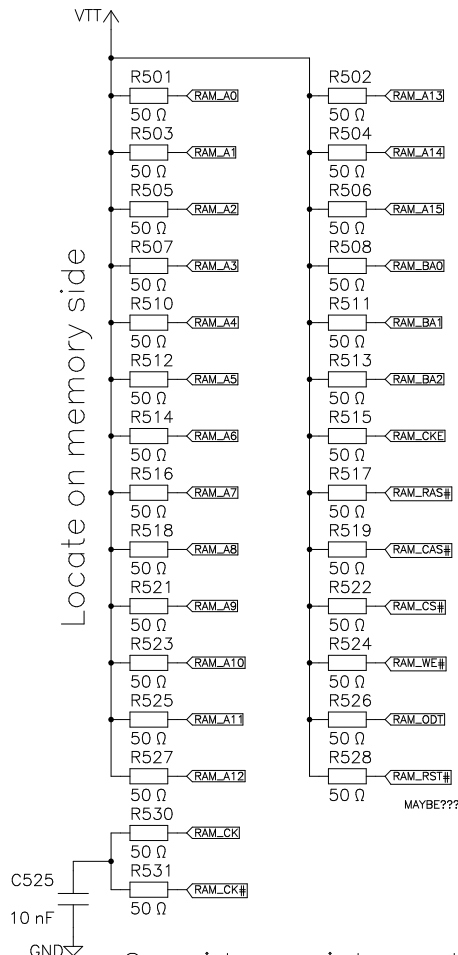
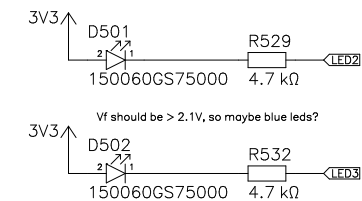
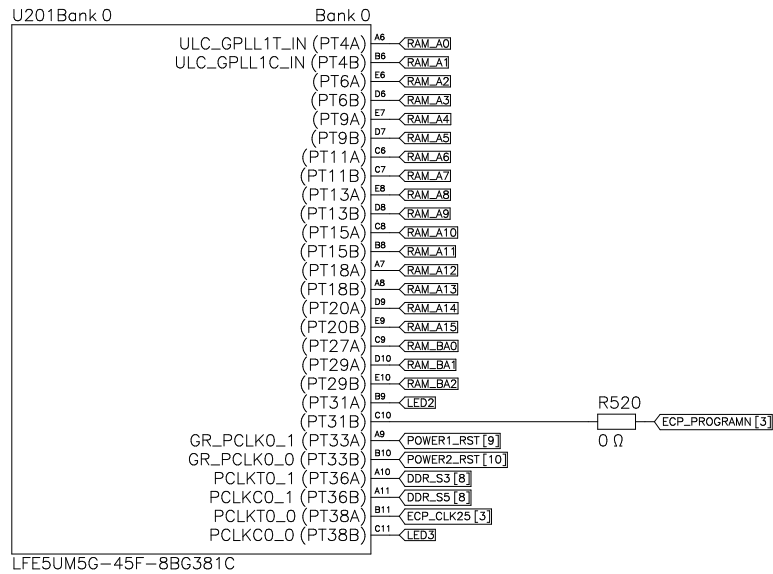
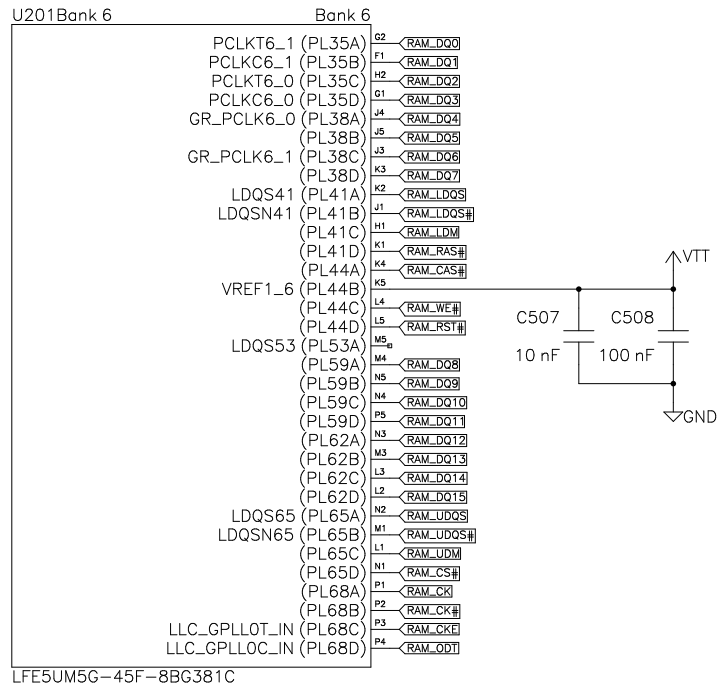
TODD: figure out if E/D is active high or low

connected to bank 0 (VCCIO0 = 1V35), this is fine, because the 3V3 input buffers are powered from VCCAUX

Sheet	Number
ecp config	3/16
Project	Revision
Axiom micro rev3	0
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Sheet	RAM	Number	5/16
Project	Axiom micro rev3	Revision	0
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Date	20200324		

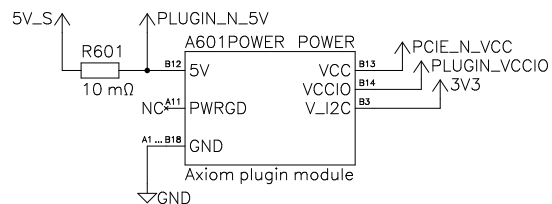
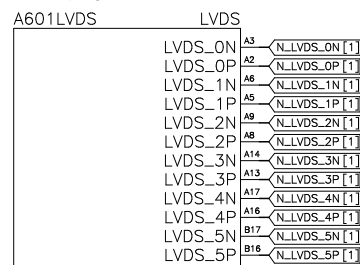
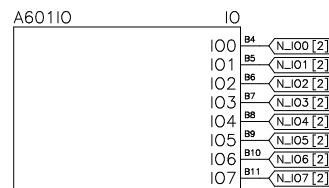


Consider resistor networks?

A601I2C I2C

SDA B1 N\_SDA [14]

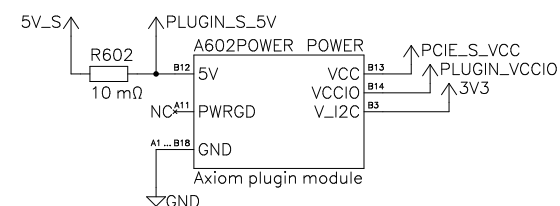
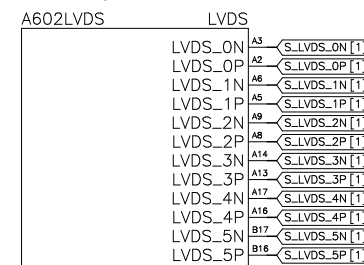
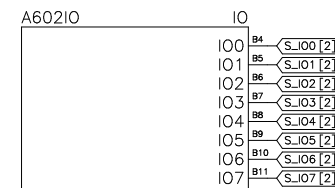
SCL B2 N\_SCL [14]



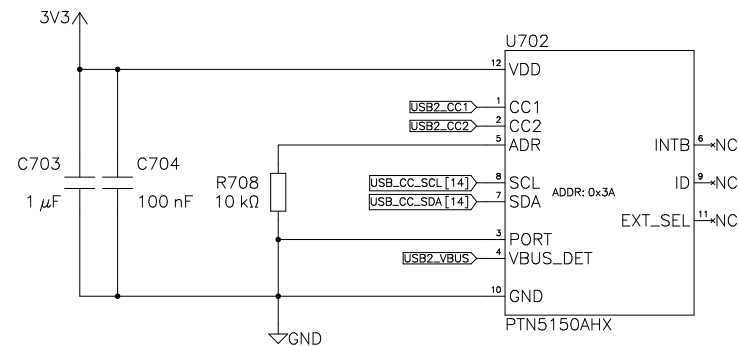
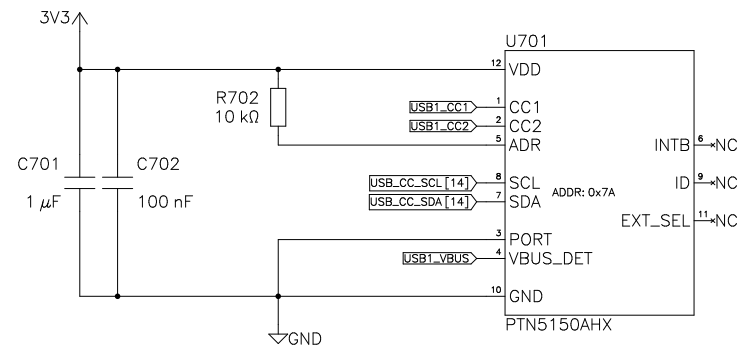
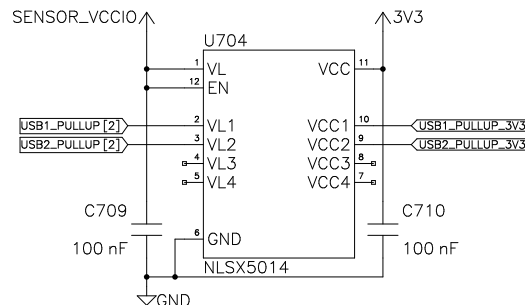
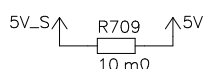
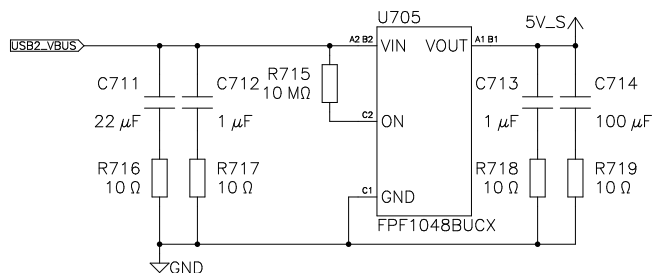
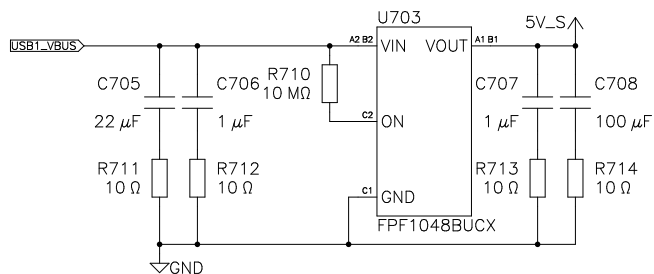
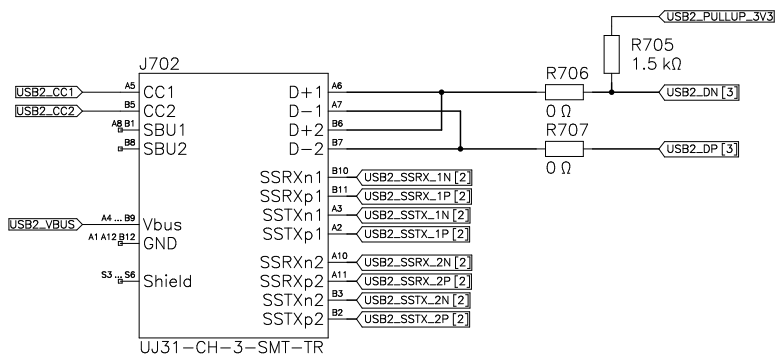
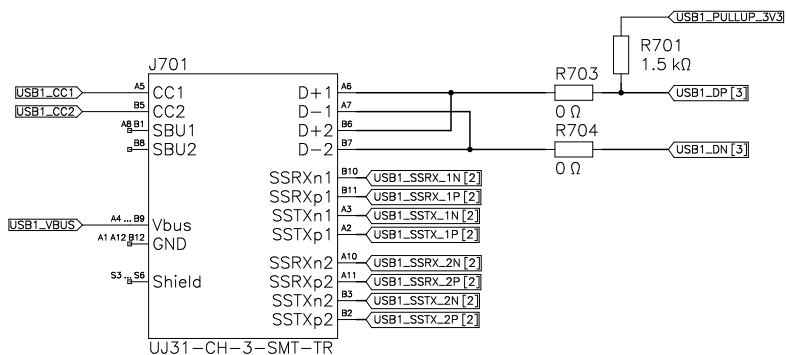
A602I2C I2C

SDA B1 S\_SDA [14]

SCL B2 S\_SCL [14]



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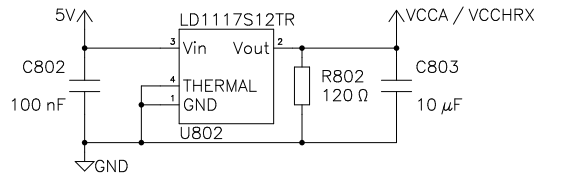


PORT= VDD: DFP mode ( $R_p = 80\mu A$  power default for non-I2C mode).  
 PORT= Mid (or floating): DRP mode  
 PORT= GND: UFP mode

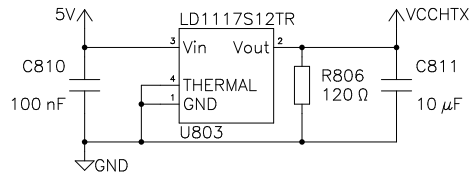
Trinary GPIO Input ADDR pin run from VDD  
 - ADDR pull up to VDD with 10 k $\Omega$  resistor (I2C Enabled with ADDR bit 6 equal to 1, I2C Address 0x7A)  
 - ADDR pull down to GND with 10 k $\Omega$  resistor. (I2C Enabled with ADDR bit 6 equal to 0, I2C Address 0x3A)  
 - ADDR = Mid or floating (Pin 6/7/8) configured as OUT1/2/3 in non-I2C mode

Sheet	Number
USB	7/16
Project	Revision
Axiom micro rev3	0
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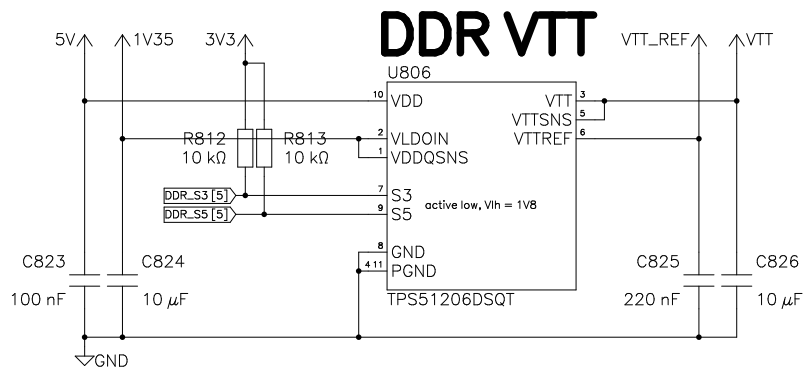




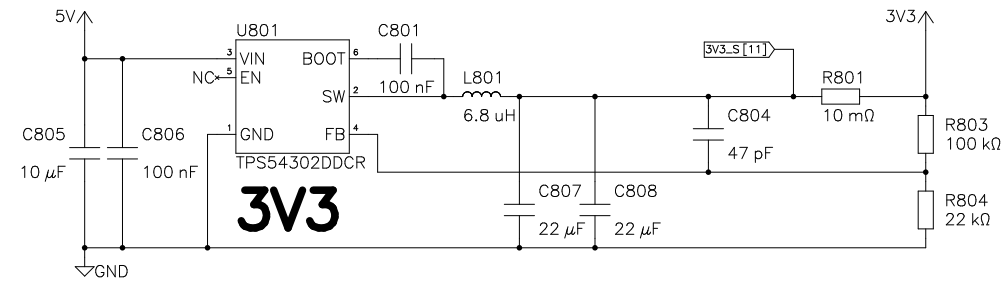
# 1V2 VCCA / VCCHRX



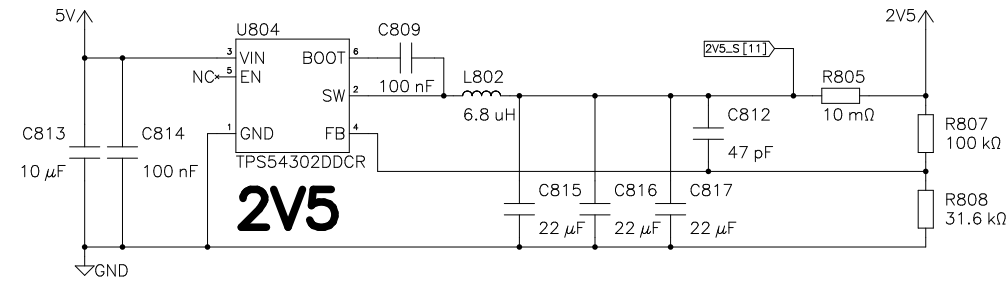
# 1V2 VCCHTX



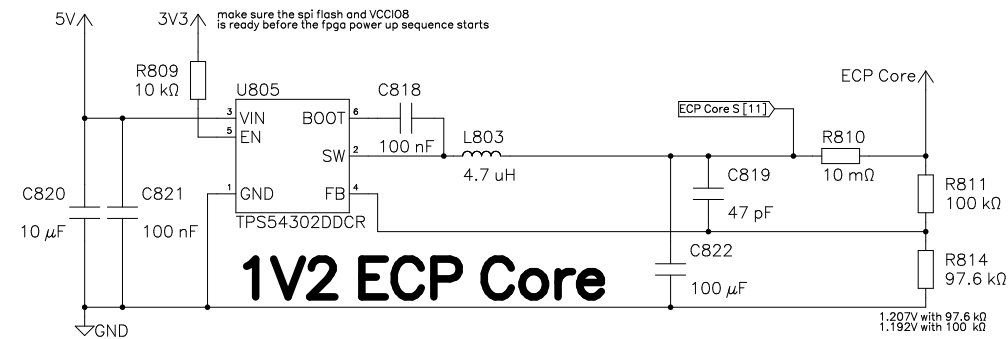
positive terminal of the VTT pin output capacitor(s) as a separate trace from the high-current path from VTT. Consider adding a low-pass R-C filter at the VTTSENS pin in case the ESR of the VTT output capacitor(s) is larger than 2 mΩ. The R-C filter time constant should be approximately the same or slightly lower than the time constant of the VTT output capacitance and ESR.



# 3V3



# 2V5

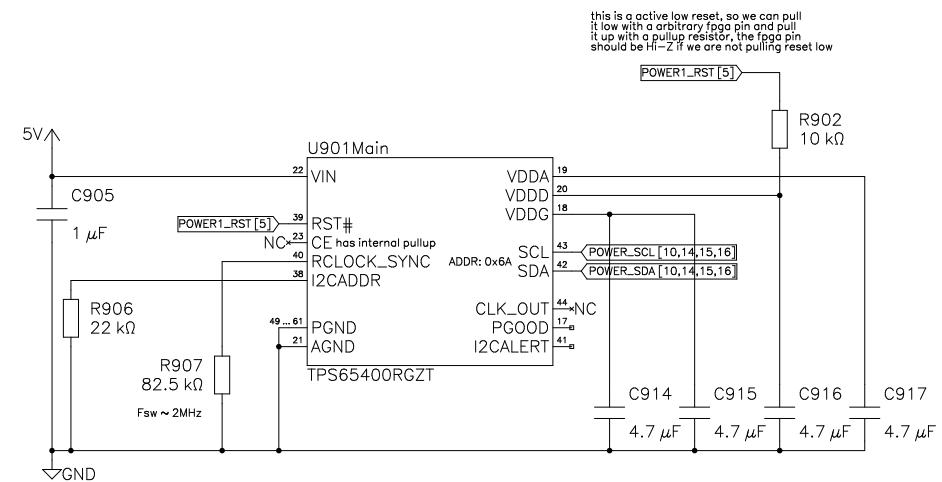


# 1V2 ECP Core

Sheet	power fixed	Number	8/16
Project	Axiom micro rev3	Revision	0
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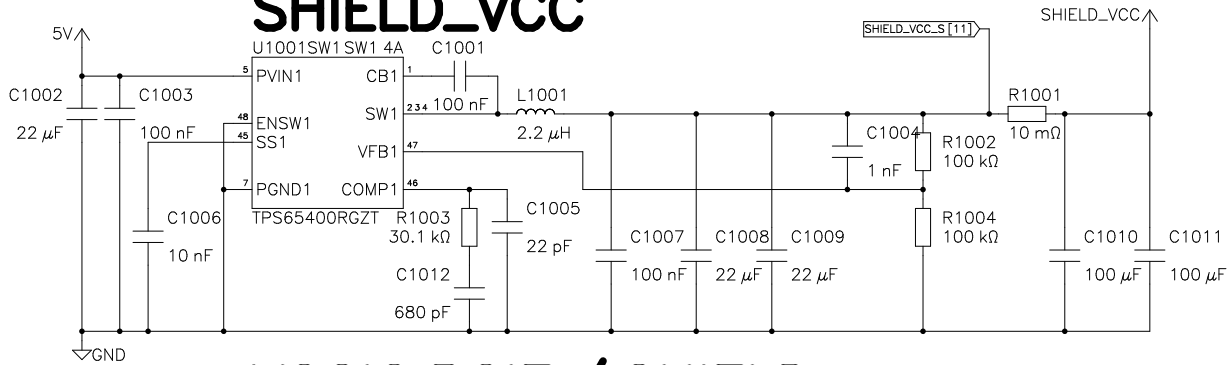
[illegible]

all rails apart from the one use for jtag are disabled by default (as we need to setup the voltages on the first start)

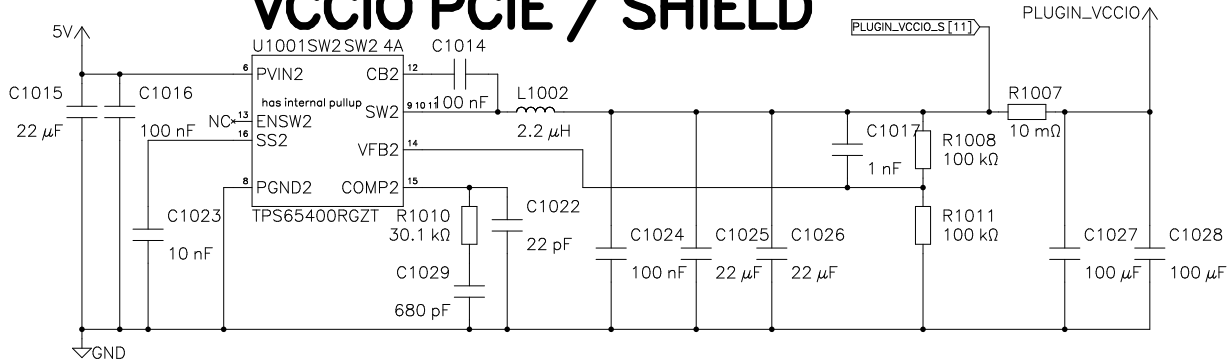
soft start caps:  $10\text{nF} / 5\mu\text{A} * 0.8\text{V} = 1.6\text{ms}$   
for ECP: max  $10\text{V/ms}$  slew rate

Sheet power adjustable 1	Number 9/16
Project Axiom micro rev3	Revision 0
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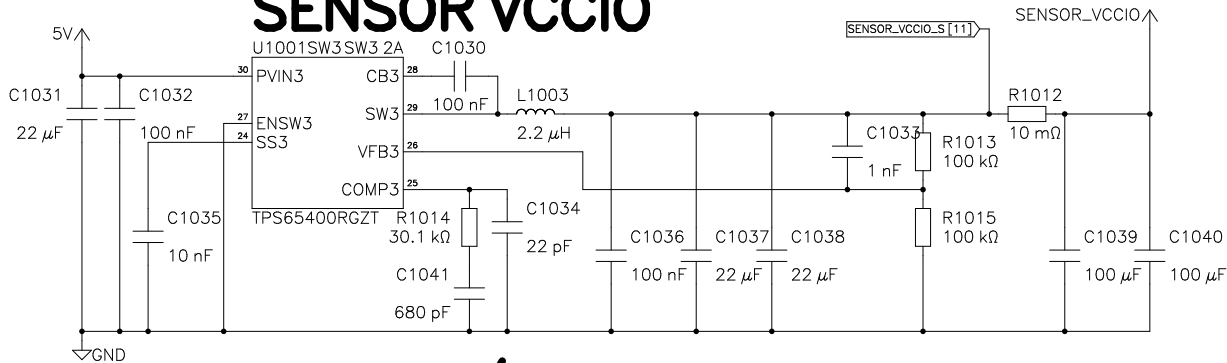
# SHIELD\_VCC



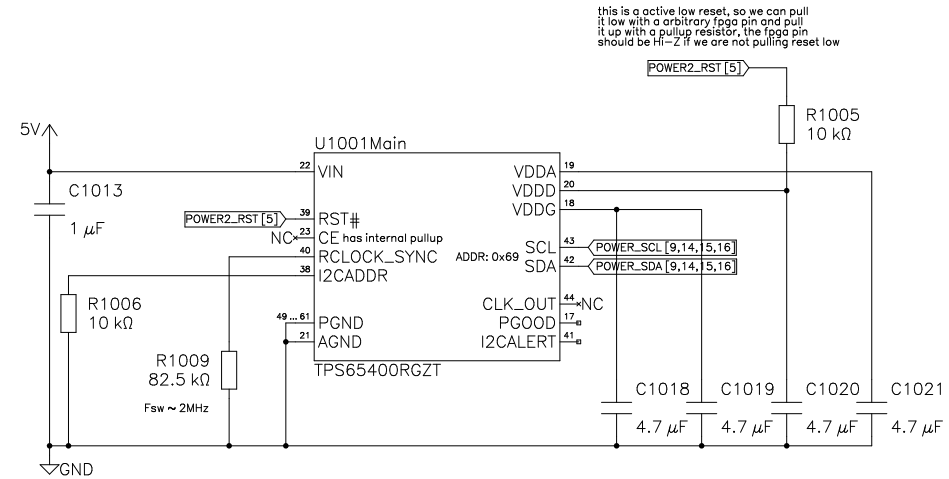
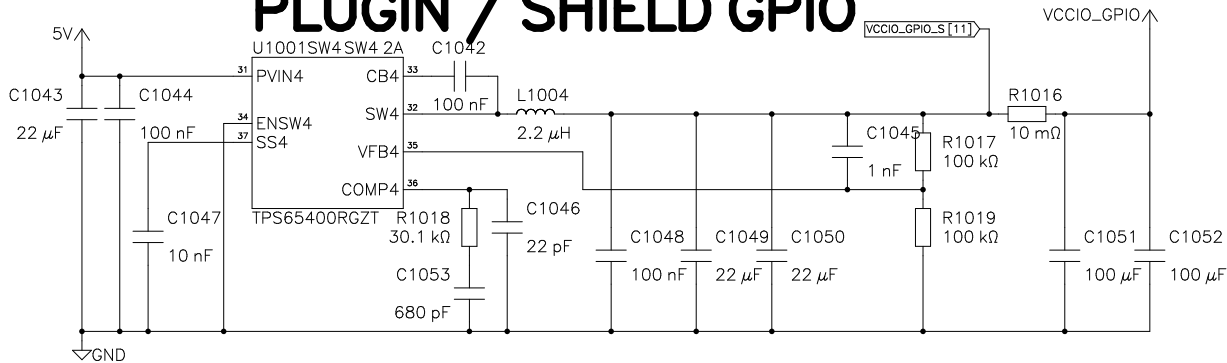
# VCCIO PCIE / SHIELD



# SENSOR VCCIO




# PLUGIN / SHIELD GPIO

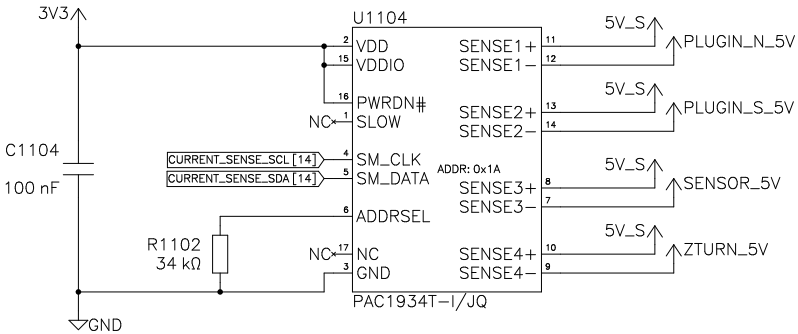
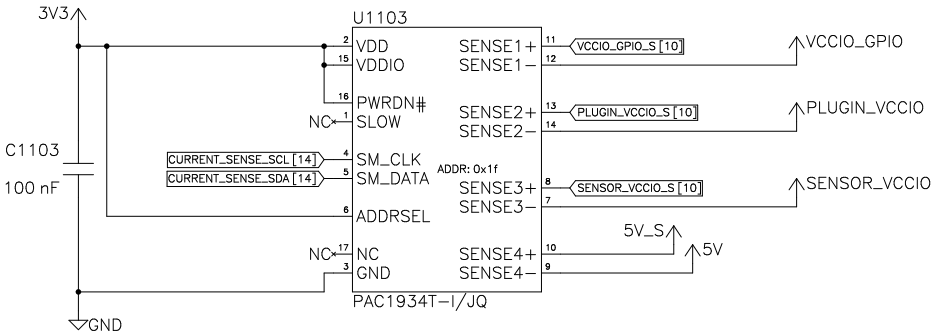
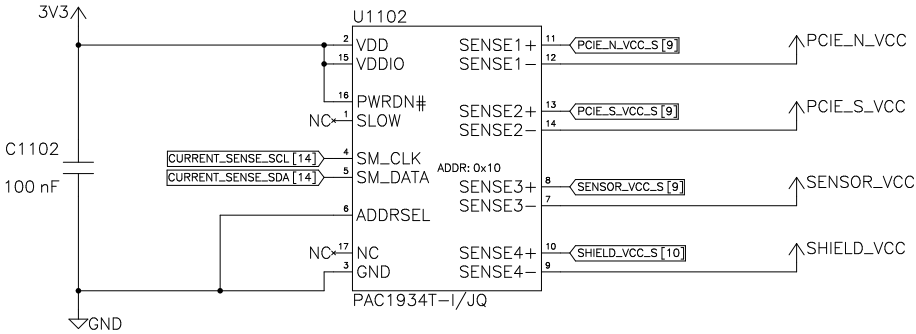
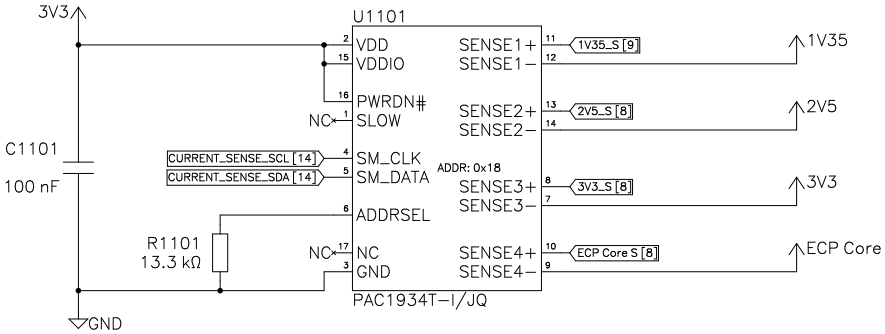


Because JTAG is driven from PLUGIN\_VCCIO we somehow need to enable that one before ever being able to access the i2c bus.

The default for the internal Vref is 0.8V, so we get a output voltage of  $0.8V * (1 + 100k / 100k) = 1.6V$   
 That should work for jtag (its shifted to 3v3 with a level shifter)  
 ENSWx have internal pullups, to the rails are enabled by default  
 This pullup can later be overridden by using some i2c commands.  
 (We want to be able to do that to not damage the plugin modules, that get a direct link to this rail)

Sheet	power adjustable 2	Number	10/16
Project	Axiom micro rev3	Revision	0
Drawn by	anuejn & vup		
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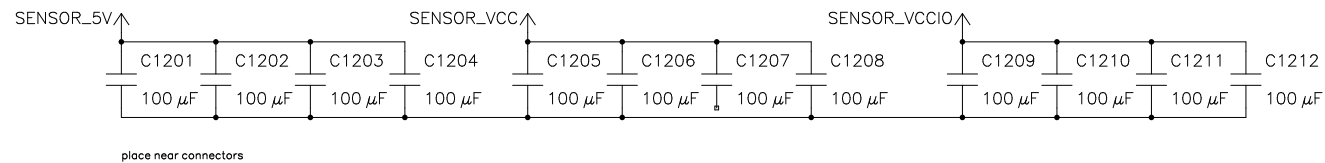
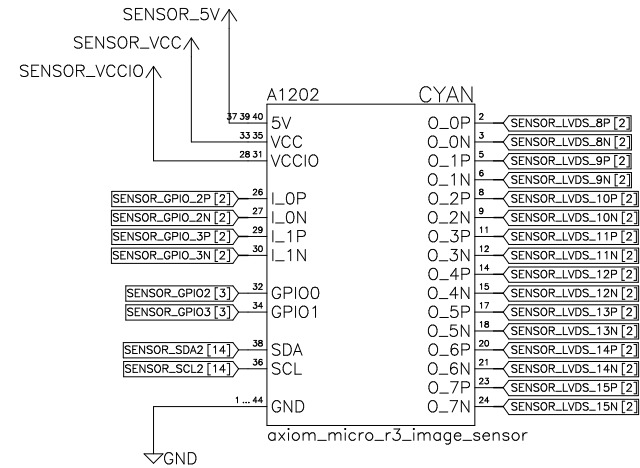
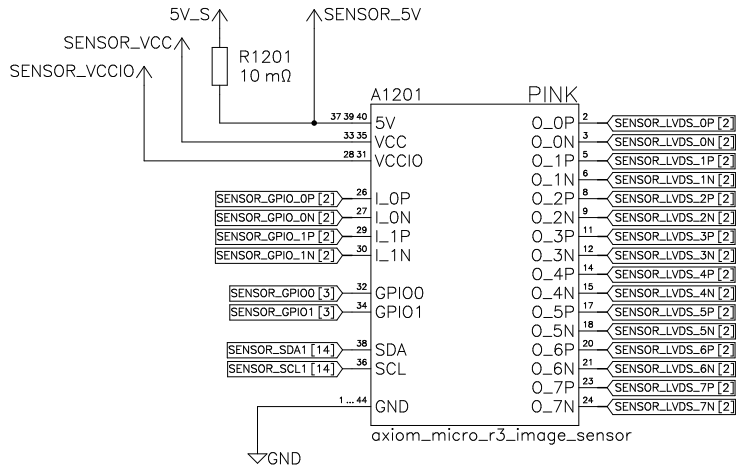
current sense resistors: 0805W8F100MT5E or CS05W8F100MT5E




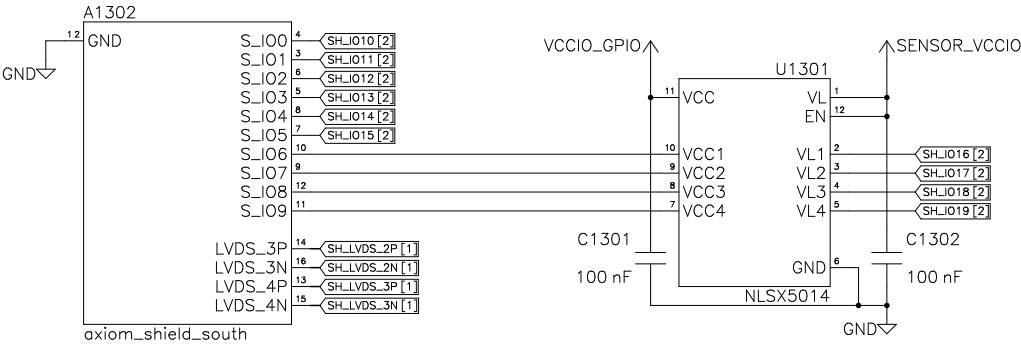
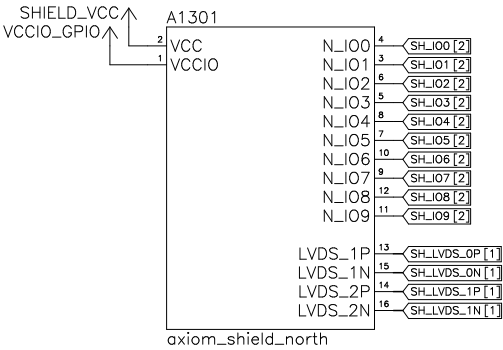
Sheet	Number
current sense	11/16
Project	Revision
Axiom micro rev3	0
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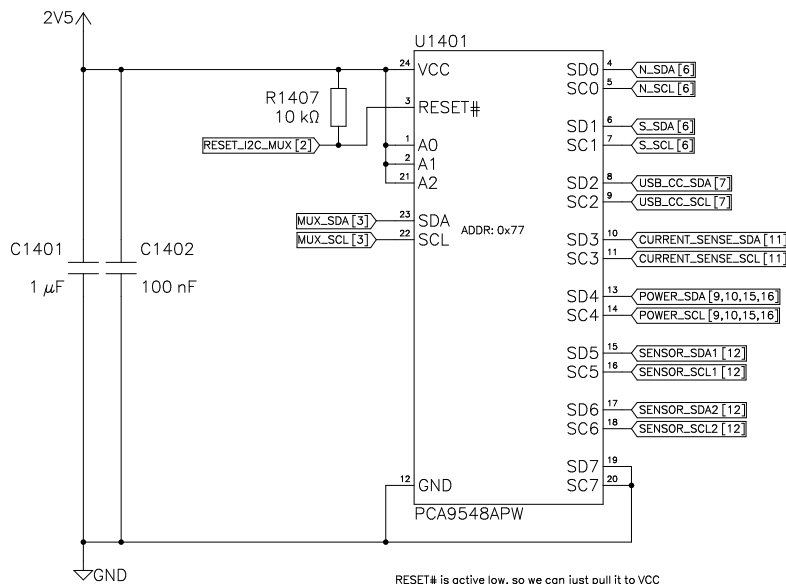
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Sheet	image sensor	Number	12/16
Project	Axiom micro rev3	Revision	0
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Sheet	shield	Number	13/16
Project	Axiom micro rev3	Revision	0
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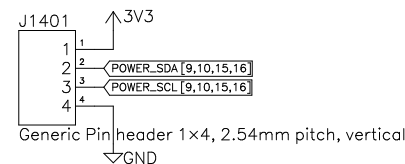
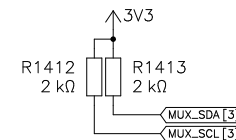
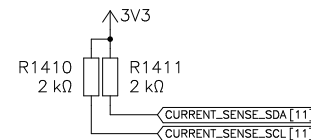
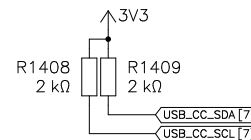
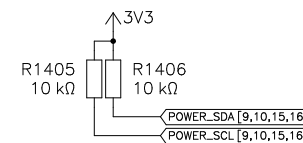
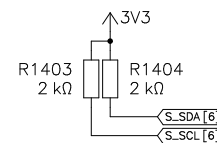
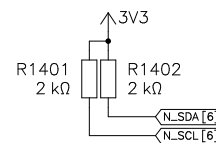


RESET# is active low, so we can just pull it to VCC  
and then pull it to GND using any VCCIO from the ECP,  
attention has to be paid to not make RESET# get over VCC,  
as otherwise current flows from the RESET pin to the VCC pin,  
this should be accomplishable by just making the fpga output Hi-Z  
if it is not pulien low

2V5 VCC means about 1V8 voltage clamping by the pass through transistors  
That should work for most applications, we just need to be careful with nothing with 1V2 is on the bus

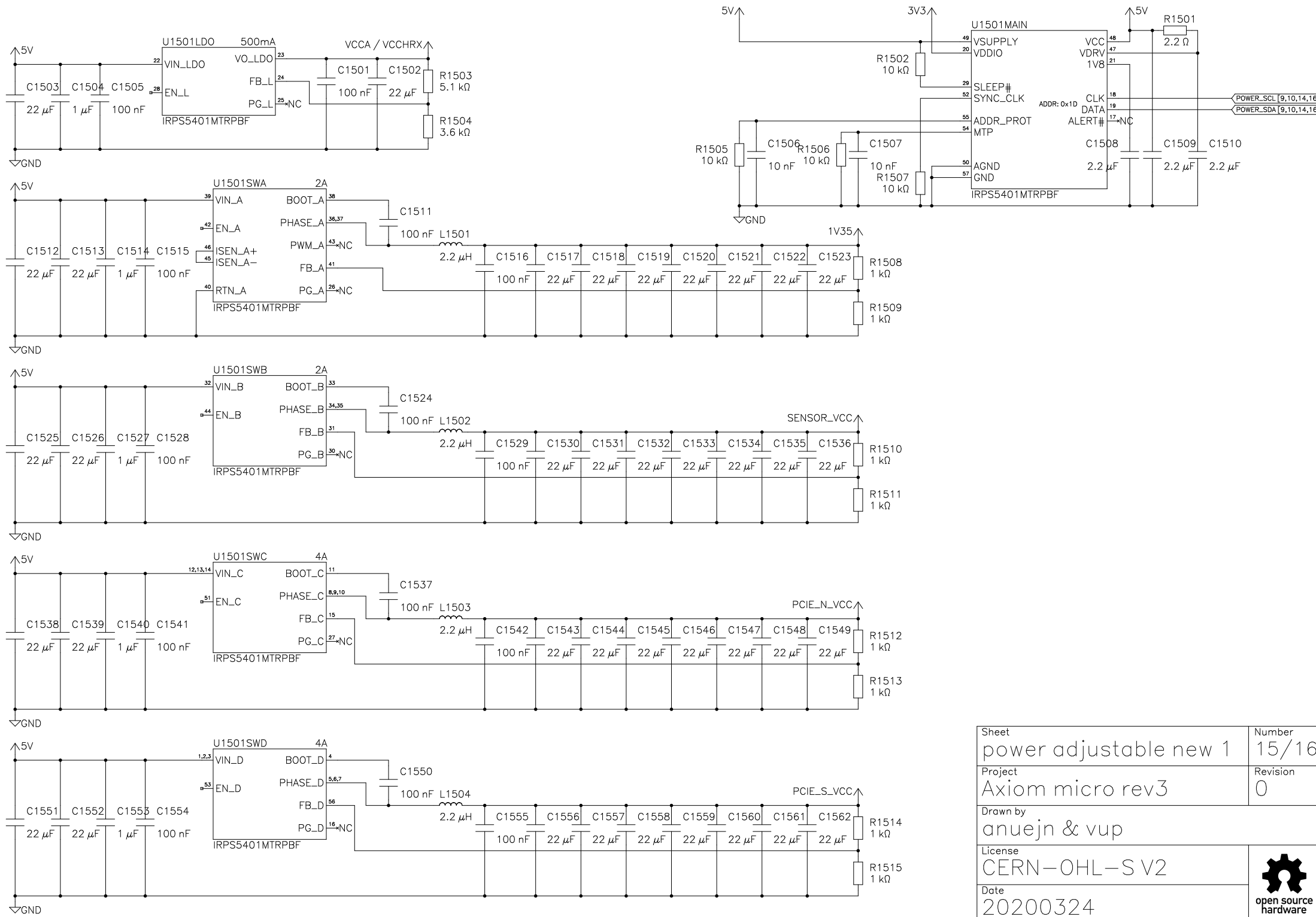
Unused channels have to be tied to GND or VCC


No pullups for these two,  
as we don't know their voltage

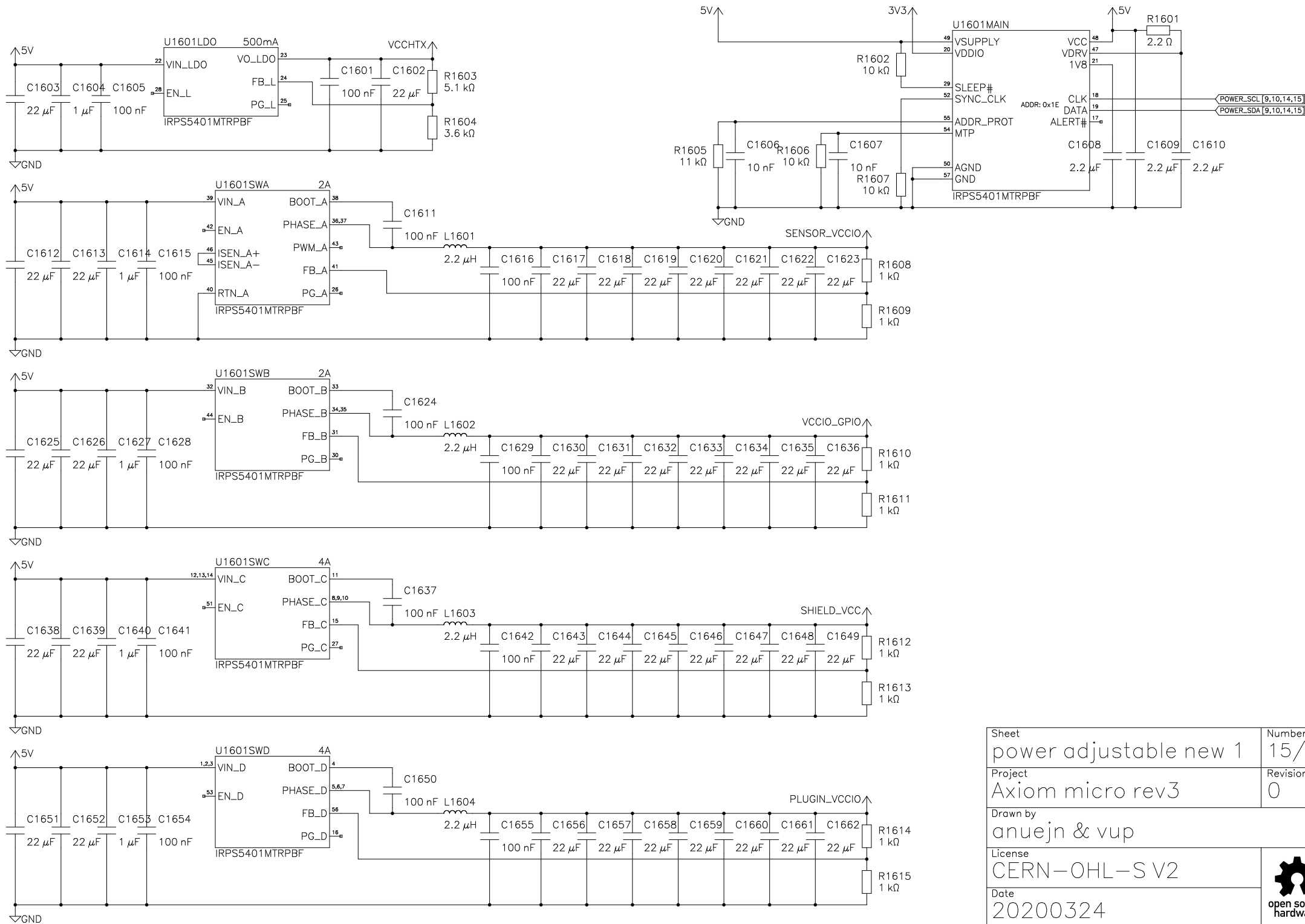


Sheet	Number
i2c mux	14/16
Project	Revision
Axiom micro rev3	0
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Sheet	power adjustable new 1	Number	15/16
Project	Axiom micro rev3	Revision	0
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Sheet	power adjustable new 1	Number	15/16
Project	Axiom micro rev3	Revision	0
Drawn by	anuejn & vup		
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