
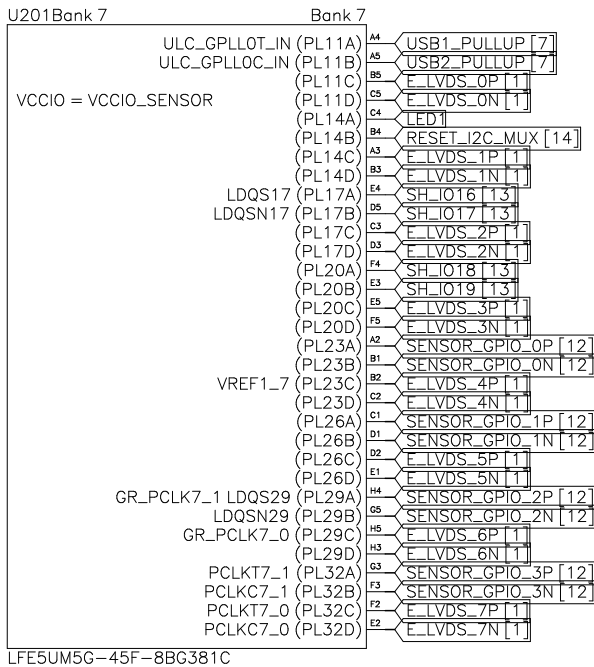
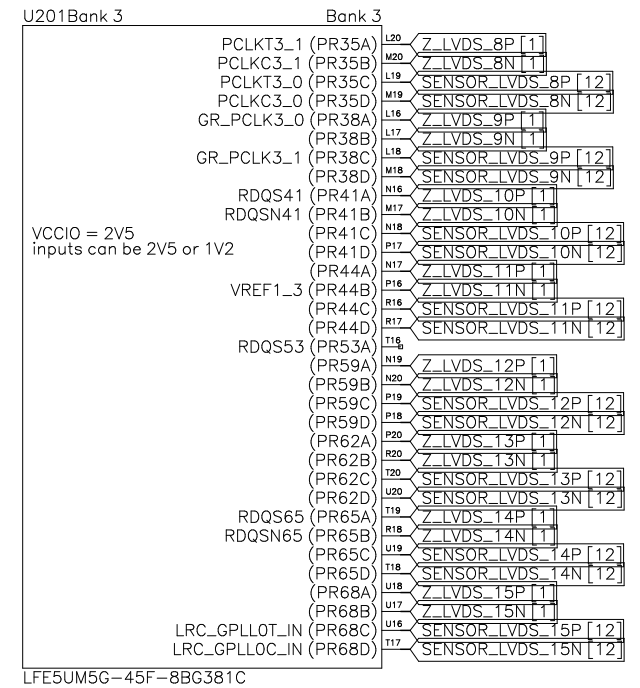
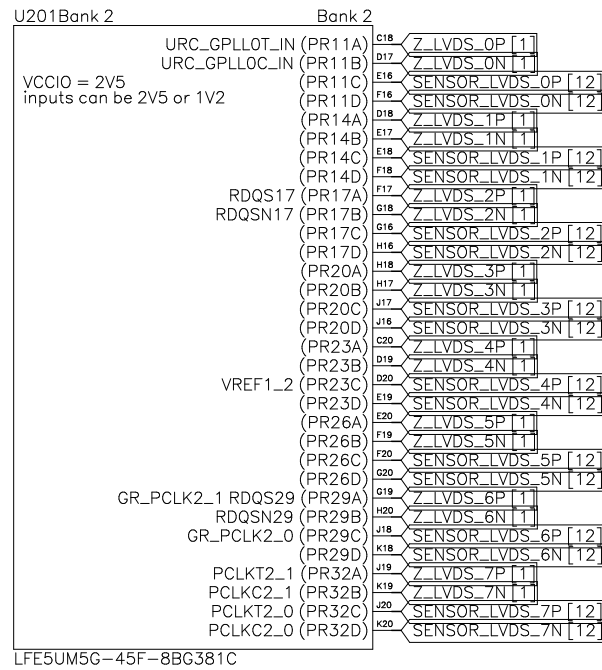
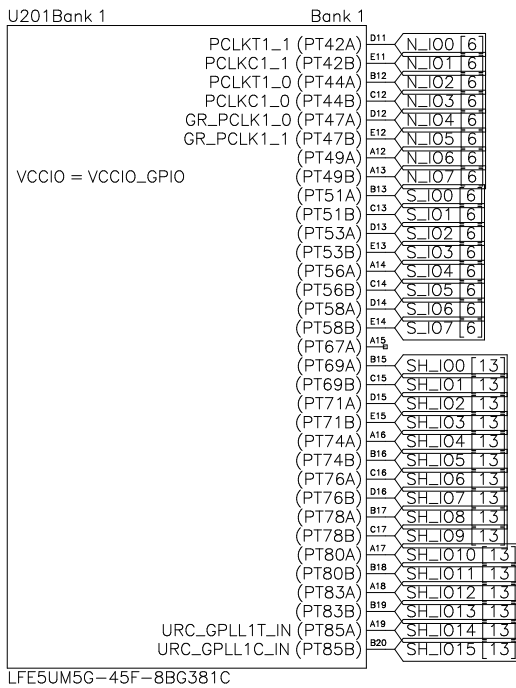
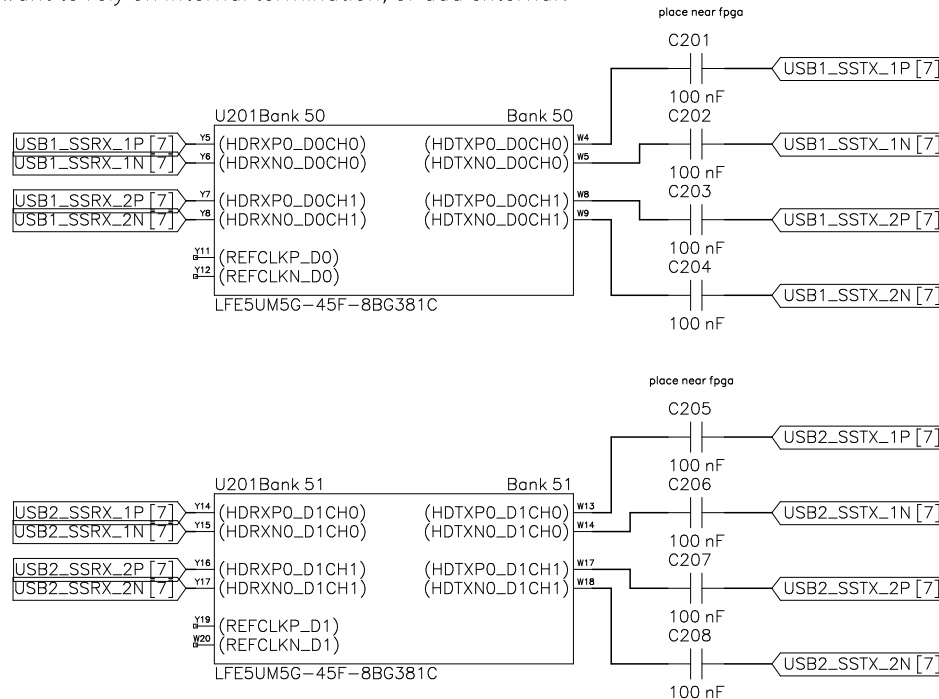


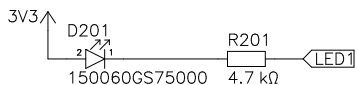
Sheet	zturn lite	Number	1/14
Project	Axiom micro rev3	Revision	0
Drawn by	anuejn & vup		
License	CERN-OHL-S V2		
Date	20200324		



Do we want to rely on internal termination, or add external?

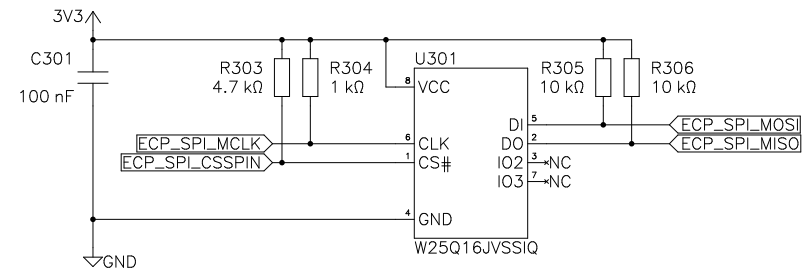
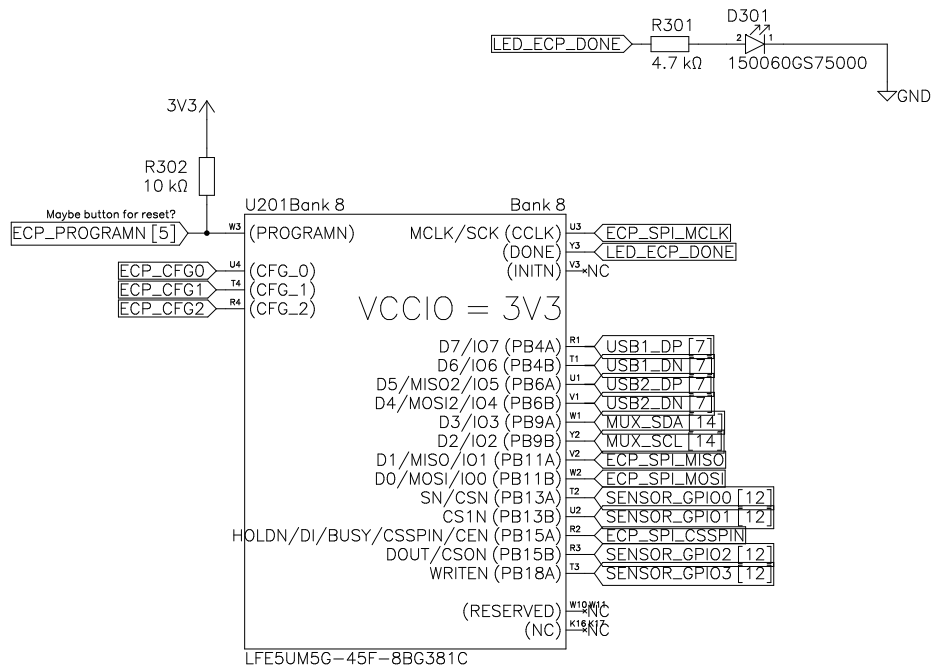


Z_LVDS goes from ECP to ZYNQ
F_LVDS goes from ZYNQ to ECP
SENSOR_LVDS goes from sensor board to ECP



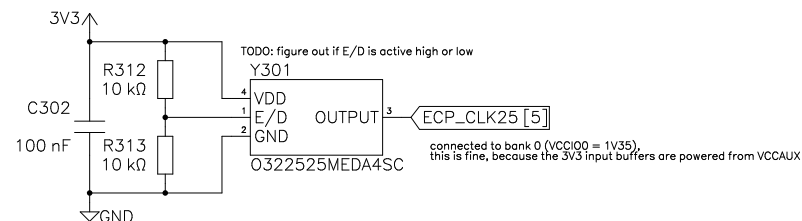
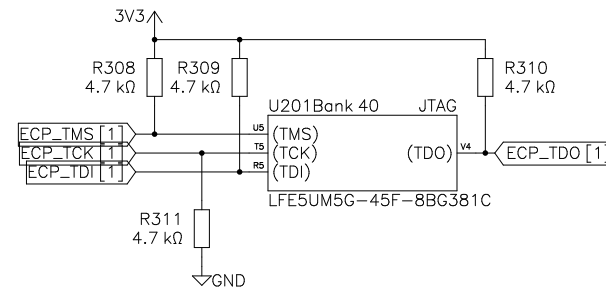
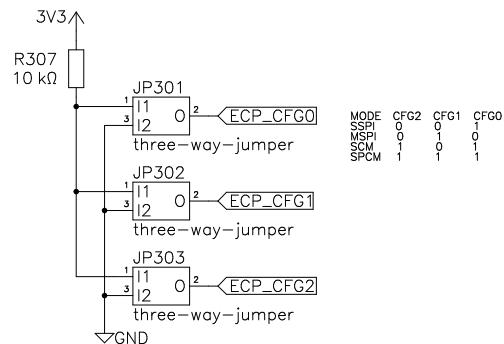
Sheet	Number
ecp	2/14
Project	Revision
Axiom micro rev3	0
Drawn by	
anuejn & vup	
License	
CERN-OHL-S V2	
Date	
20200324	





The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI operation. When the QE bit is set to a 0 state (factory default for part numbers with ordering options **TIMT**), the /WP pin and /HOLD are enabled. When the QE bit is set to a 1 (factory default for Quad Enabled part numbers with ordering option **TIGT**), the Quad I02 and I03 pins are enabled, and /WP and /HOLD functions are disabled.

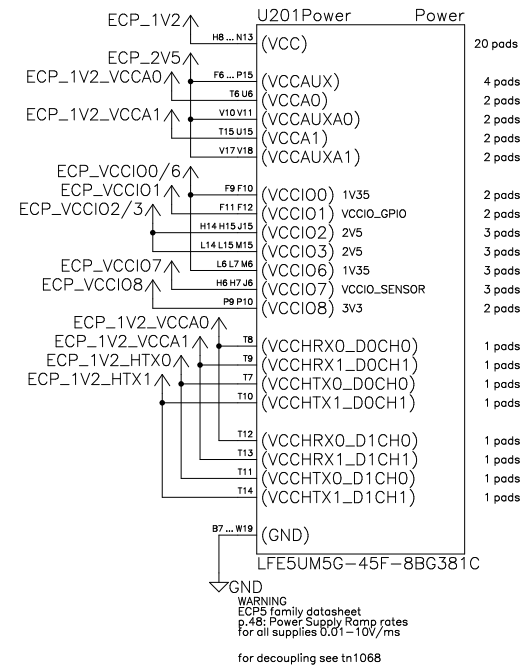
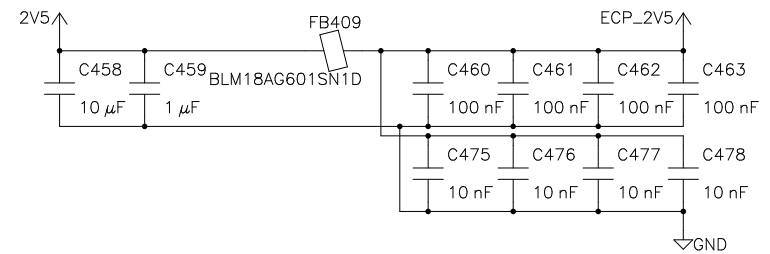
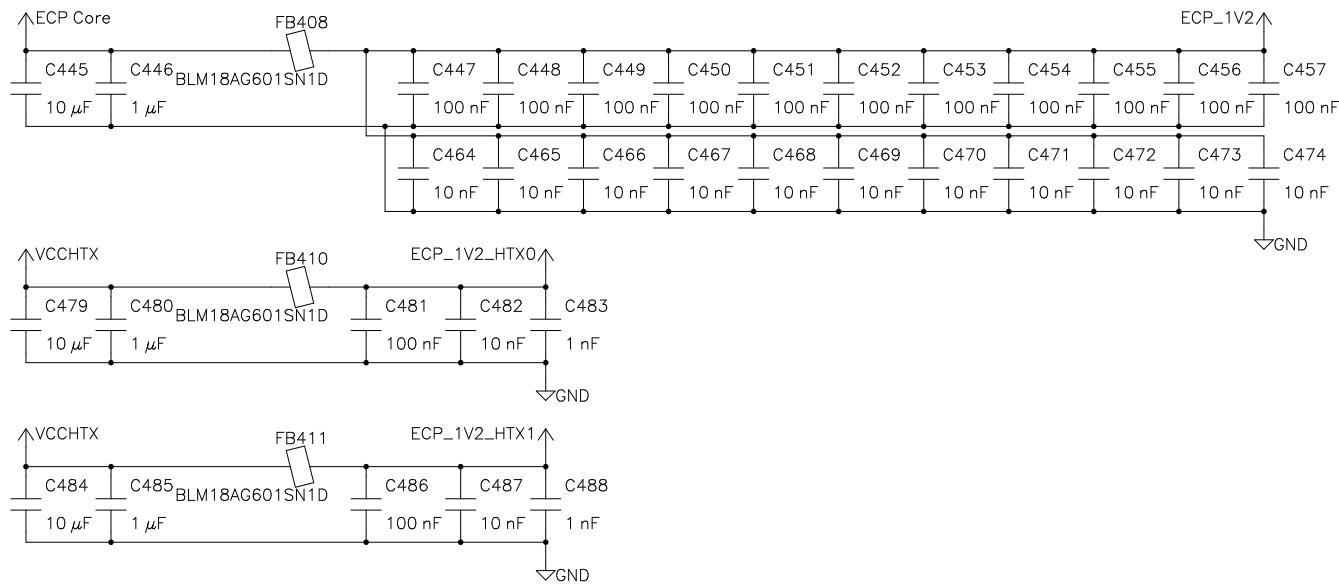
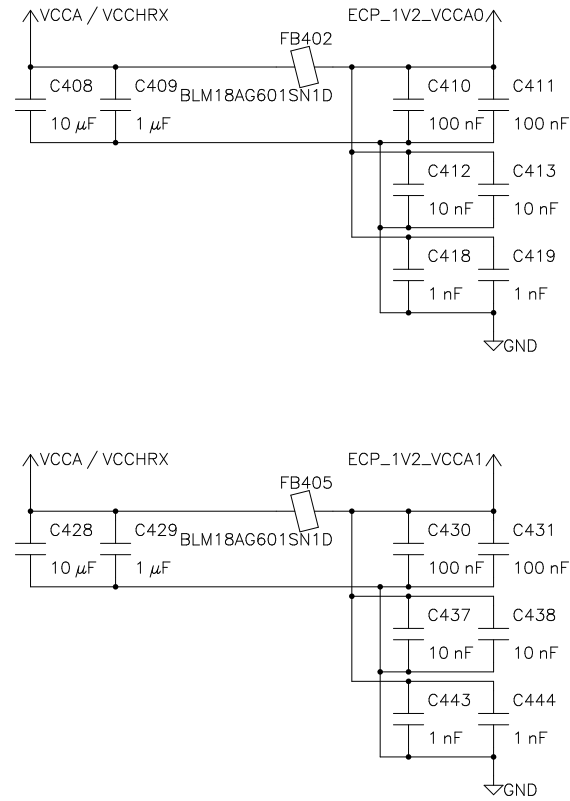
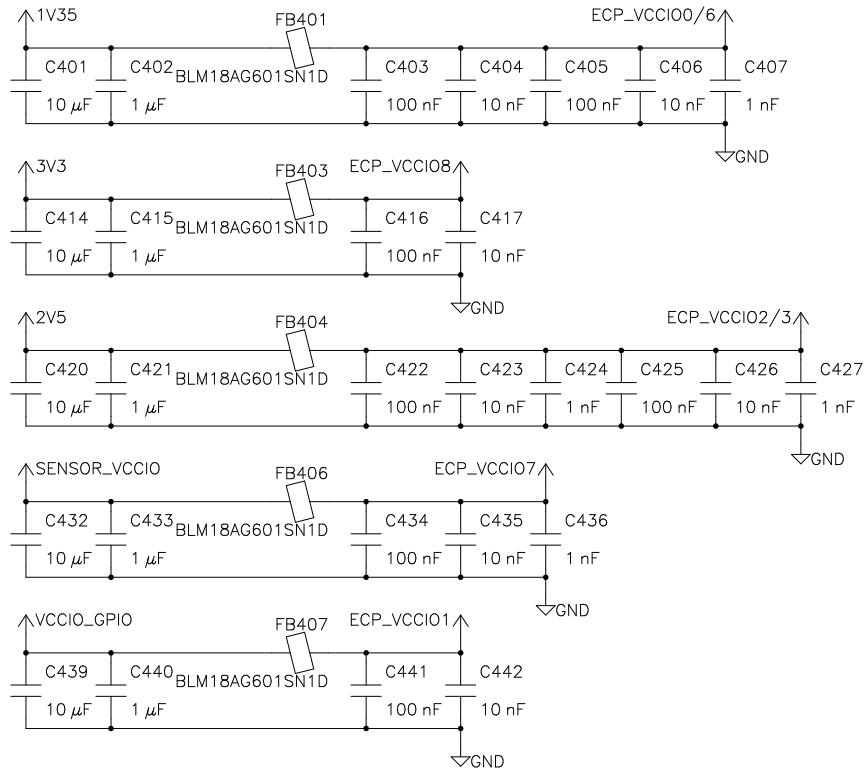
/CS must track VCC during VCC Ramp Up/Down



Sheet	Number
ecp config	3/14
Project	Revision
Axiom micro rev3	0
Drawn by	
anuejn & vup	
License	
CERN-OHL-S V2	
Date	
20200324	

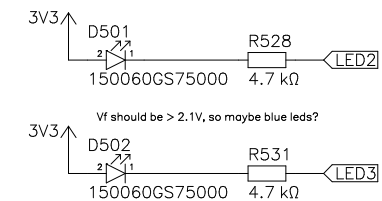
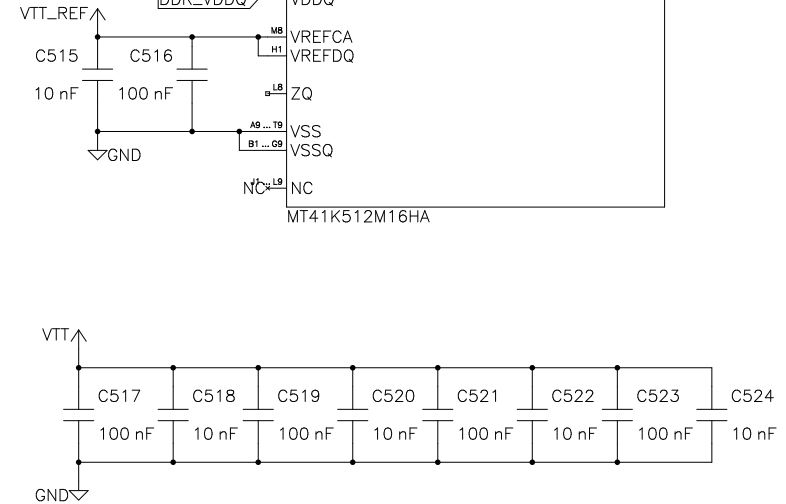
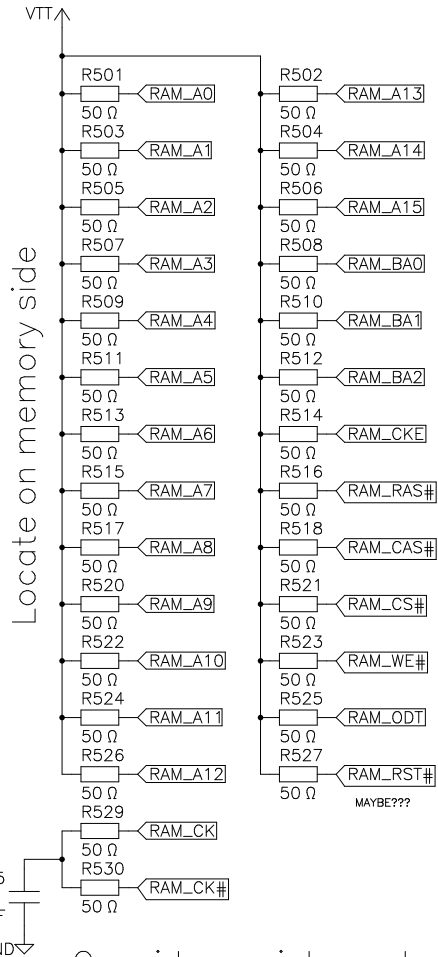
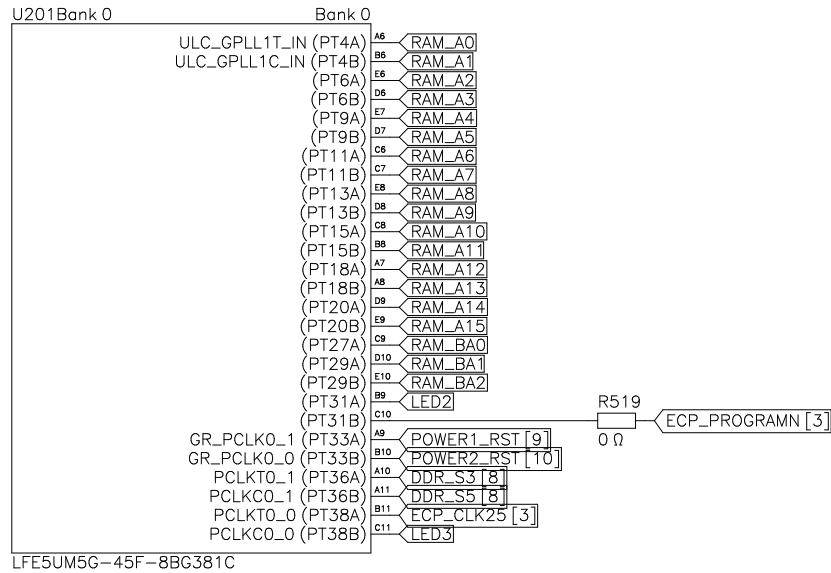
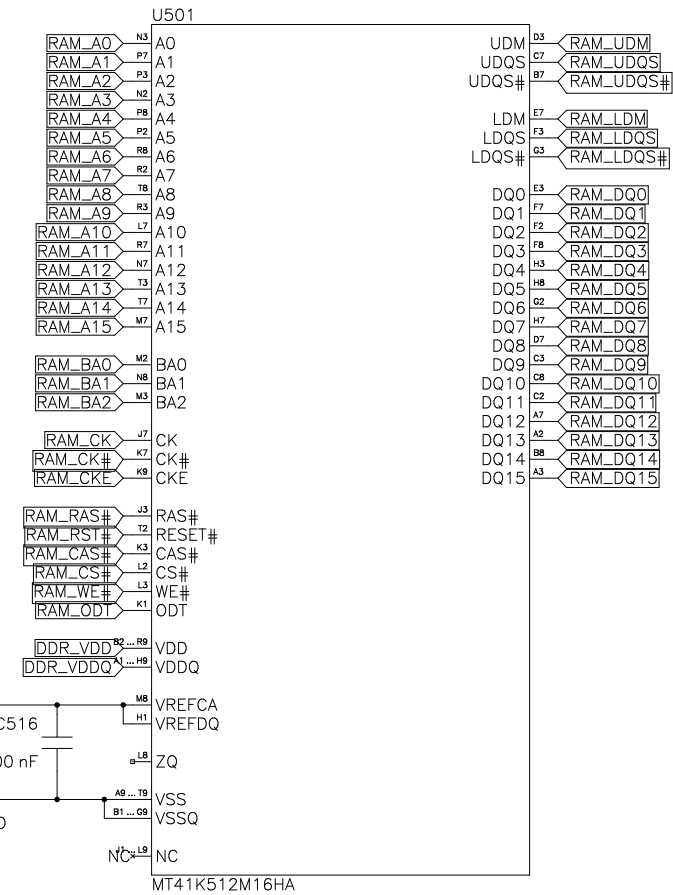
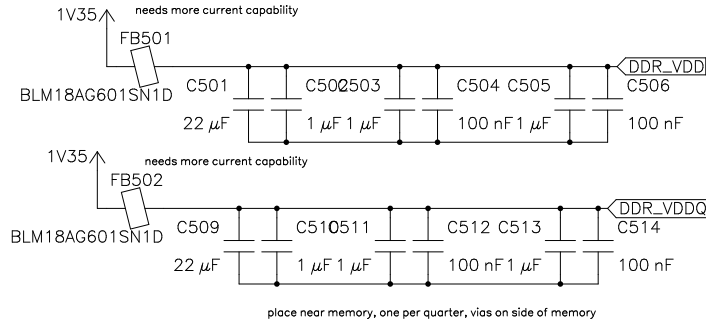
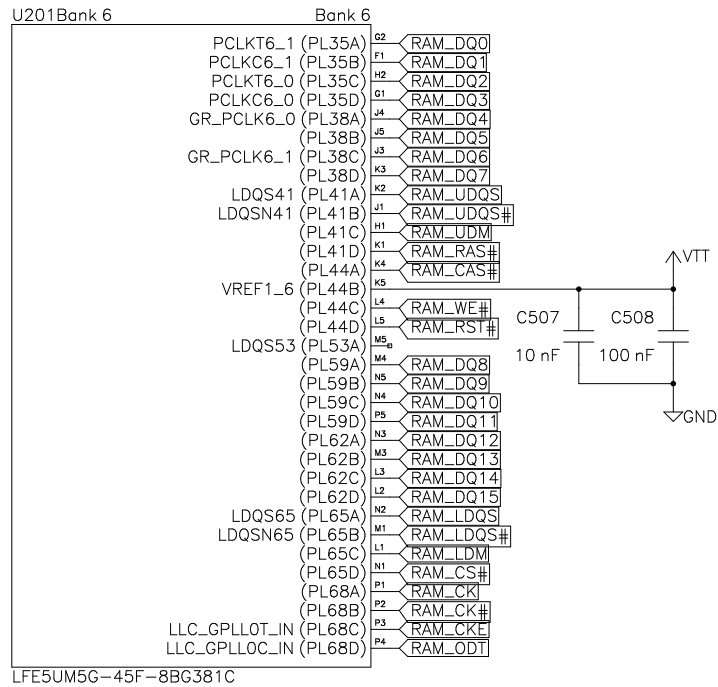


Place decoupling near FPGA, alternate 100n and 10n per pad per rail



Sheet	Number
ecp power	4/14
Project	Revision
Axiom micro rev3	0
Drawn by	
anuejn & vup	
License	
CERN-OHL-S V2	
Date	
20200324	



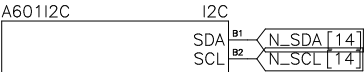


Consider resistor networks?

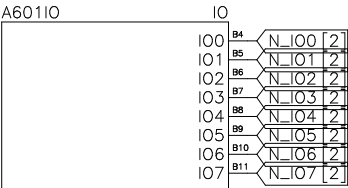
Sheet	RAM	Number	5/14
Project	Axiom micro rev3	Revision	0
Drawn by	anuejn & vup		
License	CERN-OHL-S V2		
Date	20200324		



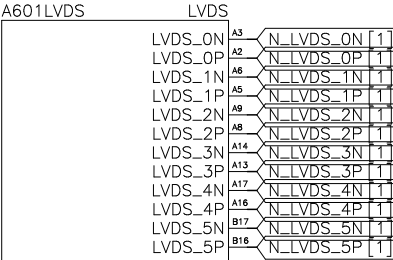
plugin north



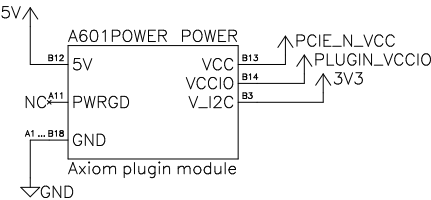
Axiom plugin module



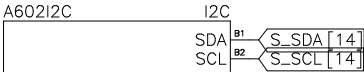
Axiom plugin module



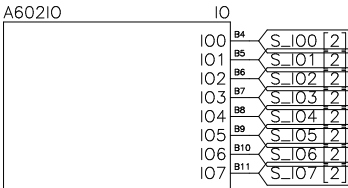
Axiom plugin module



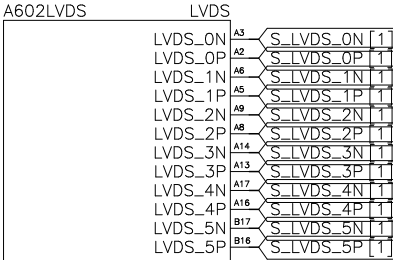
plugin south



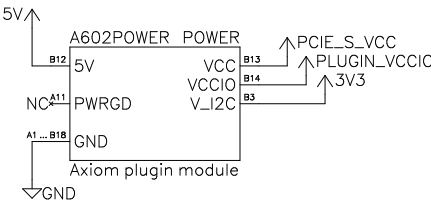
Axiom plugin module




Axiom plugin module



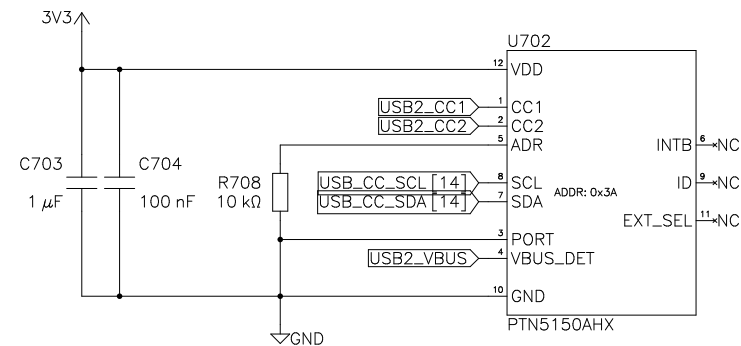
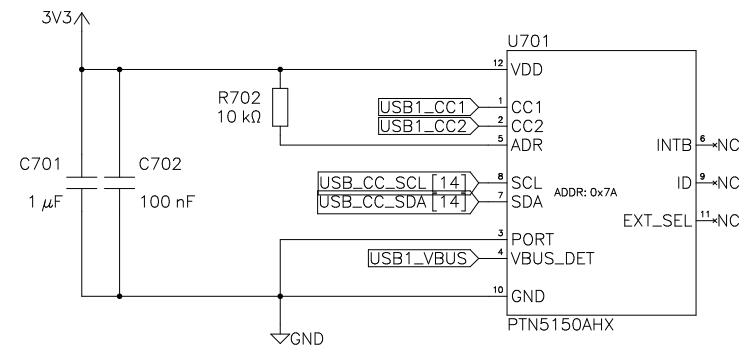
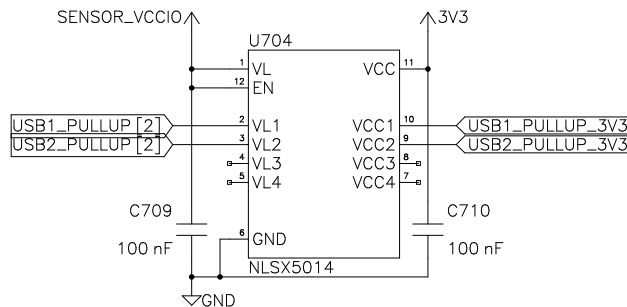
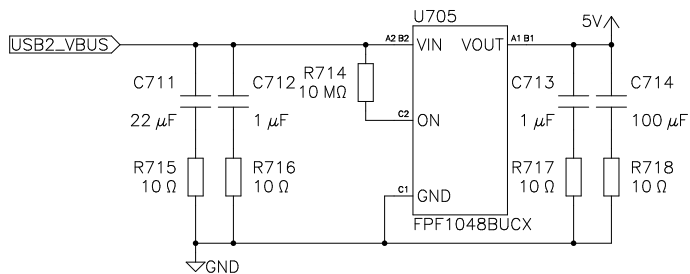
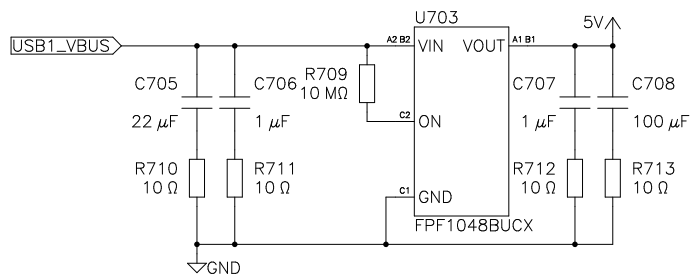
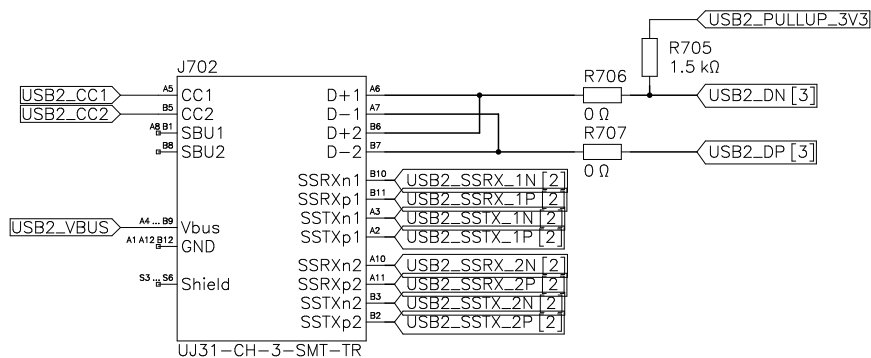
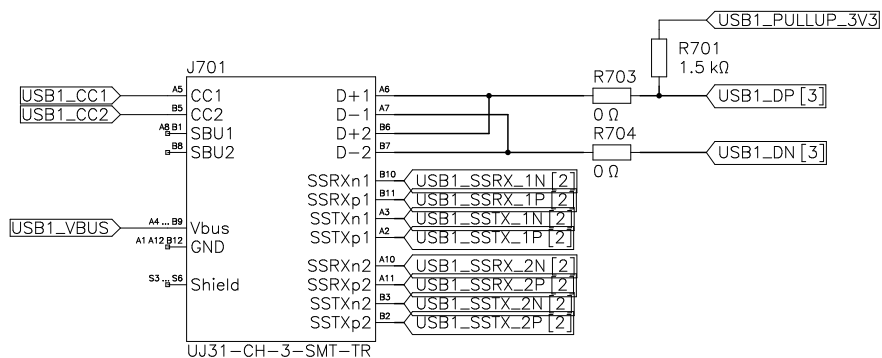
Axiom plugin module



Sheet	Number
plugin	6/14
Project	Revision
Axiom micro rev3	0
Drawn by	
anuejn & vup	
License	
CERN-OHL-S V2	
Date	
20200324	



open source hardware

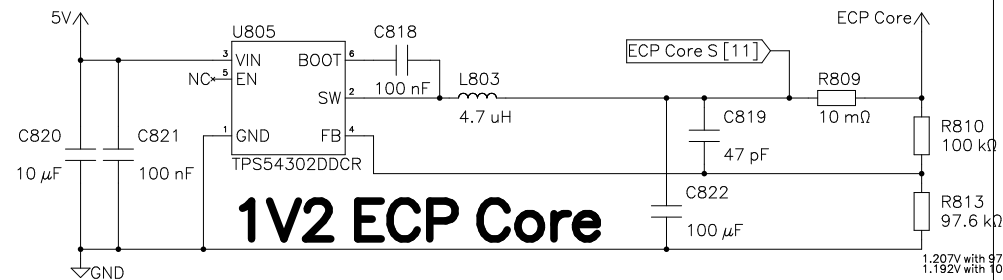
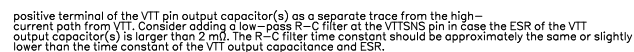


PORT = VDD: DFP mode ($R_p = 80\mu A$ power default for non-I2C mode).
 PORT = Mid (or floating): DRP mode
 PORT = GND: UFP mode

Trinary GPIO Input ADP pin run from VDD
 - ADP pull up to VDD with $10k\Omega$ resistor (I2C Enabled with ADDR bit 6 equal to 1, I2C Address 0x7A)
 - ADP pull down to GND with $10k\Omega$ resistor. (I2C Enabled with ADDR bit 6 equal to 0, I2C Address 0x3A)
 - ADP = Mid or floating (Pin 6/7/8) configured as OUT1/2/3 in non-I2C mode

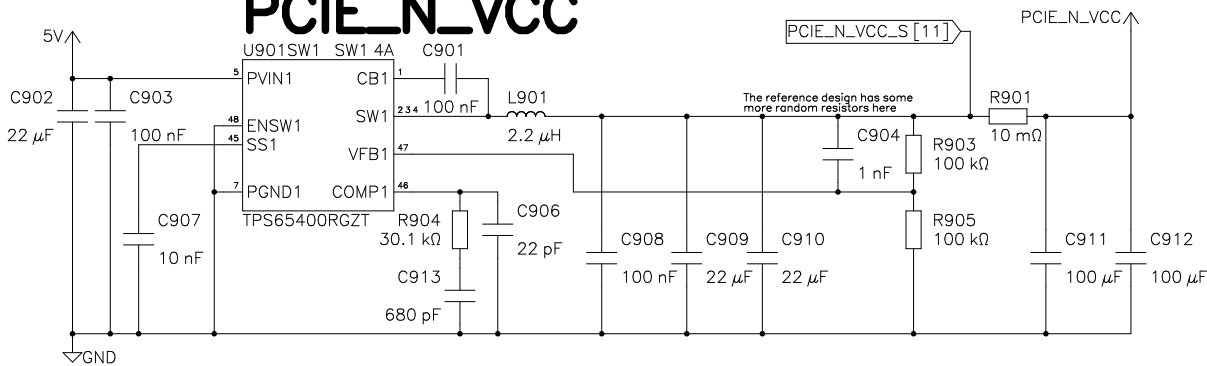
Sheet	Number
USB	7/14
Project	Revision
Axiom micro rev3	0
Drawn by	
anuejn & vup	
License	
CERN-OHL-S V2	
Date	
20200324	



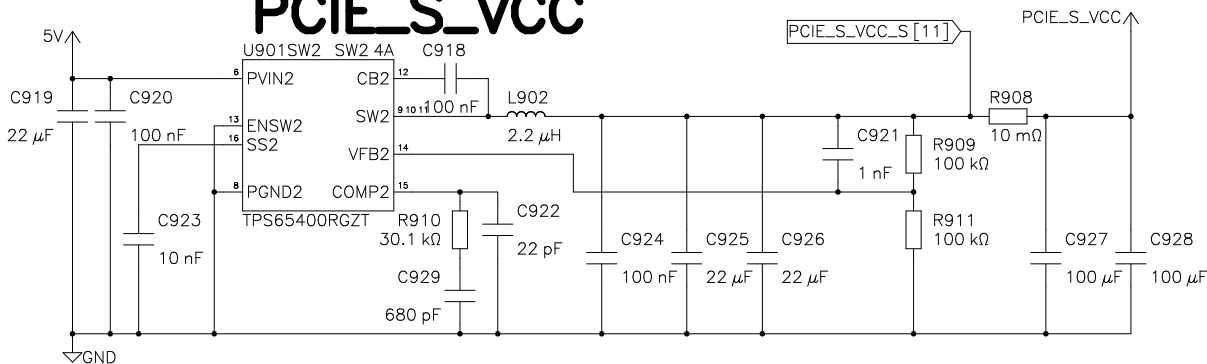


open source
hardware

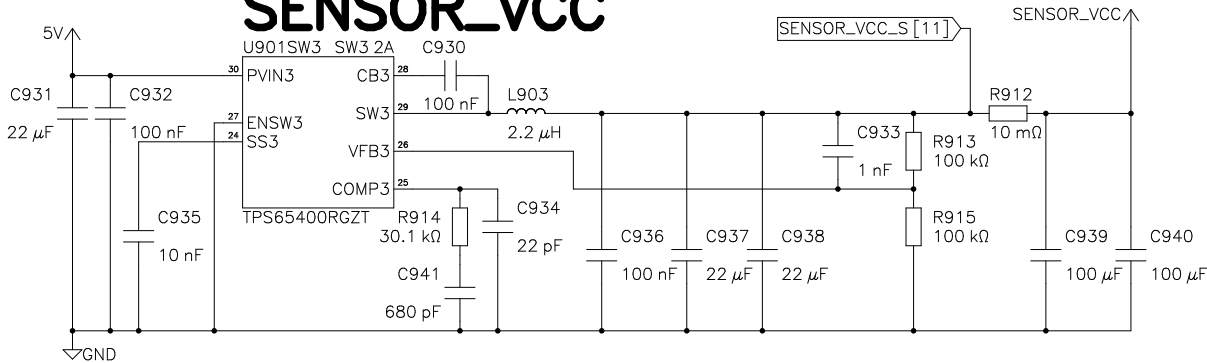
PCIE_N_VCC



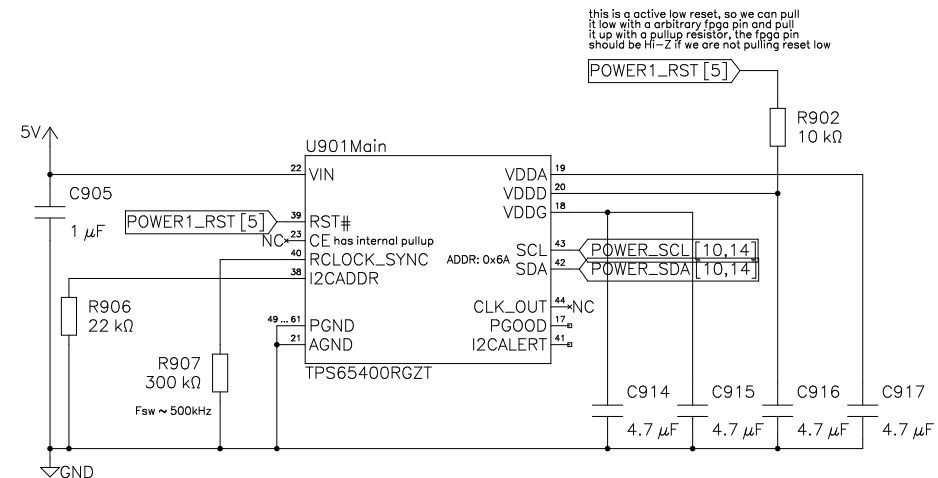
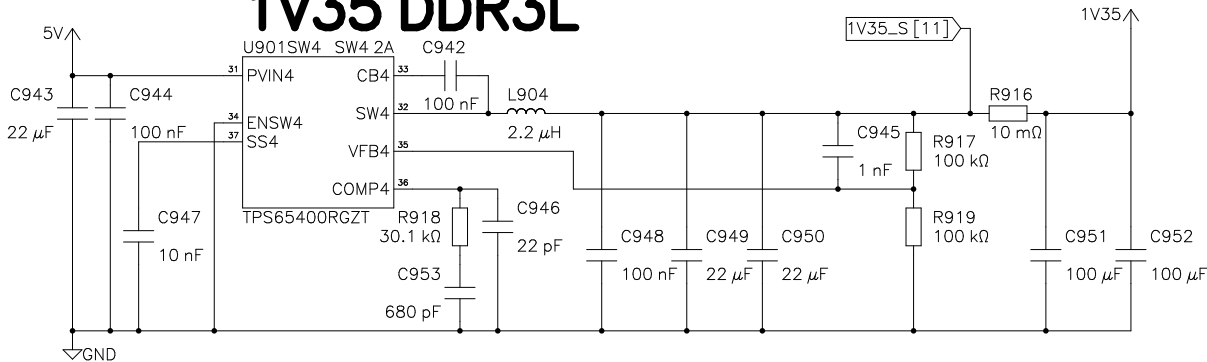
PCIE_S_VCC



SENSOR_VCC



1V35 DDR3L



all rails apart from the one use for jtag are disabled by default (as we need to setup the voltages on the first start)
soft start caps: $10\text{nF} / 5\mu\text{A} \times 0.8\text{V} = 1.6\text{ms}$
for ECP: max 10V/ms slew rate

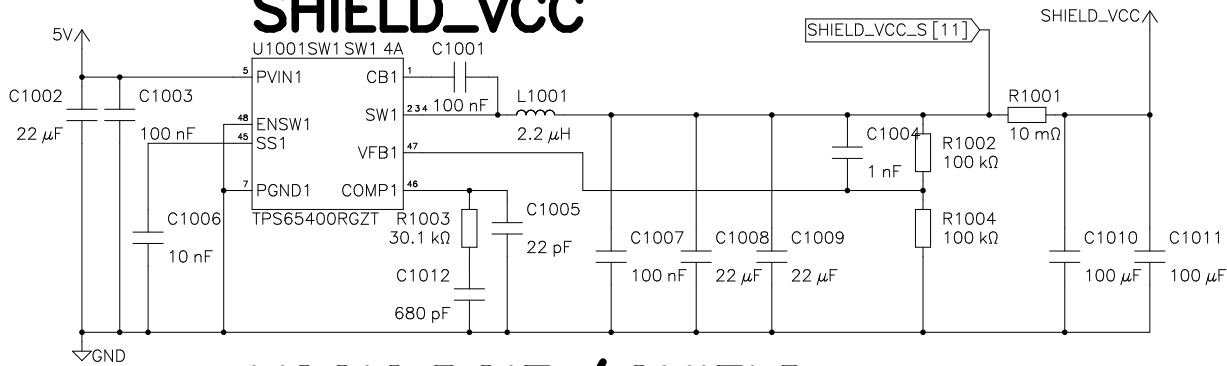
TODO:

- more bulk capacitance?
(for 1V2 the reference schematic has 470uF additionally)
- soft start capacitors
- current limiting resistor for feed forward capacitor
- think about the compensation network
- If the input supply is located more than a few inches from the TPS65400 converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of $47\mu\text{F}$ is a typical choice.

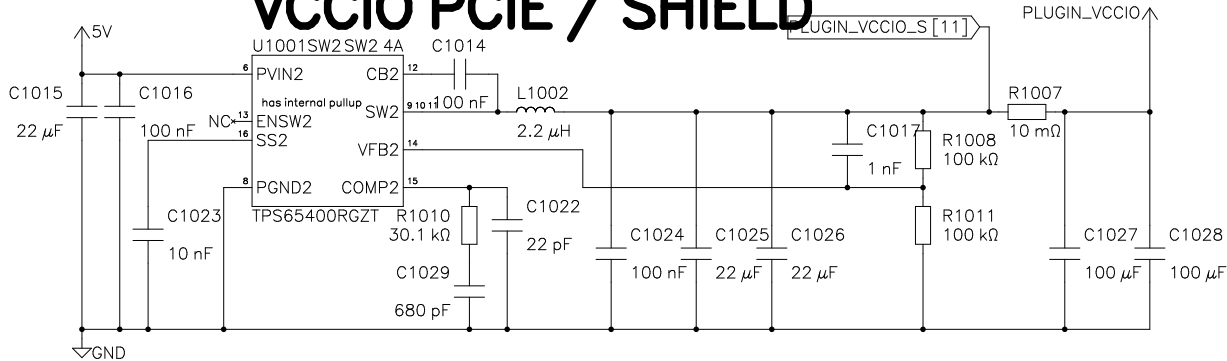
Sheet	power adjustable 1	Number	9/14
Project	Axiom micro rev3	Revision	0
Drawn by	anuejn & vup		
License	CERN-OHL-S V2		
Date	20200324		



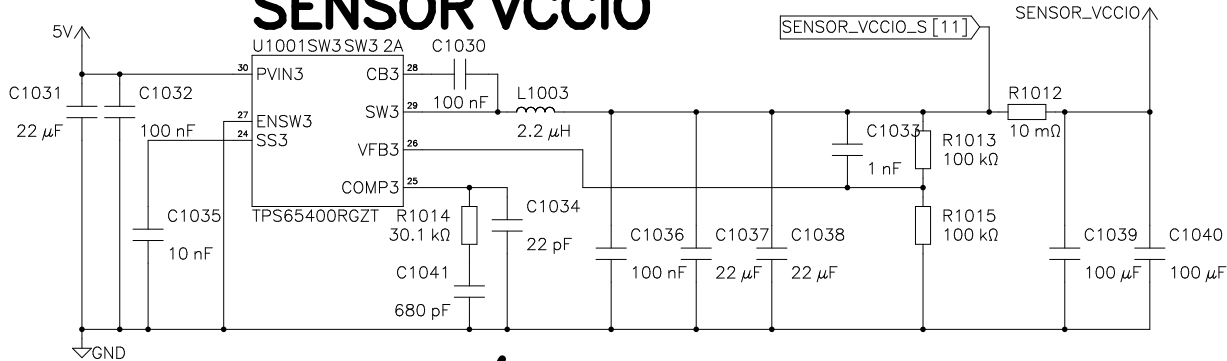
SHIELD_VCC



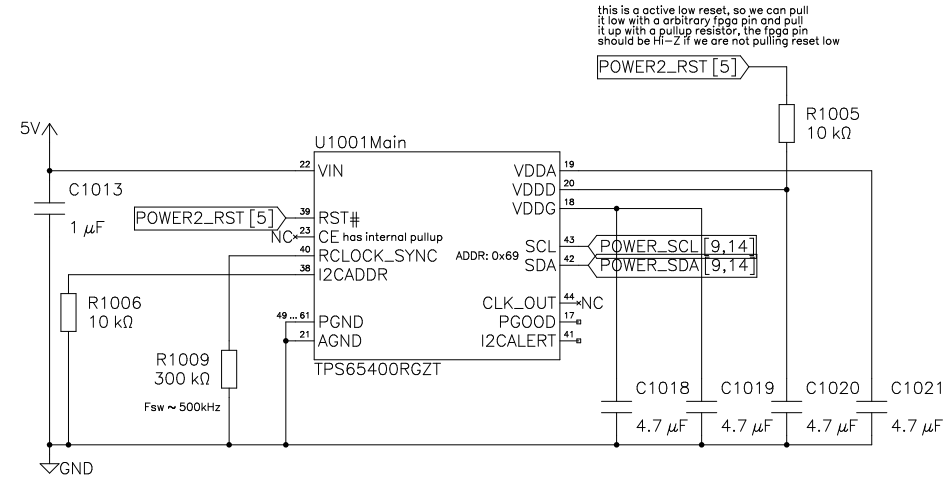
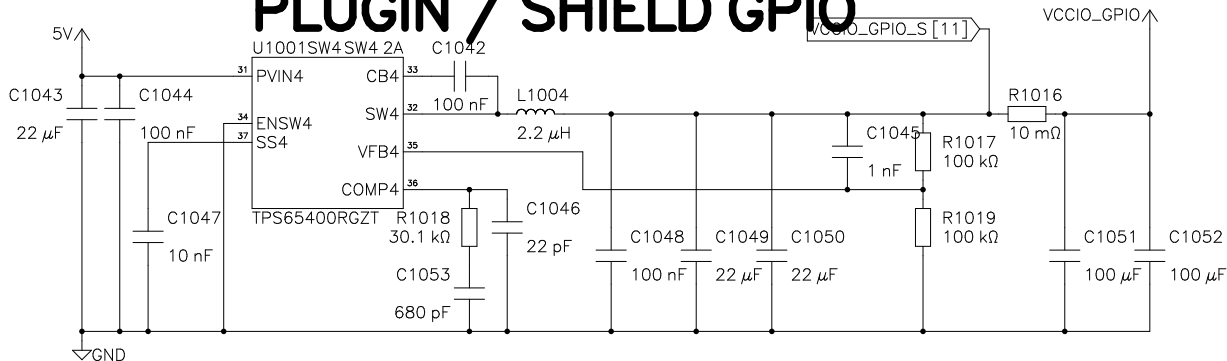
VCCIO PCIE / SHIELD



SENSOR VCCIO




PLUGIN / SHIELD GPIO

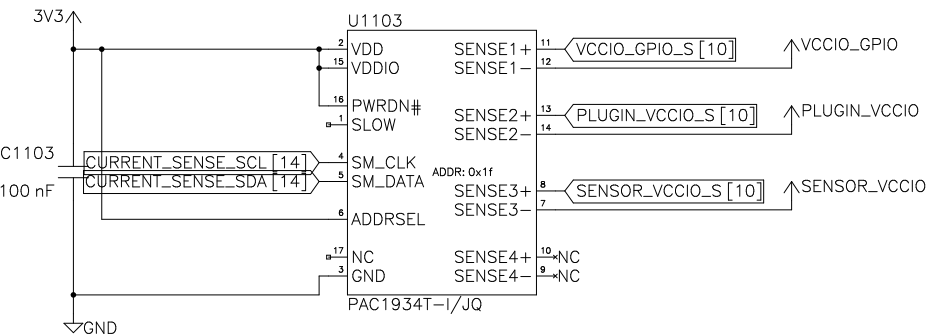
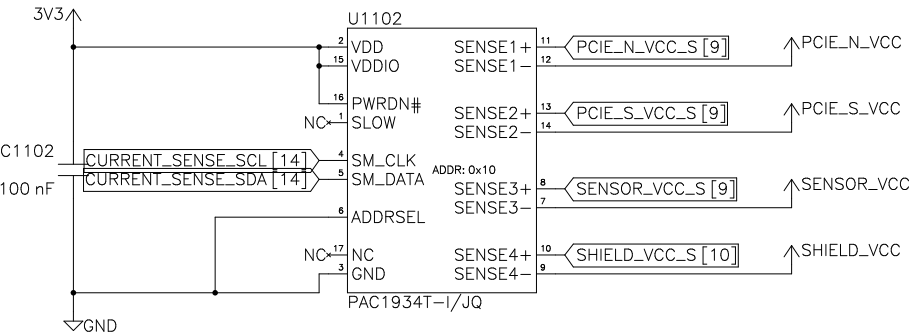
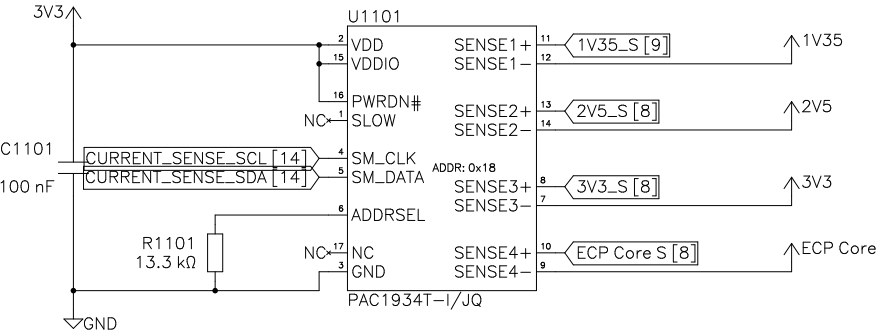



Because JTAG is driven from PLUGIN_VCCIO we somehow need to enable that one before ever being able to access the i2c bus.

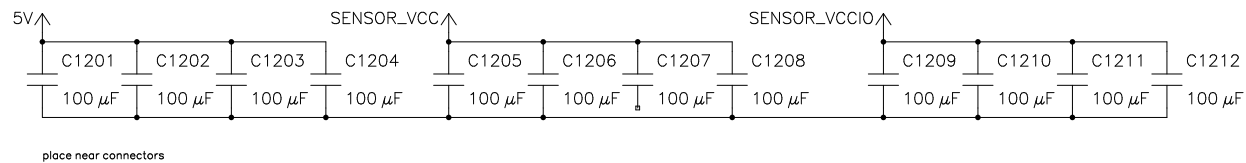
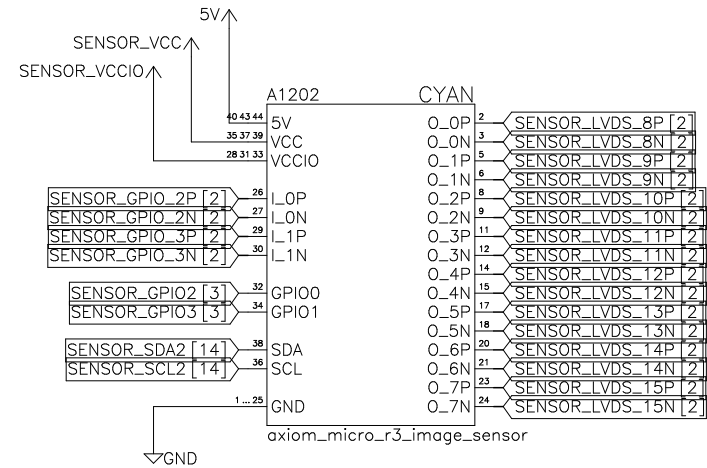
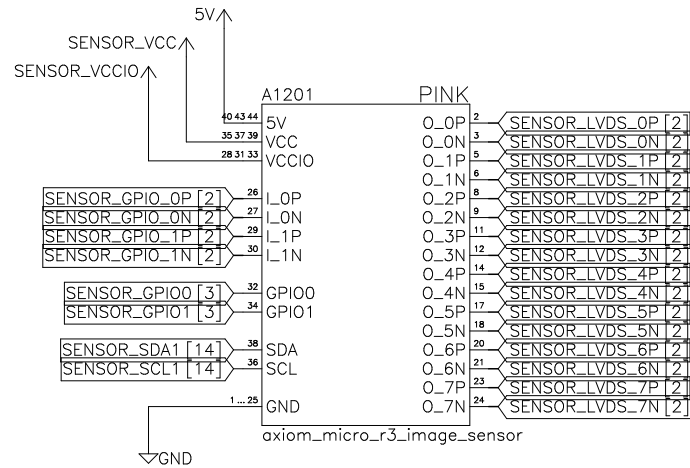
The default for the internal Vref is 0.8V, so we get a output voltage of $0.8V * (1 + 100k / 100k) = 1.6V$
 That should work for jtag (its shifted to 3v3 with a level shifter)
 ENSWx have internal pullups, to the rails are enabled by default
 This pullup can later be overridden by using some i2c commands.
 (We want to be able to do that to not damage the plugin modules, that get a direct link to this rail)

Sheet	power adjustable 2	Number	10/14
Project	Axiom micro rev3	Revision	0
Drawn by	anuejn & vup		
License	CERN-OHL-S V2		
Date	20200324		
			 open source hardware

current sense resistors: 0805W8F100MT5E or CS05W8F100MT5E



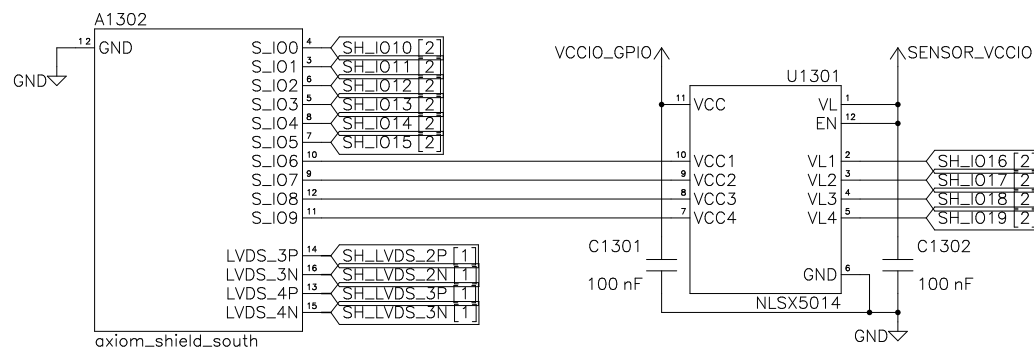
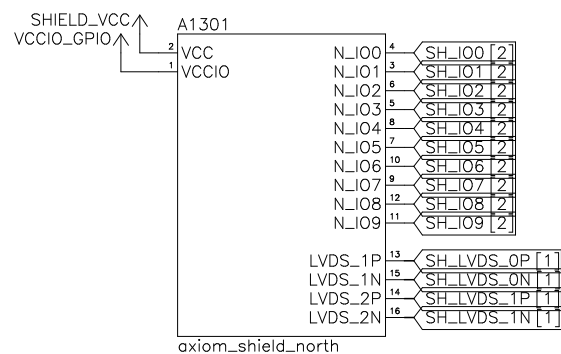
Sheet	current sense	Number	11/14
Project	Axiom micro rev3	Revision	0
Drawn by	anuejn & vup		
License	CERN-OHL-S V2		
Date	20200324		
		 open source hardware	




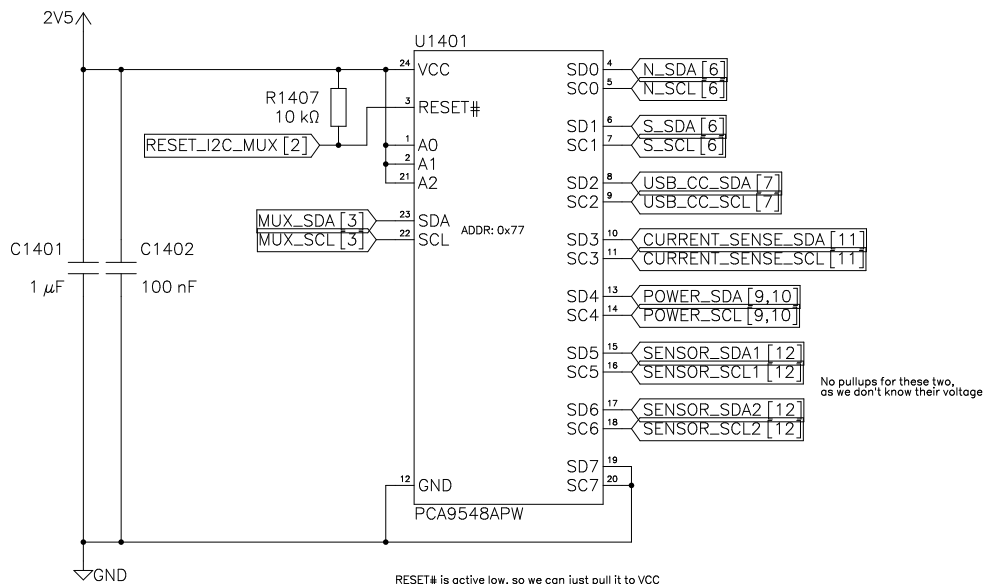
Sheet	Number
image sensor	12/14
Project	Revision
Axiom micro rev3	0
Drawn by	
anuejn & vup	
License	
CERN-OHL-S V2	
Date	
20200324	



open source
hardware



Sheet shield	Number 13/14
Project Axiom micro rev3	Revision 0
Drawn by anuejn & vup	
License CERN-OHL-S V2	 open source hardware
Date 20200324	

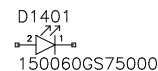
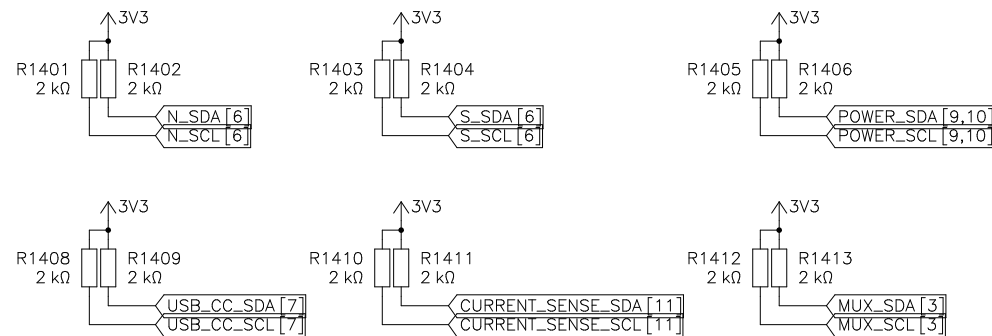


RESET# is active low, so we can just pull it to VCC, and then pull it to GND using any VCCIO from the ECP, attention has to be paid to not make RESET# get over VCC, as otherwise current flows from the RESET pin to the VCC pin, this should be accomplishable by just making the fpga output Hi-Z if it is not pulled low

2V5 VCC means about 1V8 voltage clamping by the pass through transistors That should work for most applications, we just need to be careful with nothing with 1V2 is on the bus

Unused channels have to be tied to GND or VCC

No pullups for these two, as we don't know their voltage



Sheet	Number
i2c mux	14/14
Project	Revision
Axiom micro rev3	0
Drawn by	
anuejn & vup	
License	
CERN-OHL-S V2	
Date	
20200324	

