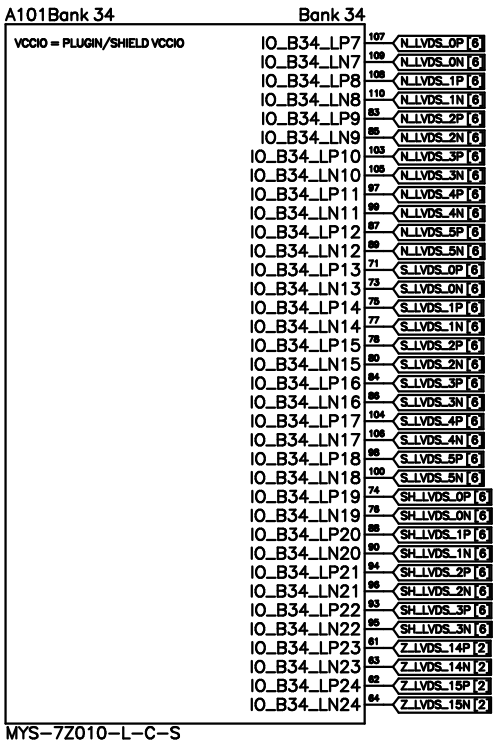
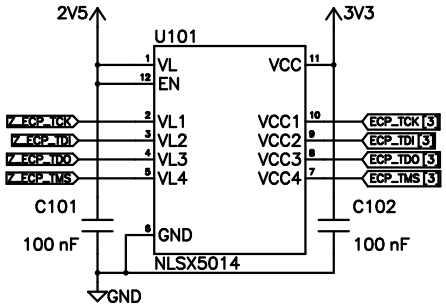
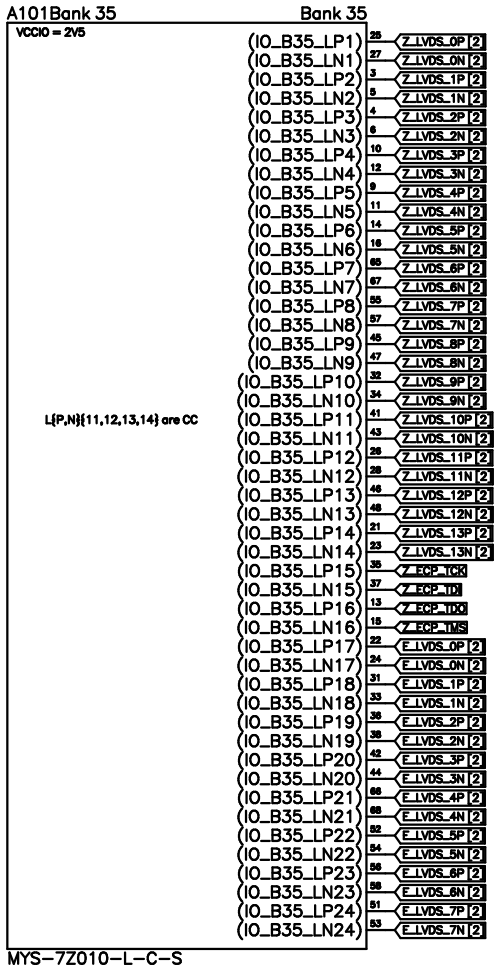
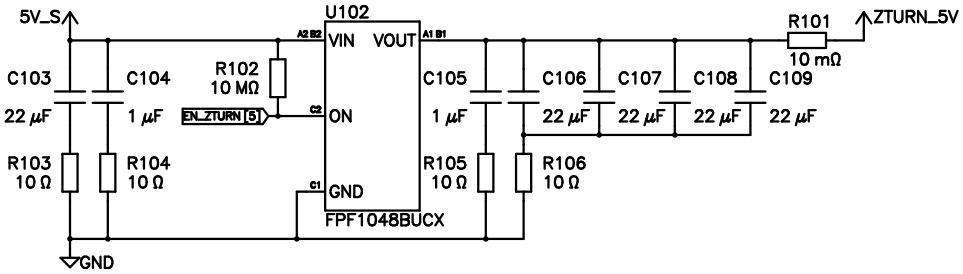
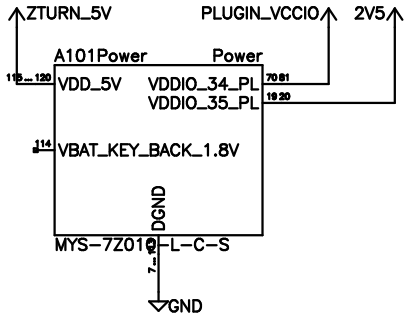
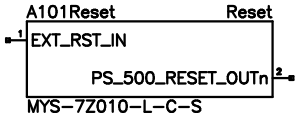




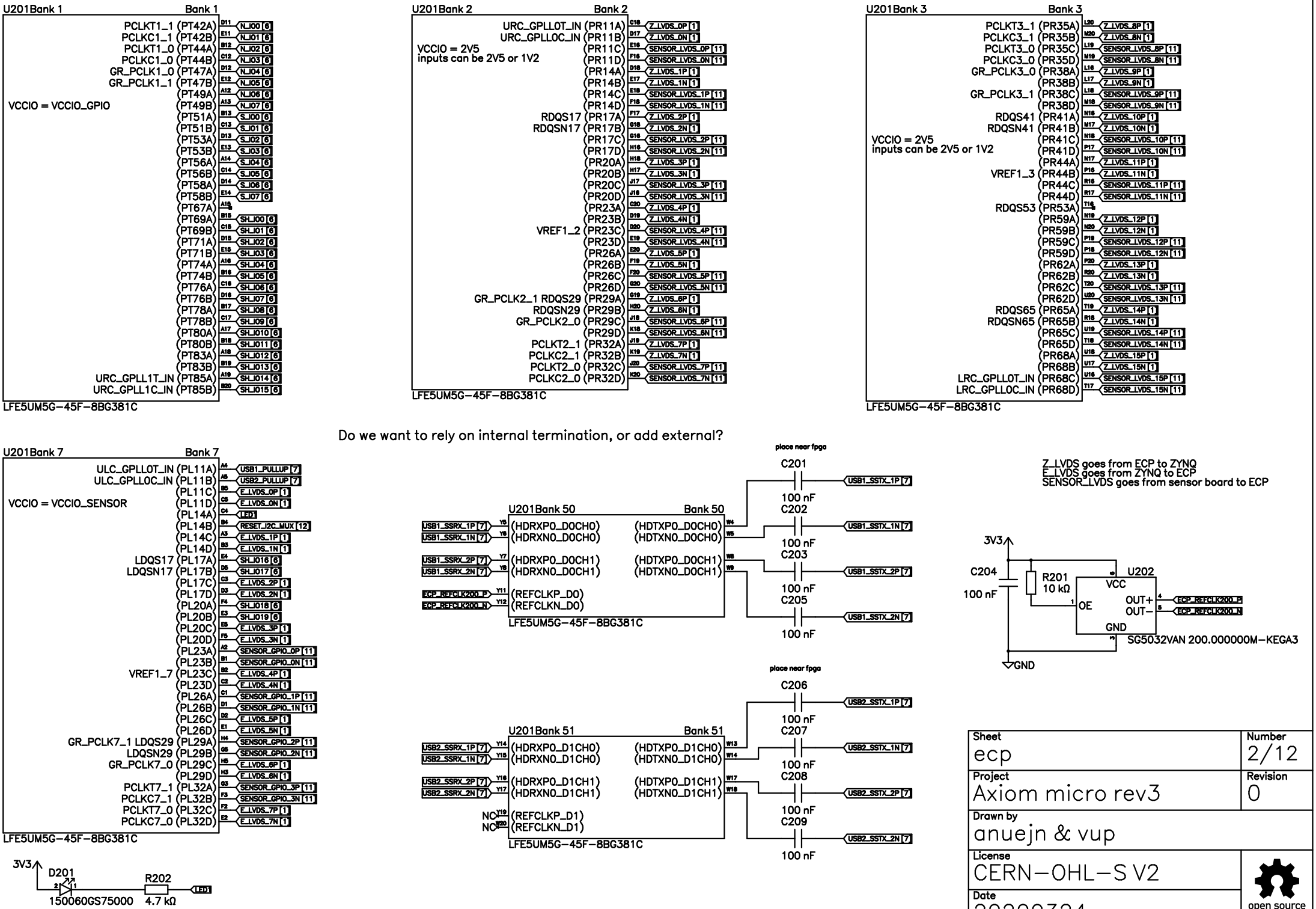


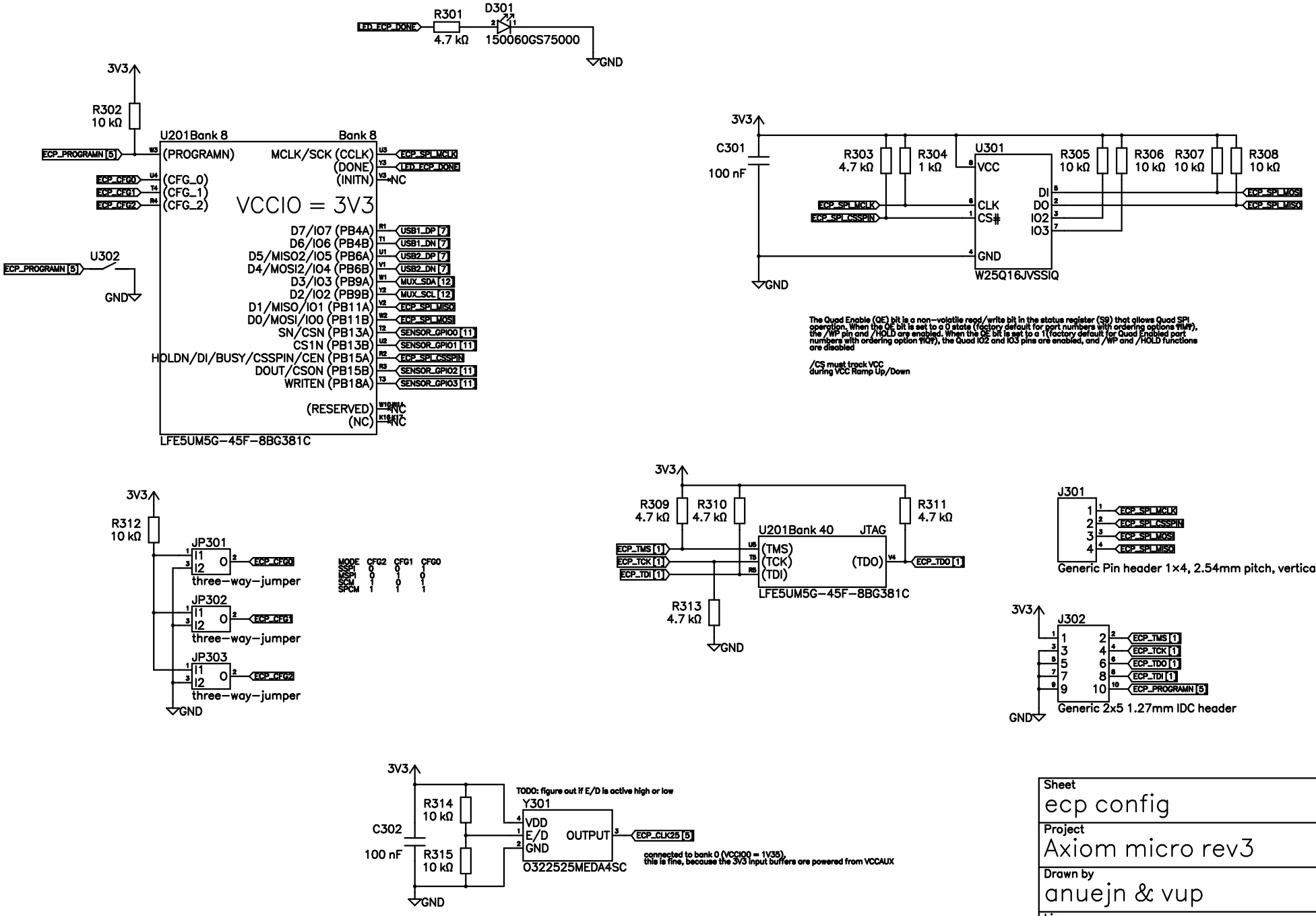






Sheet: zturn lite	Number: 1/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	open source hardware
Date: 20200324	


U201Bank 1
Bank 1
PCLKT1_1 (PT42A)
PCLKC1_1 (PT42B)
PCLKT1_0 (PT44A)
PCLKC1_0 (PT44B)
GR_PCLK1_0 (PT47A)
GR_PCLK1_1 (PT47B)
(PT49A)
VCCIO = VCCIO_GPIO
(PT49B)
(PT51A)
(PT51B)
(PT53A)
(PT53B)
(PT56A)
(PT56B)
(PT58A)
(PT58B)
(PT67A)
(PT69A)
(PT69B)
(PT71A)
(PT71B)
(PT74A)
(PT74B)
(PT76A)
(PT76B)
(PT78A)
(PT78B)
(PT80A)
(PT80B)
(PT83A)
(PT83B)
URC_GPLL1T_IN (PT85A)
URC_GPLL1C_IN (PT85B)
LFE5UM5G-45F-8BG381C
U201Bank 2
Bank 2
URC_GPLL0T_IN (PR11A)
URC_GPLL0C_IN (PR11B)
VCCIO = 2V5
inputs can be 2V5 or 1V2
(PR11C)
(PR11D)
(PR14A)
(PR14B)
(PR14C)
(PR14D)
RDQS17 (PR17A)
RDQSN17 (PR17B)
(PR17C)
(PR17D)
(PR20A)
(PR20B)
(PR20C)
(PR20D)
(PR23A)
(PR23B)
VREF1_2 (PR23C)
(PR23D)
(PR26A)
(PR26B)
(PR26C)
(PR26D)
GR_PCLK2_1 RDQS29 (PR29A)
RDQSN29 (PR29B)
GR_PCLK2_0 (PR29C)
(PR29D)
PCLKT2_1 (PR32A)
PCLKC2_1 (PR32B)
PCLKT2_0 (PR32C)
PCLKC2_0 (PR32D)
LFE5UM5G-45F-8BG381C
U201Bank 3
Bank 3
PCLKT3_1 (PR35A)
PCLKC3_1 (PR35B)
PCLKT3_0 (PR35C)
PCLKC3_0 (PR35D)
GR_PCLK3_0 (PR38A)
(PR38B)
GR_PCLK3_1 (PR38C)
(PR38D)
RDQS41 (PR41A)
RDQSN41 (PR41B)
VCCIO = 2V5
inputs can be 2V5 or 1V2
(PR41C)
(PR41D)
(PR44A)
VREF1_3 (PR44B)
(PR44C)
(PR44D)
RDQS53 (PR53A)
(PR59A)
(PR59B)
(PR59C)
(PR59D)
(PR62A)
(PR62B)
(PR62C)
(PR62D)
RDQS65 (PR65A)
RDQSN65 (PR65B)
(PR65C)
(PR65D)
(PR68A)
(PR68B)
LRC_GPLL0T_IN (PR68C)
LRC_GPLL0C_IN (PR68D)
LFE5UM5G-45F-8BG381C
Do we want to rely on internal termination, or add external?
U201Bank 7
Bank 7
ULC_GPLL0T_IN (PL11A)
ULC_GPLL0C_IN (PL11B)
(PL11C)
VCCIO = VCCIO_SENSOR
(PL11D)
(PL14A)
(PL14B)
(PL14C)
(PL14D)
LDQS17 (PL17A)
LDQSN17 (PL17B)
(PL17C)
(PL17D)
(PL20A)
(PL20B)
(PL20C)
(PL20D)
(PL23A)
(PL23B)
VREF1_7 (PL23C)
(PL23D)
(PL26A)
(PL26B)
(PL26C)
(PL26D)
GR_PCLK7_1 LDQS29 (PL29A)
LDQSN29 (PL29B)
GR_PCLK7_0 (PL29C)
(PL29D)
PCLKT7_1 (PL32A)
PCLKC7_1 (PL32B)
PCLKT7_0 (PL32C)
PCLKC7_0 (PL32D)
LFE5UM5G-45F-8BG381C
3V3
D201
150060GS75000
R202
4.7 kΩ
LED1
place near fpga
C201
100 nF
C202
100 nF
C203
100 nF
C205
100 nF
U201Bank 50
Bank 50
(HDRXP0_D0CH0)
(HDRXN0_D0CH0)
(HDRXP0_D0CH1)
(HDRXN0_D0CH1)
(REFCLKP_D0)
(REFCLKN_D0)
(HDTXP0_D0CH0)
(HDTXN0_D0CH0)
(HDTXP0_D0CH1)
(HDTXN0_D0CH1)
LFE5UM5G-45F-8BG381C
place near fpga
C206
100 nF
C207
100 nF
C208
100 nF
C209
100 nF
U201Bank 51
Bank 51
(HDRXP0_D1CH0)
(HDRXN0_D1CH0)
(HDRXP0_D1CH1)
(HDRXN0_D1CH1)
(REFCLKP_D1)
(REFCLKN_D1)
(HDTXP0_D1CH0)
(HDTXN0_D1CH0)
(HDTXP0_D1CH1)
(HDTXN0_D1CH1)
LFE5UM5G-45F-8BG381C
Z_LVDS goes from ECP to ZYNQ
E_LVDS goes from ZYNQ to ECP
SENSOR_LVDS goes from sensor board to ECP
3V3
C204
100 nF
R201
10 kΩ
U202
VCC
OE
OUT+
OUT−
GND
SG5032VAN 200.000000M-KEGA3
GND
Sheet
ecp
Number
2/12
Project
Axiom micro rev3
Revision
0
Drawn by
anuejn & vup
License
CERN-OHL-S V2
Date
20200324
open source hardware



Sheet: ecp config	Number: 3/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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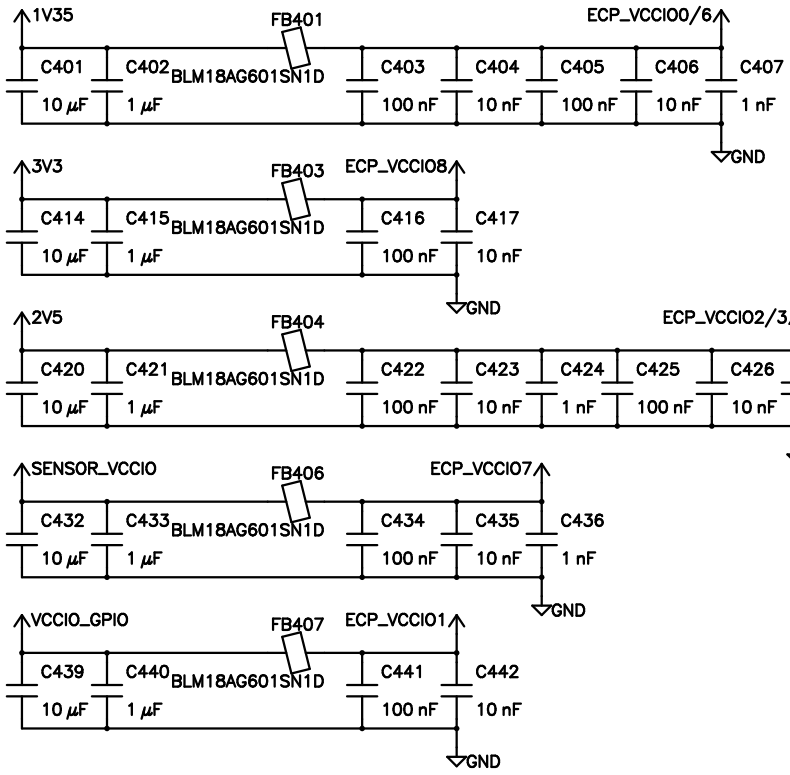
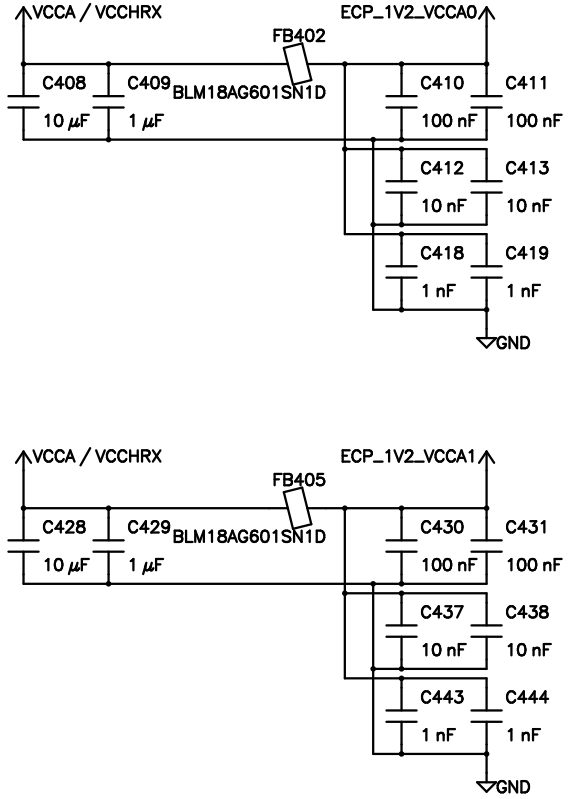
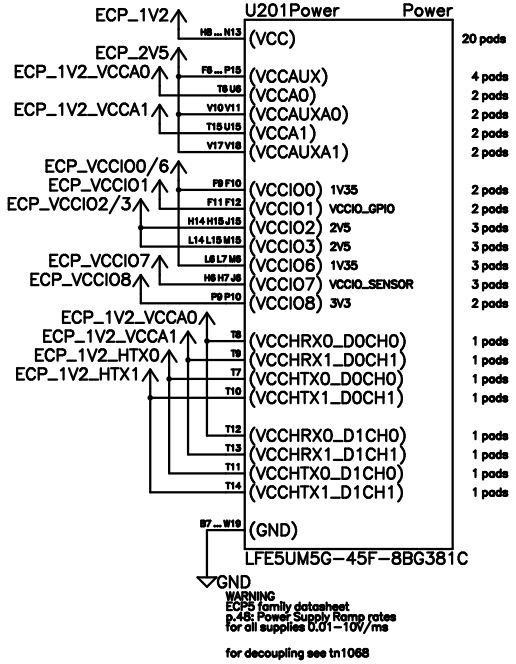
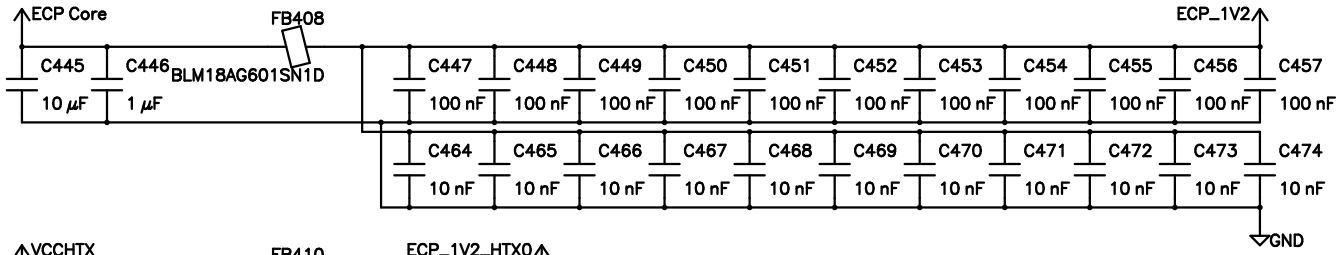
Date: 20200324	open source hardware

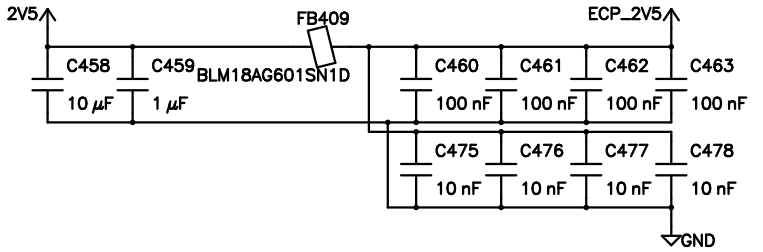
Place decoupling near FPGA, alternate 100n and 10n per pad per rail

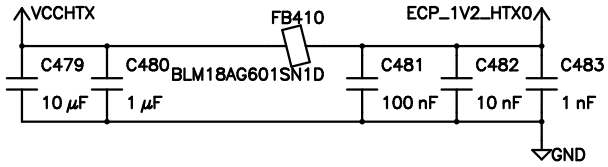


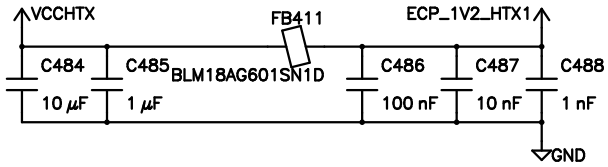




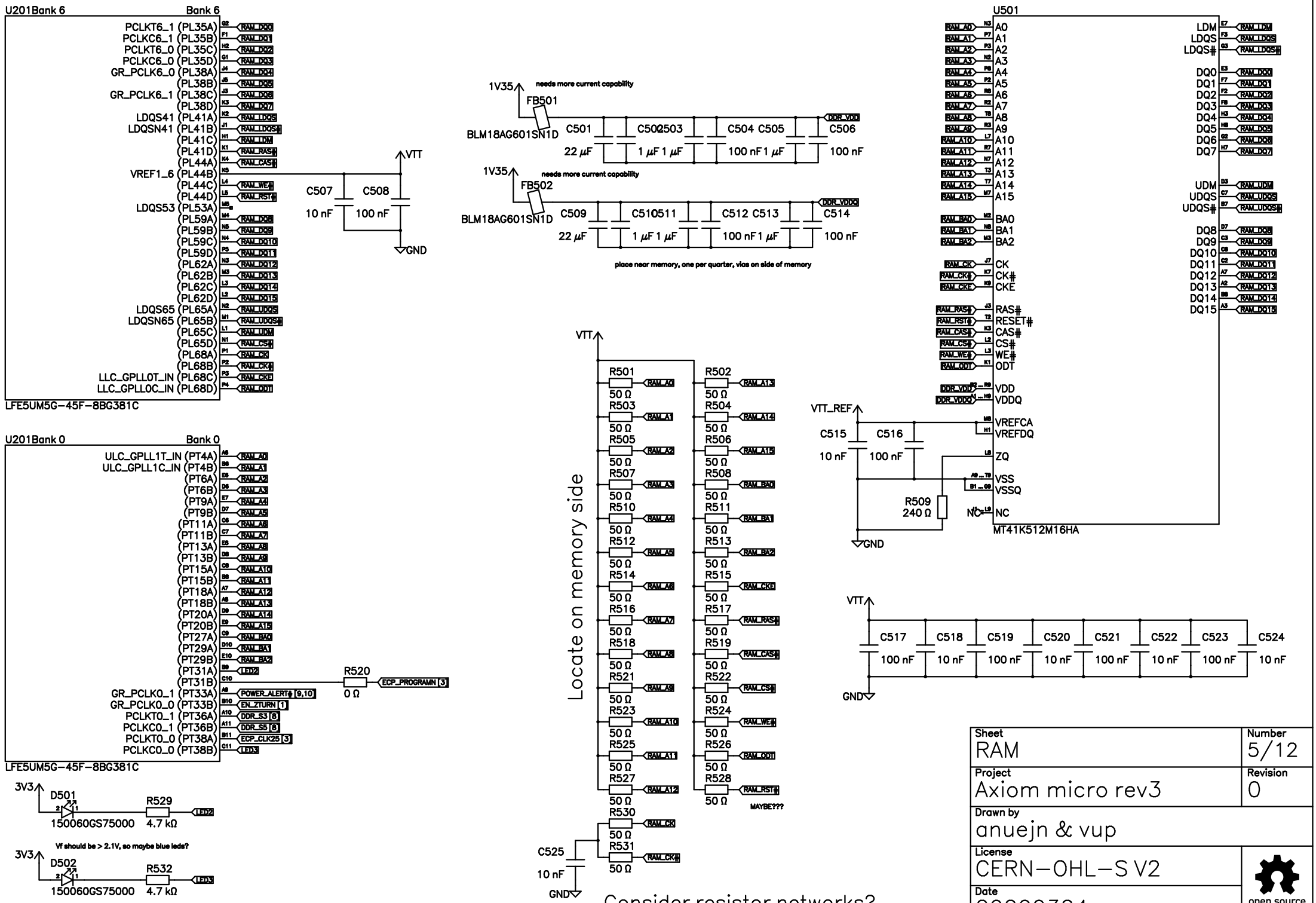


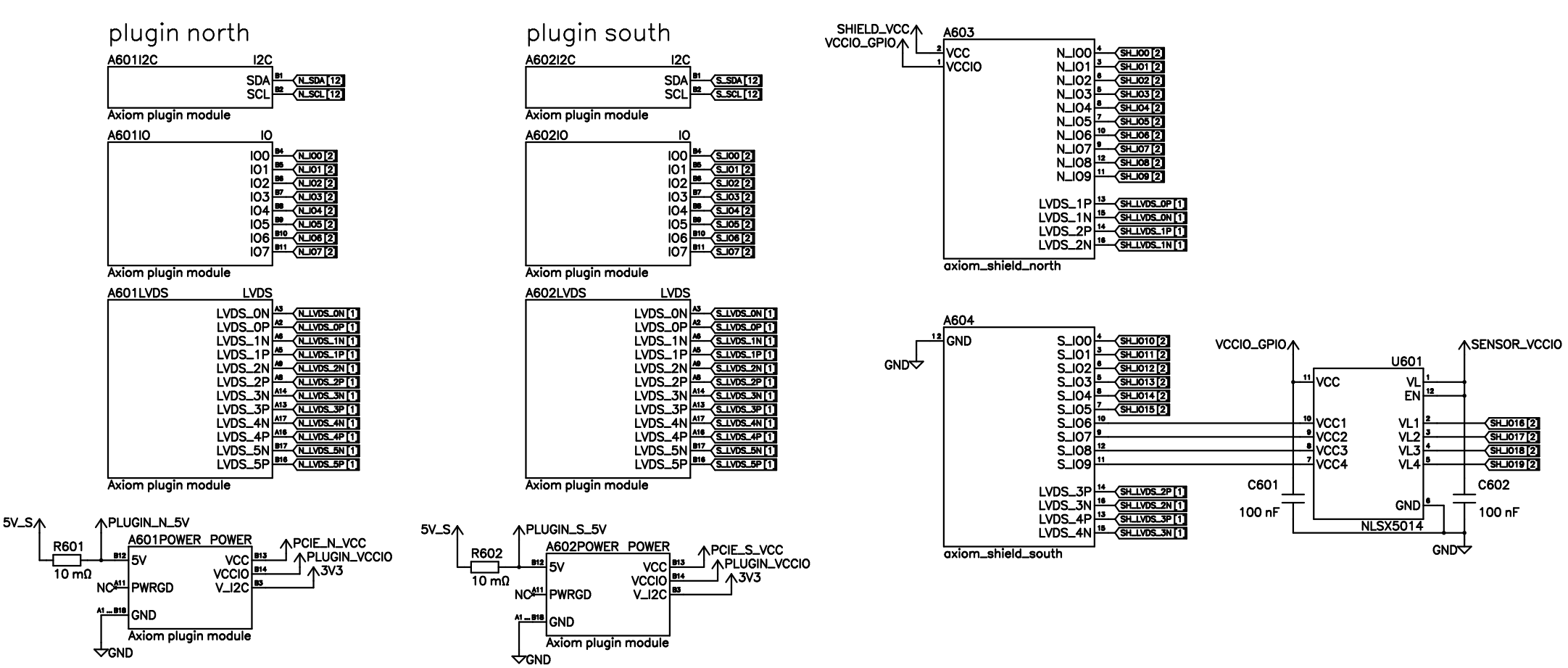




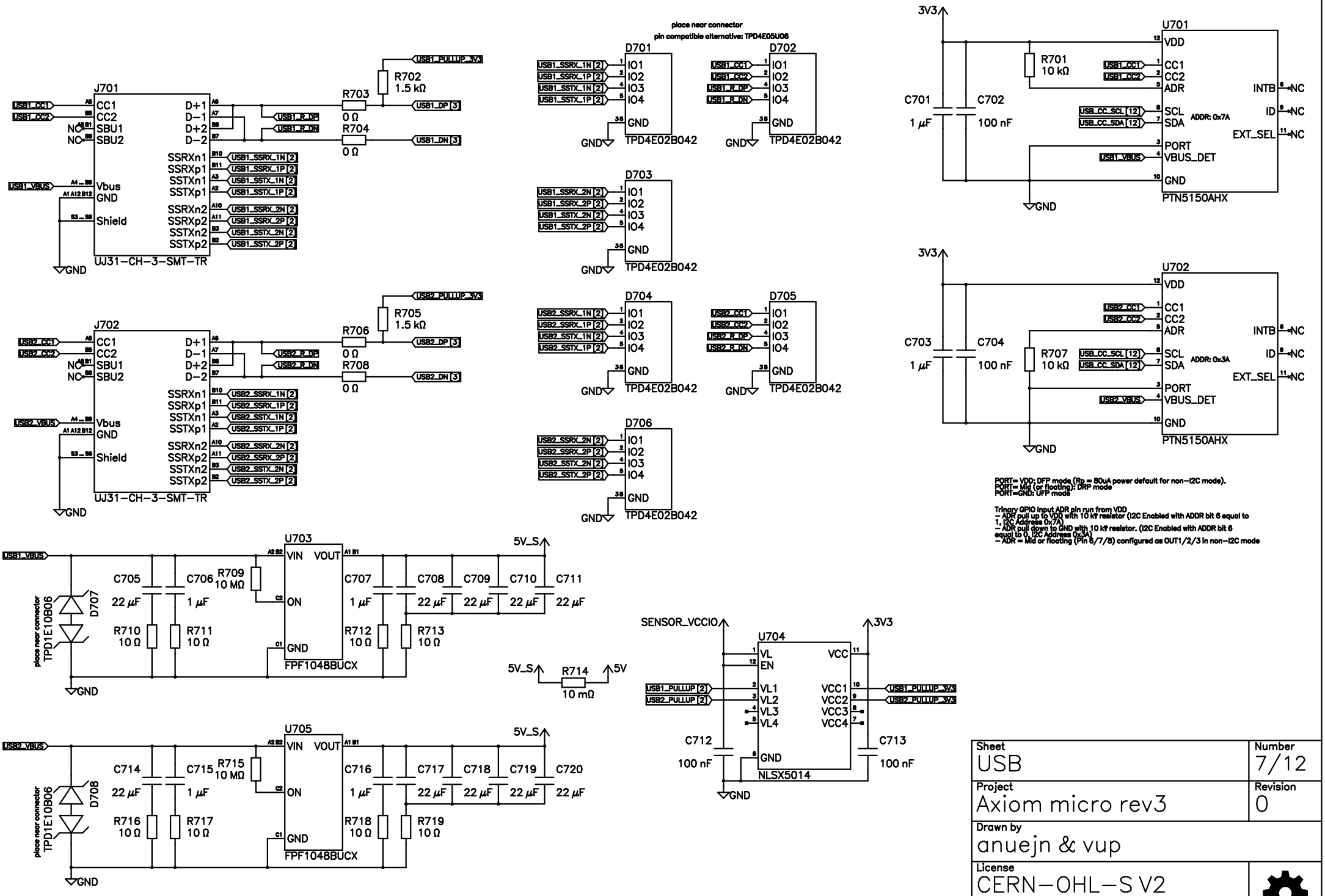


Sheet: ecp power	Number: 4/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	open source hardware
Date: 20200324	

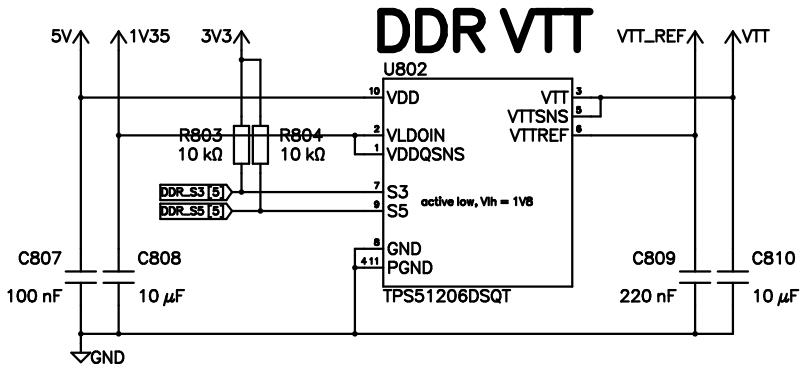

U201Bank 6
Bank 6
PCLKT6_1 (PL35A)
PCLKC6_1 (PL35B)
PCLKT6_0 (PL35C)
PCLKC6_0 (PL35D)
GR_PCLK6_0 (PL38A)
(PL38B)
GR_PCLK6_1 (PL38C)
(PL38D)
LDQS41 (PL41A)
LDQSN41 (PL41B)
(PL41C)
(PL41D)
(PL44A)
VREF1_6 (PL44B)
(PL44C)
(PL44D)
LDQS53 (PL53A)
(PL59A)
(PL59B)
(PL59C)
(PL59D)
(PL62A)
(PL62B)
(PL62C)
(PL62D)
LDQS65 (PL65A)
LDQSN65 (PL65B)
(PL65C)
(PL65D)
(PL68A)
(PL68B)
LLC_GPLL0T_IN (PL68C)
LLC_GPLL0C_IN (PL68D)
RAM_DQ0
RAM_DQ1
RAM_DQ2
RAM_DQ3
RAM_DQ4
RAM_DQ5
RAM_DQ6
RAM_DQ7
RAM_LDQS
RAM_LDQS#
RAM_LDM
RAM_RAS#
RAM_CAS#
RAM_WE#
RAM_RST#
RAM_DQ8
RAM_DQ9
RAM_DQ10
RAM_DQ11
RAM_DQ12
RAM_DQ13
RAM_DQ14
RAM_DQ15
RAM_UDQS
RAM_UDQS#
RAM_UDM
RAM_CS#
RAM_CK
RAM_CK#
RAM_CKE
RAM_ODT
LFE5UM5G-45F-8BG381C
VTT
C507
10 nF
C508
100 nF
GND
1V35
needs more current capability
FB501
BLM18AG601SN1D
C501
22 µF
C502
1 µF
C503
1 µF
C504
100 nF
C505
1 µF
C506
100 nF
DDR_VDD
1V35
needs more current capability
FB502
BLM18AG601SN1D
C509
22 µF
C510
1 µF
C511
1 µF
C512
100 nF
C513
1 µF
C514
100 nF
DDR_VDDQ
place near memory, one per quarter, vias on side of memory
U501
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
BA0
BA1
BA2
CK
CK#
CKE
RAS#
RESET#
CAS#
CS#
WE#
ODT
VDD
VDDQ
VREFCA
VREFDQ
ZQ
VSS
VSSQ
NC
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
LDM
LDQS
LDQS#
UDM
UDQS
UDQS#
MT41K512M16HA
VTT_REF
C515
10 nF
C516
100 nF
R509
240 Ω
GND
U201Bank 0
Bank 0
ULC_GPLL1T_IN (PT4A)
ULC_GPLL1C_IN (PT4B)
(PT6A)
(PT6B)
(PT9A)
(PT9B)
(PT11A)
(PT11B)
(PT13A)
(PT13B)
(PT15A)
(PT15B)
(PT18A)
(PT18B)
(PT20A)
(PT20B)
(PT27A)
(PT29A)
(PT29B)
(PT31A)
(PT31B)
GR_PCLK0_1 (PT33A)
GR_PCLK0_0 (PT33B)
PCLKT0_1 (PT36A)
PCLKC0_1 (PT36B)
PCLKT0_0 (PT38A)
PCLKC0_0 (PT38B)
RAM_A0
RAM_A1
RAM_A2
RAM_A3
RAM_A4
RAM_A5
RAM_A6
RAM_A7
RAM_A8
RAM_A9
RAM_A10
RAM_A11
RAM_A12
RAM_A13
RAM_A14
RAM_A15
RAM_BA0
RAM_BA1
RAM_BA2
LED2
R520
0 Ω
ECP_PROGRAMN [3]
POWER_ALERT# [9,10]
EN_ZTURN [1]
DDR_S3 [6]
DDR_S5 [6]
ECP_CLK25 [3]
LED3
LFE5UM5G-45F-8BG381C
Locate on memory side
R501
R502
R503
R504
R505
R506
R507
R508
R510
R511
R512
R513
R514
R515
R516
R517
R518
R519
R521
R522
R523
R524
R525
R526
R527
R528
50 Ω
MAYBE???
R530
R531
C525
10 nF
GND
3V3
D501
150060GS75000
R529
4.7 kΩ
LED2
Vf should be > 2.1V, so maybe blue leds?
3V3
D502
150060GS75000
R532
4.7 kΩ
LED3
C517
C518
C519
C520
C521
C522
C523
C524
100 nF
10 nF
GND
Consider resistor networks?
Sheet
RAM
Number
5/12
Project
Axiom micro rev3
Revision
0
Drawn by
anuejn & vup
License
CERN-OHL-S V2
Date
20200324
open source hardware



Sheet: plugins / shield	Number: 6/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN-OHL-S V2	open source hardware
Date: 20200324	

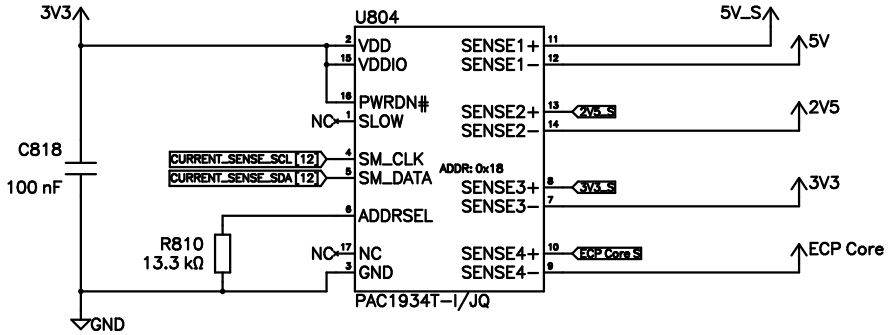


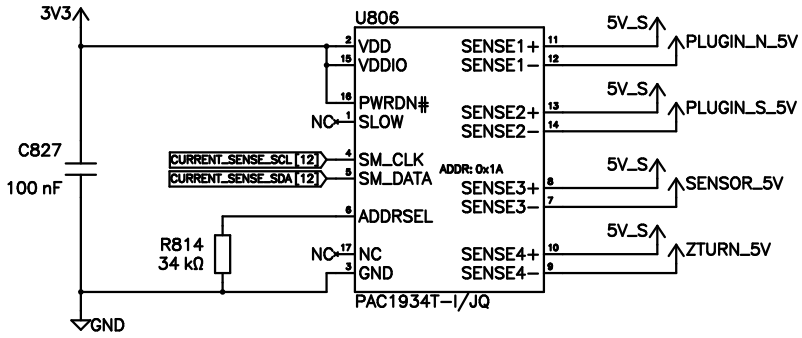
Sheet: USB	Number: 7/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN−OHL−S V2	
Date: 20200324	open source hardware

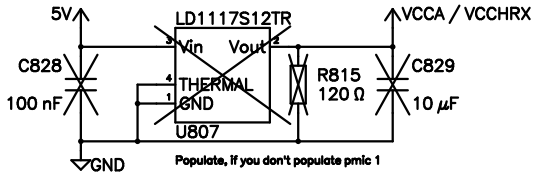


positive terminal of the VTT pin output capacitor(s) as a separate trace from the high–current path from VTT. Consider adding a low–pass R–C filter at the VTTSNS pin in case the ESR of the VTT output capacitor(s) is larger than 2 mΩ. The R–C filter time constant should be approximately the same or slightly lower than the time constant of the VTT output capacitance and ESR.

current sense resistors: 0805W8F100MT5E or CS05W8F100MT5E

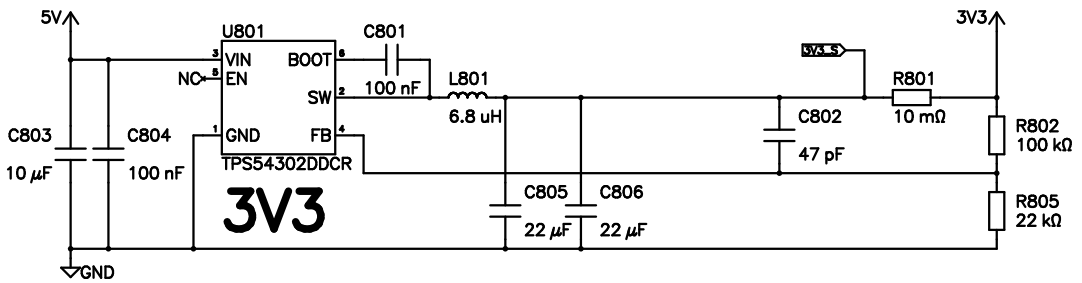


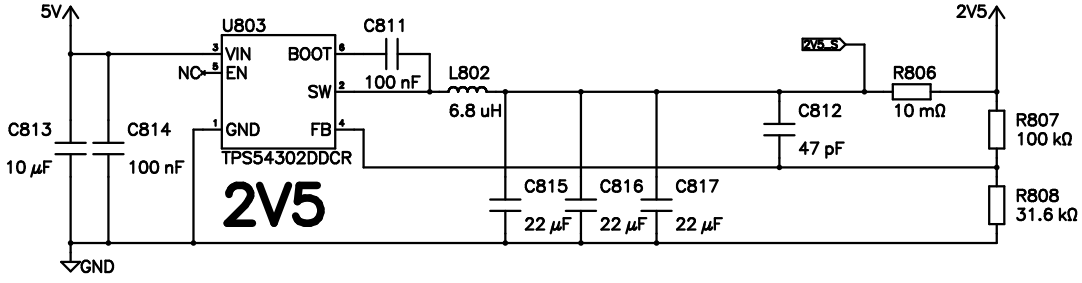


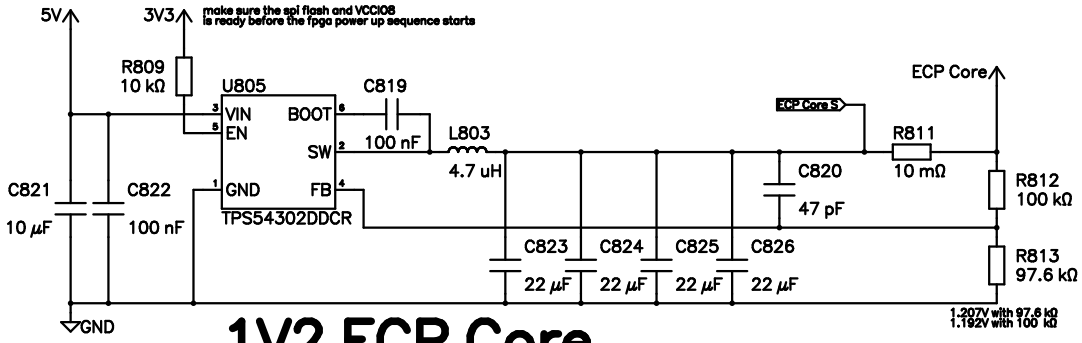


Populate, if you don't populate pmic 1

1V2 VCCA / VCCHRX

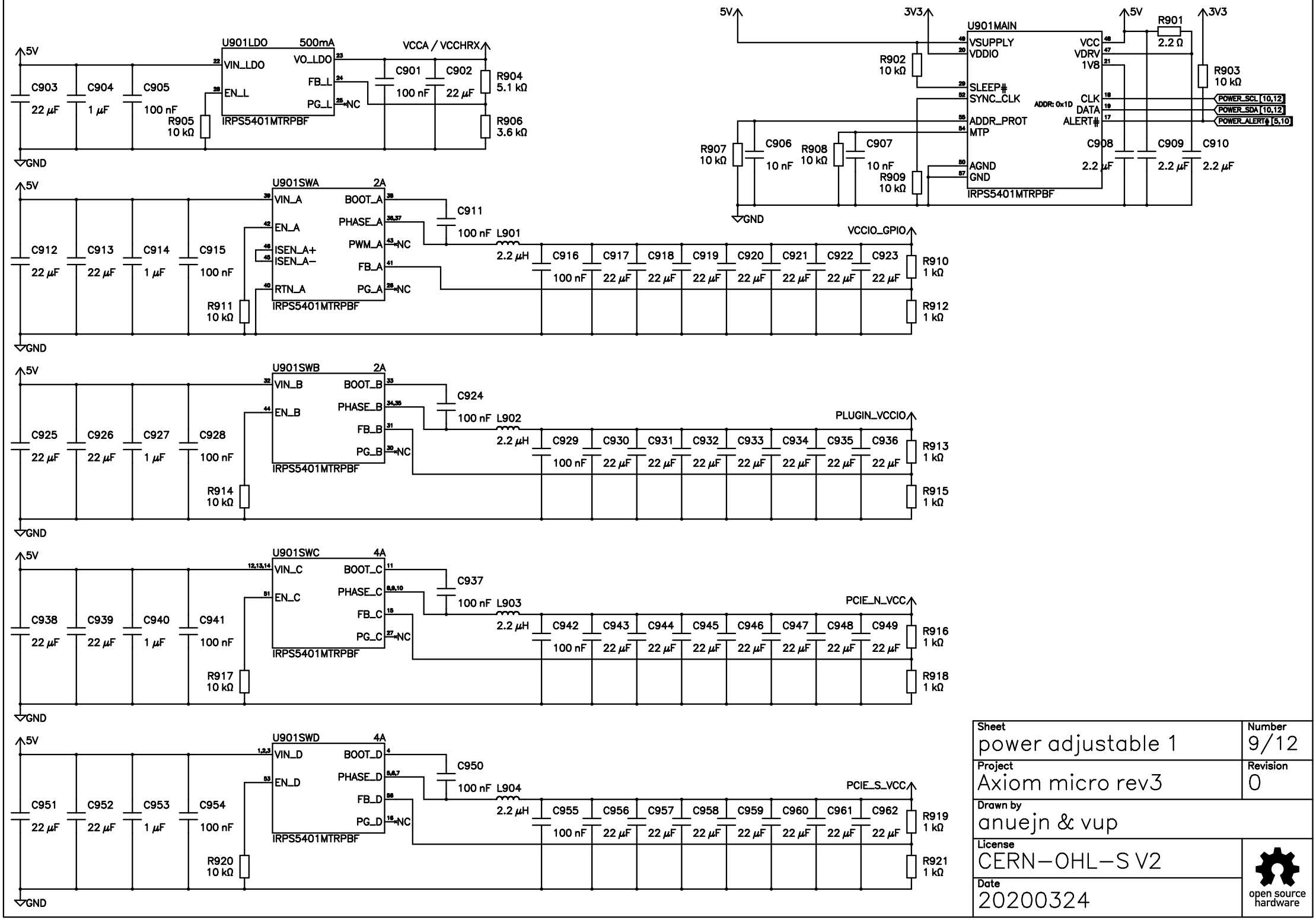


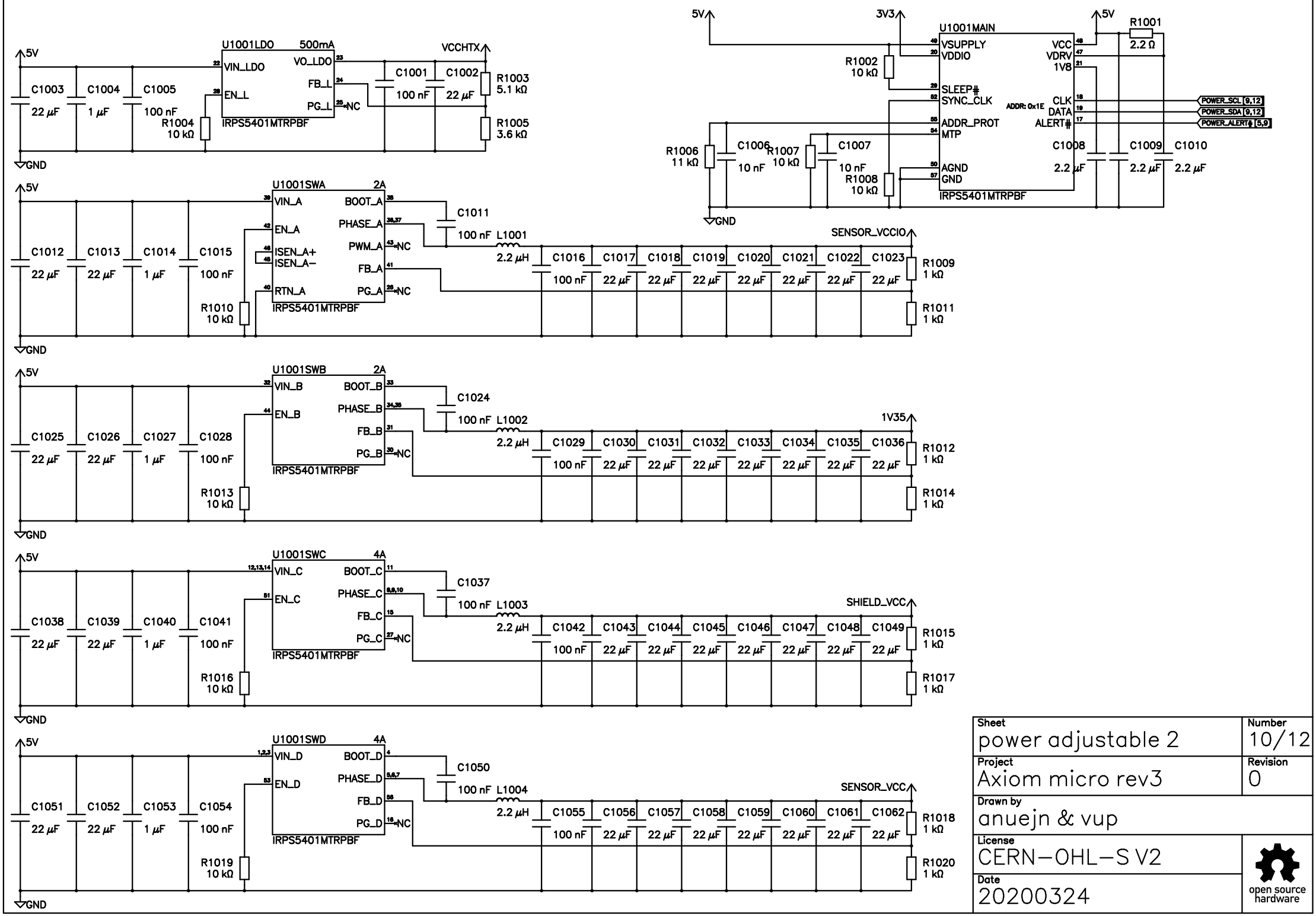




1V2 ECP Core

Sheet: power fixed / current sense	Number: 8/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
License: CERN–OHL–S V2	open source hardware
Date: 20200324	


U901LDO 500mA
VIN_LDO
EN_L
VO_LDO
FB_L
PG_L
NC
IRPS5401MTRPBF
VCCA / VCCHRX
C901 100 nF
C902 22 µF
R904 5.1 kΩ
R906 3.6 kΩ
R905 10 kΩ
C903 22 µF
C904 1 µF
C905 100 nF
U901MAIN
VSUPPLY
VDDIO
SLEEP#
SYNC_CLK
ADDR_PROT
MTP
AGND
GND
VCC
VDRV
1V8
CLK
DATA
ALERT#
ADDR: 0x1D
R901 2.2 Ω
R902 10 kΩ
R903 10 kΩ
R907 10 kΩ
R908 10 kΩ
R909 10 kΩ
C906 10 nF
C907 10 nF
C908 2.2 µF
C909 2.2 µF
C910 2.2 µF
POWER_SCL [10,12]
POWER_SDA [10,12]
POWER_ALERT# [5,10]
U901SWA 2A
VIN_A
EN_A
ISEN_A+
ISEN_A−
RTN_A
BOOT_A
PHASE_A
PWM_A
FB_A
PG_A
C911 100 nF
L901 2.2 µH
VCCIO_GPIO
C912 22 µF
C913 22 µF
C914 1 µF
C915 100 nF
C916 100 nF
C917 22 µF
C918 22 µF
C919 22 µF
C920 22 µF
C921 22 µF
C922 22 µF
C923 22 µF
R910 1 kΩ
R911 10 kΩ
R912 1 kΩ
U901SWB 2A
VIN_B
EN_B
BOOT_B
PHASE_B
FB_B
PG_B
C924 100 nF
L902 2.2 µH
PLUGIN_VCCIO
C925 22 µF
C926 22 µF
C927 1 µF
C928 100 nF
C929 100 nF
C930 22 µF
C931 22 µF
C932 22 µF
C933 22 µF
C934 22 µF
C935 22 µF
C936 22 µF
R913 1 kΩ
R914 10 kΩ
R915 1 kΩ
U901SWC 4A
VIN_C
EN_C
BOOT_C
PHASE_C
FB_C
PG_C
C937 100 nF
L903 2.2 µH
PCIE_N_VCC
C938 22 µF
C939 22 µF
C940 1 µF
C941 100 nF
C942 100 nF
C943 22 µF
C944 22 µF
C945 22 µF
C946 22 µF
C947 22 µF
C948 22 µF
C949 22 µF
R916 1 kΩ
R917 10 kΩ
R918 1 kΩ
U901SWD 4A
VIN_D
EN_D
BOOT_D
PHASE_D
FB_D
PG_D
C950 100 nF
L904 2.2 µH
PCIE_S_VCC
C951 22 µF
C952 22 µF
C953 1 µF
C954 100 nF
C955 100 nF
C956 22 µF
C957 22 µF
C958 22 µF
C959 22 µF
C960 22 µF
C961 22 µF
C962 22 µF
R919 1 kΩ
R920 10 kΩ
R921 1 kΩ
5V
3V3
GND
Sheet
power adjustable 1
Number
9/12
Project
Axiom micro rev3
Revision
0
Drawn by
anuejn & vup
License
CERN−OHL−S V2
Date
20200324
open source hardware



Sheet: power adjustable 2	Number: 10/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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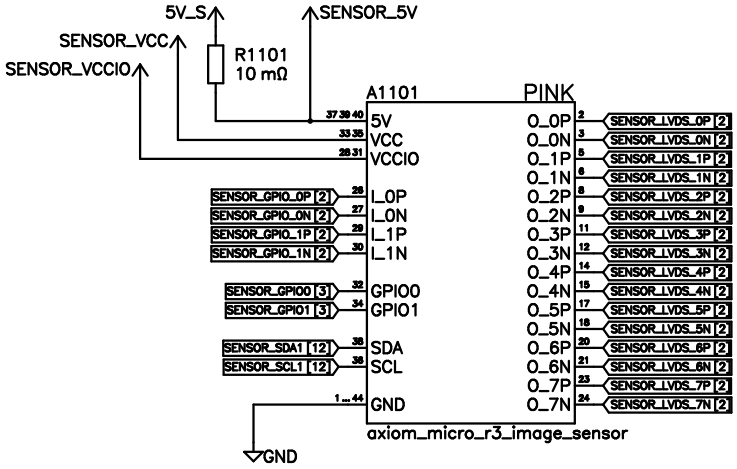
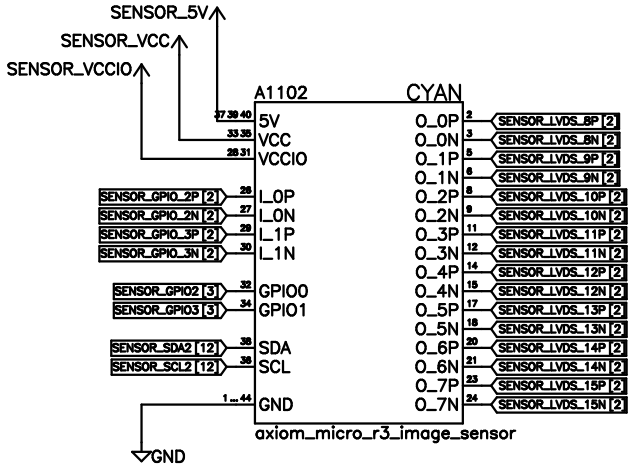
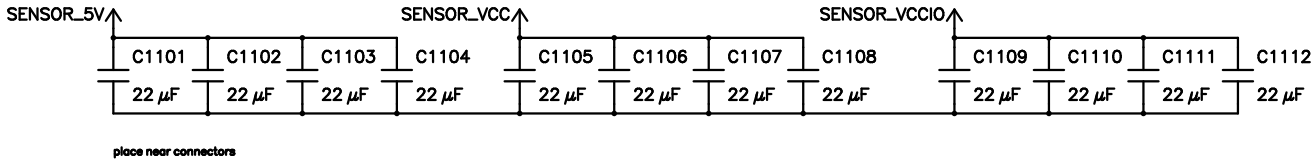
Date: 20200324	







Sheet: image sensor	Number: 11/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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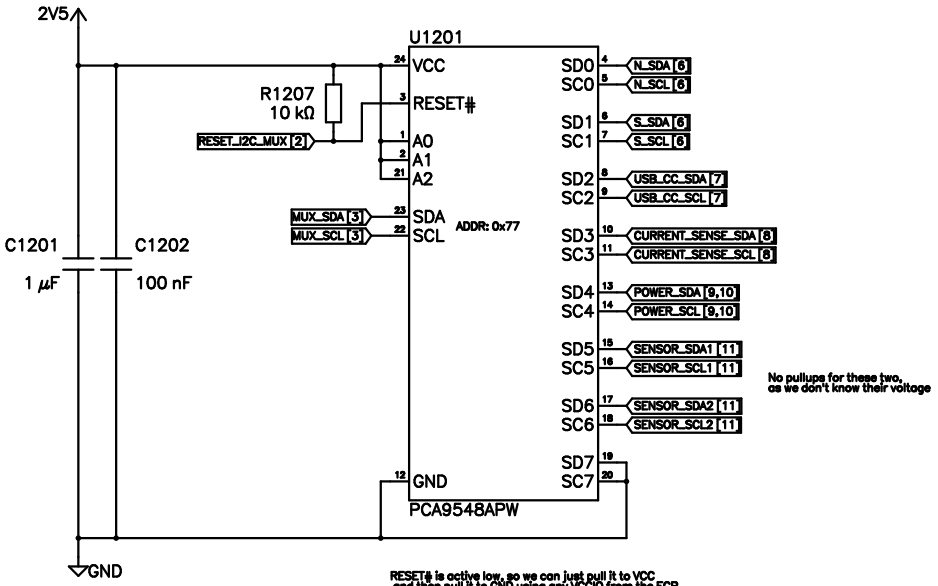
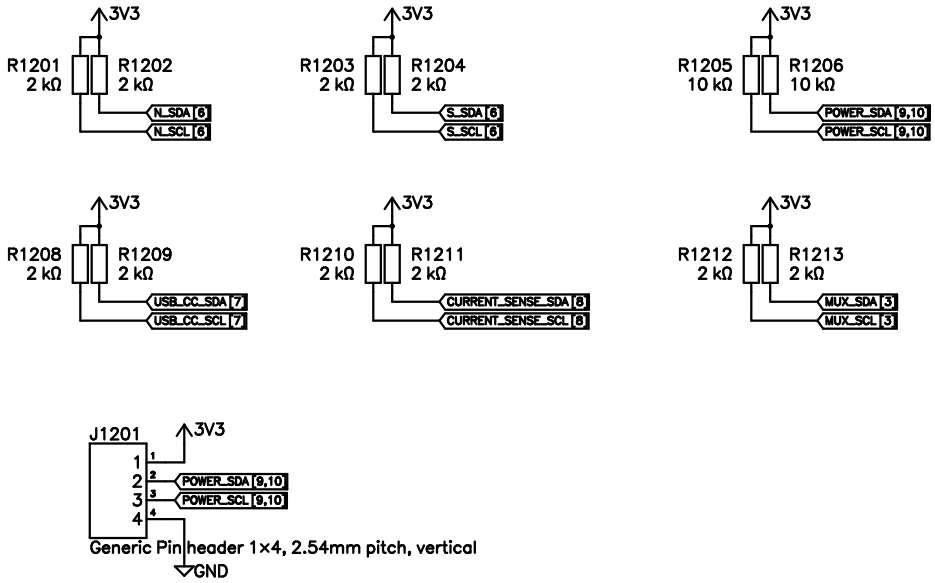
Date: 20200324	



RESET# is active low, so we can just pull it to VCC
and then pull it to GND using any VCCIO from the ECP.
attention has to be paid to not make RESET# get over VCC,
as otherwise current flows from the RESET pin to the VCC pin.
this should be accomplishable by just making the fpga output HI-Z
if it is not pullen low

2V5 VCC means about 1V8 voltage clamping by the pass through translators
That sholud work for most applications, we just need to be careful with nothing with 1V2 is on the bus

Unused channels have to be tied to GND or VCC



Sheet: i2c mux	Number: 12/12
Project: Axiom micro rev3	Revision: 0
Drawn by: anuejn & vup	
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Date: 20200324	