Dynamic Partial Self-Reconfiguration of Self-Aware Systems

Constantin Schieber, 01228774

***Abstract*—This work focuses on fault aspects of Self-Aware Systems. This includes a review of the types of faults that are occurring, methods for their detection and how one mitigate certain faults. One could argue that Network on Chips (NoCs) are Self-Aware too, as the nodes / controllers monitor the behavior of the throughput and can react accordingly to arising situations.**

I. Types of Faults

A. Transient Faults

- Single Event Upsets (SEUs), e.g. radiation induced [1], [2]
  - Change of logic state in memory cell
  - Commonly tackled by redundancy
  - Built-in fault detection unit possible
- Single Bit Errors (SBEs)
- Single Event Transients (SETs)
- Address Decoding Faults

Faults occur either in the interconnect of the Field Programmable Gate Array (FPGA) (which uses up to 80% of the available silicon) or in its actual logic blocks [1], [3].

B. Permanent Faults

- Time Dependant Dielectric Breakdowns (TDDBs)
- Electro Migration
- Hot Carrier Effect

II. Detection of Faults

A. Network on Chip

[4] introduces ways to test the fault tolerance of NoC.

B. Monitoring AXI-Core Traffic

[5] introduces the basis of cognitive reconfigurable hardware and presents a design that maintains a desired system performance by using run-time reconfiguration (RTR) and self-awareness. Self-awareness is achieved by monitoring and evaluating critical AXI-core metrics.

C. Duplication with Compare

[6] proposes a fault detection technique to detect open faults, Stuck-At faults and SEUs.

III. Mitigation of Faults

A. Network on Chip - make fault-tolerant per design

[7] adds additional network resources to a non-fault-tolerant design to mitigate interconnect faults.

[8] provides a case study on implementing a fault-tolerant routing algorithm and its monitoring mechanism.

B. Redundancy by need based replication

[9] tackles the problem of radiation by the creation of redundant modules - based on currently measured SEUs rates in on-chip memories.

C. Dynamic Partial Self-Reconfiguration

[6] goes on to propose system recovery by re-instantiating defective modules into the Partially Reconfigurable block.

[10] proposes a similar solution in the context of Electronic Control Units (ECUs).

[11] shows an approach on how to decide which configuration is currently desired in a multi-modal / multi-task System on Programmable Chip (SoPC).

Glossary

ECU Electronic Control Unit. 1

FPGA Field Programmable Gate Array. 1

NoC Network on Chip. 1

RTR Runtime Reconfiguration. 1

SEU Single Event Upset. 1

SoPC System on Programmable Chip (SoPC). 1

References

[1] G. I. Alkady, N. A. El-Araby, M. Abdelhalim, H. Amer, and A. Madian, "A fault-tolerant technique to detect and recover from open faults in FPGA interconnects," in *2014 14th Biennial Baltic Electronic Conference (BEC)*. IEEE, pp. 69–72. [Online]. Available: http://ieeexplore.ieee.org/document/7320558/

[2] K. Lee and S. S. Wong, "Fault-tolerant FPGA with column-based redundancy and power gating using RRAM," vol. 66, no. 6, pp. 946–956.

[3] Jing Huang, M. Tahoori, and F. Lombardi, "Routability and fault tolerance of FPGA interconnect architectures," in *2004 International Conferce on Test*. IEEE, pp. 479–488. [Online]. Available: http://ieeexplore.ieee.org/document/1386984/

[4] L. Sterpone, D. Sabena, and M. S. Reorda, "A new fault injection approach for testing network-on-chips," in *2012 20th Euromicro International Conference on Parallel, Distributed and Network-based Processing*, pp. 530–535.

[5] B. Navas, I. Sander, and J. ÃŰberg, "Towards cognitive reconfigurable hardware: Self-aware learning in RTR fault-tolerant SoCs," in *2015 10th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC)*, pp. 1–8.

[6] G. I. Alkady, N. A. El-Araby, M. B. Abdelhalim, H. H. Amer, and A. H. Madian, "Dynamic fault recovery using partial reconfiguration for highly reliable FPGAs," in *2015 4th Mediterranean Conference on Embedded Computing (MECO)*. IEEE, pp. 56–59. [Online]. Available: http://ieeexplore.ieee.org/document/7181865/

[7] S. Yesil, S. Tosun, and O. Ozturk, "FPGA implementation of a fault-tolerant application-specific NoC design," in *2016 International Conference on Design and Technology of Integrated Systems in Nanoscale Era (DTIS)*, pp. 1–6.

[8] Z. Lu, S. Y. Jiang, L. T. Huang, C. Wu, G. Luo, Q. Li, and G. M. Song, "The fault-tolerant NoC techniques with FPGA," in *2015 IEEE International Conference on Applied Superconductivity and Electromagnetic Devices (ASEMD)*, pp. 54–55.

[9] R. Glein, B. Schmidt, F. Rittner, J. Teich, and D. Ziener, "A self-adaptive SEU mitigation system for FPGAs with an internal block RAM radiation particle sensor," in *2014 IEEE 22nd Annual International Symposium on Field-Programmable Custom Computing Machines*, pp. 251–258.

[10] S. Shanker, "Enhancing automotive embedded systems with FPGAs," p. 249.

[11] D. Sharma, L. Kirischian, and V. Kirischian, "Run-time mitigation of power budget variations and hardware faults by structural adaptation of FPGA-based multi-modal SoPC," vol. 7, no. 4, p. 52. [Online]. Available: http://www.mdpi.com/2073-431X/7/4/52