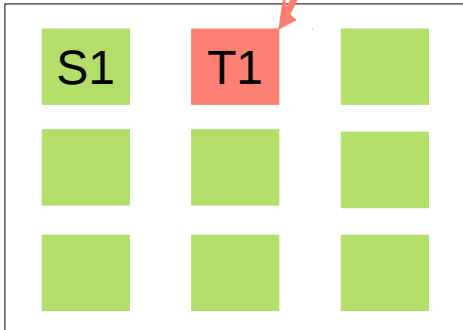


FPGA



$t+1$
→

FPGA

