

# Dynamic Partial Self-Reconfiguration of Self-Aware Systems

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**Abstract**—This work focuses on fault aspects of Self-Aware Systems. This includes a review of the types of faults that are occurring, methods for their detection and how one mitigate certain faults. One could argue that Network on Chips (NoCs) are Self-Aware too, as the nodes / controllers monitor the behavior of the throughput and can react accordingly to arising situations.

## I. TYPES OF FAULTS

### A. Transient Faults

- Single Event Upsets (SEUs), e.g. radiation induced [1], [2]
  - Change of logic state in memory cell
  - Commonly tackled by redundancy
  - Built-in fault detection unit possible
- Single Bit Errors (SBEs)
- Single Event Transients (SETs)
- Address Decoding Faults

Faults occur either in the interconnect of the Field Programmable Gate Array (FPGA) (which uses up to 80% of the available silicon) or in its actual logic blocks [1], [3].

### B. Permanent Faults

- Time Dependant Dielectric Breakdowns (TDDBs)
- Electro Migration
- Hot Carrier Effect

## II. DETECTION OF FAULTS

### A. Network on Chip

[4] introduces ways to test the fault tolerance of NoC.

### B. Monitoring AXI-Core Traffic

[5] introduces the basis of cognitive reconfigurable hardware and presents a design that maintains a desired system performance by using run-time reconfiguration (RTR) and self-awareness. Self-awareness is achieved by monitoring and evaluating critical AXI-core metrics.

### C. Duplication with Compare

[6] proposes a fault detection technique to detect open faults, Stuck-At faults and SEUs.

## III. MITIGATION OF FAULTS

### A. Network on Chip - make fault-tolerant per design

[7] adds additional network resources to a non-fault-tolerant design to mitigate interconnect faults.

[8] provides a case study on implementing a fault-tolerant routing algorithm and its monitoring mechanism.

### B. Redundancy by need based replication

[9] tackles the problem of radiation by the creation of redundant modules - based on currently measured SEUs rates in on-chip memories.

### C. Dynamic Partial Self-Reconfiguration

[6] goes on to propose system recovery by re-instantiating defective modules into the Partially Reconfigurable block.

[10] proposes a similar solution in the context of Electronic Control Units (ECUs).

[11] shows an approach on how to decide which configuration is currently desired in a multi-modal / multi-task System on Programmable Chip (SoPC).

## GLOSSARY

ECU Electronic Control Unit. 1

FPGA Field Programmable Gate Array. 1

NoC Network on Chip. 1

RTR Runtime Reconfiguration. 1

SEU Single Event Upset. 1

SoPC System on Programmable Chip (SoPC). 1

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