Table 5. High-density STM32F103xx pin definitions

Pins							_	(2)		Alternate fund	tions
BGA144	BGA100	WLCSP64	LQFP64	LQFP100	LQFP144	Pin name	Type <sup>(1)</sup>	I / O Level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Default	Remap
А3	А3	-	ı	1	1	PE2	I/O	FT	PE2	TRACECK/ FSMC_A23	
A2	ВЗ	-	-	2	2	PE3	I/O	FT	PE3	TRACED0/FSMC_A19	
B2	СЗ	-	ı	3	3	PE4	I/O	FT	PE4	TRACED1/FSMC_A20	
ВЗ	D3	-	ı	4	4	PE5	I/O	FT	PE5	TRACED2/FSMC_A21	
B4	E3	-	-	5	5	PE6	I/O	FT	PE6	TRACED3/FSMC_A22	
C2	B2	C6	1	6	6	V <sub>BAT</sub>	S		$V_{BAT}$		
A1	A2	C8	2	7	7	PC13-TAMPER- RTC <sup>(4)</sup>	I/O		PC13 <sup>(5)</sup>	TAMPER-RTC	
B1	A1	B8	3	8	8	PC14- OSC32_IN <sup>(4)</sup>	I/O		PC14 <sup>(5)</sup>	OSC32_IN	
C1	B1	В7	4	9	9	PC15- OSC32_OUT <sup>(4)</sup>	I/O		PC15 <sup>(5)</sup>	OSC32_OUT	
СЗ	-	-	-	-	10	PF0	I/O	FT	PF0	FSMC_A0	
C4	-	-	-	-	11	PF1	I/O	FT	PF1	FSMC_A1	
D4	-	-	-	-	12	PF2	I/O	FT	PF2	FSMC_A2	
E2	-	-	1	-	13	PF3	I/O	FT	PF3	FSMC_A3	
E3	-	1	1	-	14	PF4	I/O	FT	PF4	FSMC_A4	
E4	-	-	ı	ı	15	PF5	I/O	FΤ	PF5	FSMC_A5	
D2	C2	-	-	10	16	V <sub>SS_5</sub>	S		V <sub>SS_5</sub>		
D3	D2	-	1	11	17	V <sub>DD_5</sub>	S		$V_{DD_5}$		
F3	-	-	•	-	18	PF6	I/O		PF6	ADC3_IN4/FSMC_NIORD	
F2	-	-	-	-	19	PF7	I/O		PF7	ADC3_IN5/FSMC_NREG	
G3	-	-	1	-	20	PF8	I/O		PF8	ADC3_IN6/FSMC_NIOWR	
G2	-	-	ı	ı	21	PF9	I/O		PF9	ADC3_IN7/FSMC_CD	
G1	-	-	ı	-	22	PF10	I/O		PF10	ADC3_IN8/FSMC_INTR	
D1	C1	D8	5	12	23	OSC_IN	I		OSC_IN		
E1	D1	D7	6	13	24	OSC_OUT	0		OSC_OUT		
F1	E1	C7	7	14	25	NRST	I/O		NRST		
H1	F1	E8	8	15	26	PC0	I/O		PC0	ADC123_IN10	
H2	F2	F8	9	16	27	PC1	I/O		PC1	ADC123_IN11	
НЗ	E2	D6	10	17	28	PC2	I/O		PC2	ADC123_IN12	
H4	F3	-	11	18	29	PC3	I/O		PC3	ADC123_IN13	
J1	G1	E7	12	19	30	V <sub>SSA</sub>	S		V <sub>SSA</sub>		

Table 5. High-density STM32F103xx pin definitions (continued)

		Pir	าร					(2)		Alternate fund	tions
BGA144	BGA100	WLCSP64	LQFP64	LQFP100	LQFP144	Pin name	Type <sup>(1)</sup>	I / O Level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Default	Remap
K1	H1	-	-	20	31	$V_{REF}$	S		V <sub>REF-</sub>		
L1	J1	F7 (6)	-	21	32	$V_{REF+}$	s		V <sub>REF+</sub>		
M1	K1	G8	13	22	33	$V_{DDA}$	S		$V_{DDA}$		
J2	G2	F6	14	23	34	PA0-WKUP	I/O		PA0	WKUP/USART2_CTS <sup>(7)</sup> ADC123_IN0 TIM2_CH1_ETR TIM5_CH1/TIM8_ETR	
K2	H2	E6	15	24	35	PA1	I/O		PA1	USART2_RTS <sup>(7)</sup> ADC123_IN1/ TIM5_CH2/TIM2_CH2 <sup>(7)</sup>	
L2	J2	Н8	16	25	36	PA2	I/O		PA2	USART2_TX <sup>(7)</sup> /TIM5_CH3 ADC123_IN2/ TIM2_CH3 <sup>(7)</sup>	
M2	K2	G7	17	26	37	PA3	I/O		PA3	USART2_RX <sup>(7)</sup> /TIM5_CH4 ADC123_IN3/TIM2_CH4 <sup>(7)</sup>	
G4	E4	F5	18	27	38	V <sub>SS_4</sub>	S		V <sub>SS_4</sub>		
F4	F4	G6	19	28	39	V <sub>DD_4</sub>	S		V <sub>DD_4</sub>		
J3	G3	H7	20	29	40	PA4	I/O		PA4	SPI1_NSS <sup>(7)</sup> / USART2_CK <sup>(7)</sup> DAC_OUT1/ADC12_IN4	
K3	НЗ	E5	21	30	41	PA5	I/O		PA5	SPI1_SCK <sup>(7)</sup> DAC_OUT2 ADC12_IN5	
L3	J3	G5	22	31	42	PA6	I/O		PA6	SPI1_MISO <sup>(7)</sup> TIM8_BKIN/ADC12_IN6 TIM3_CH1 <sup>(7)</sup>	TIM1_BKIN
МЗ	КЗ	G4	23	32	43	PA7	I/O		PA7	SPI1_MOSI <sup>(7)</sup> / TIM8_CH1N/ADC12_IN7 TIM3_CH2 <sup>(7)</sup>	TIM1_CH1N
J4	G4	H6	24	33	44	PC4	I/O		PC4	ADC12_IN14	
K4	H4	H5	25	34	45	PC5	I/O		PC5	ADC12_IN15	
L4	J4	H4	26	35	46	PB0	I/O		PB0	ADC12_IN8/TIM3_CH3 TIM8_CH2N	TIM1_CH2N
M4	K4	F4	27	36	47	PB1	I/O		PB1	ADC12_IN9/TIM3_CH4 <sup>(7)</sup> TIM8_CH3N	TIM1_CH3N
J5	G5	НЗ	28	37	48	PB2	I/O	FT	PB2/BOOT1		
M5	-	-	-	-	49	PF11	I/O	FT	PF11	FSMC_NIOS16	
L5	-	-	-	-	50	PF12	I/O	FT	PF12	FSMC_A6	·
H5	-	-	-	-	51	$V_{SS\_6}$	S		$V_{SS\_6}$		

Table 5. High-density STM32F103xx pin definitions (continued)

		Pir	าร					(2)		Alternate fund	tions
BGA144	BGA100	WLCSP64	LQFP64	LQFP100	LQFP144	Pin name	Type <sup>(1)</sup>	1 / O Level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Default	Remap
G5	-	-	-	-	52	$V_{DD_6}$	S		V <sub>DD_6</sub>		
K5	-	-	-	-	53	PF13	I/O	FT	PF13	FSMC_A7	
M6	-	-	-	-	54	PF14	I/O	FT	PF14	FSMC_A8	
L6	-	-	-	-	55	PF15	I/O	FT	PF15	FSMC_A9	
K6	-	ı	-	-	56	PG0	I/O	FT	PG0	FSMC_A10	
J6	-	-	-	-	57	PG1	I/O	FT	PG1	FSMC_A11	
M7	H5	-	-	38	58	PE7	I/O	FT	PE7	FSMC_D4	TIM1_ETR
L7	J5	-	-	39	59	PE8	I/O	FT	PE8	FSMC_D5	TIM1_CH1N
K7	K5	-	-	40	60	PE9	I/O	FT	PE9	FSMC_D6	TIM1_CH1
H6	-	•	-	-	61	V <sub>SS_7</sub>	s		V <sub>SS_7</sub>		
G6	-	1	-	-	62	V <sub>DD_7</sub>	S		V <sub>DD_7</sub>		
J7	G6	-	-	41	63	PE10	I/O	FT	PE10	FSMC_D7	TIM1_CH2N
H8	H6	-	-	42	64	PE11	I/O	FT	PE11	FSMC_D8	TIM1_CH2
J8	J6	-	-	43	65	PE12	I/O	FT	PE12	FSMC_D9	TIM1_CH3N
K8	K6	-	-	44	66	PE13	I/O	FT	PE13	FSMC_D10	TIM1_CH3
L8	G7	-	-	45	67	PE14	I/O	FT	PE14	FSMC_D11	TIM1_CH4
M8	H7	-	-	46	68	PE15	I/O	FT	PE15	FSMC_D12	TIM1_BKIN
M9	J7	G3	29	47	69	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX <sup>(7)</sup>	TIM2_CH3
M10	K7	F3	30	48	70	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX <sup>(7)</sup>	TIM2_CH4
H7	<b>E</b> 7	H2	31	49	71	V <sub>SS_1</sub>	S		V <sub>SS_1</sub>		
G7	F7	H1	32	50	72	$V_{\mathrm{DD}\_1}$	S		V <sub>DD_1</sub>		
M11	K8	G2	33	51	73	PB12	I/O	FT	PB12	SPI2_NSS/I2S2_WS/ I2C2_SMBA/ USART3_CK <sup>(7)</sup> / TIM1_BKIN <sup>(7)</sup>	
M12	J8	G1	34	52	74	PB13	I/O	FT	PB13	SPI2_SCK/I2S2_CK USART3_CTS <sup>(7)</sup> / TIM1_CH1N	
L11	H8	F2	35	53	75	PB14	I/O	FT	PB14	SPI2_MISO/TIM1_CH2N USART3_RTS <sup>(7)</sup>	
L12	G8	F1	36	54	76	PB15	I/O	FT	PB15	SPI2_MOSI/I2S2_SD TIM1_CH3N <sup>(7)</sup>	
L9	K9	_	1	55	77	PD8	I/O	FT	PD8	FSMC_D13	USART3_TX
K9	J9	-	-	56	78	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX
J9	H9	-	-	57	79	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK

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Table 5. High-density STM32F103xx pin definitions (continued)

Iabi	Pins					,			,	Alternate fund	ctions
BGA144	BGA100	WLCSP64	LQFP64	LQFP100	LQFP144	Pin name	Type <sup>(1)</sup>	I / O Level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Default	Remap
H9	G9	-	ı	58	80	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS
L10	K10		1	59	81	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1 / USART3_RTS
K10	J10	-	ı	60	82	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2
G8	-	-	1	-	83	$V_{\rm SS\_8}$	S		$V_{SS\_8}$		
F8	-	-	ı	ı	84	$V_{DD_8}$	S		$V_{DD_8}$		
K11	H10		1	61	85	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3
K12	G10	-	1	62	86	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4
J12	,	1	1	-	87	PG2	I/O	FT	PG2	FSMC_A12	
J11	-	-	-	-	88	PG3	I/O	FT	PG3	FSMC_A13	
J10	-	-	-	-	89	PG4	I/O	FT	PG4	FSMC_A14	
H12	-	-	1	-	90	PG5	I/O	FT	PG5	FSMC_A15	
H11	-	-	-	-	91	PG6	I/O	FT	PG6	FSMC_INT2	
H10	-	-	ı	-	92	PG7	I/O	FT	PG7	FSMC_INT3	
G11	-	-	1	-	93	PG8	I/O	FT	PG8		
G10	-	-	-	-	94	V <sub>SS_9</sub>	s		V <sub>SS_9</sub>		
F10	-	-	1	-	95	V <sub>DD_9</sub>	S		V <sub>DD_9</sub>		
G12	F10	E1	37	63	96	PC6	I/O	FT	PC6	I2S2_MCK/ TIM8_CH1/SDIO_D6	TIM3_CH1
F12	E10	E2	38	64	97	PC7	I/O	FT	PC7	I2S3_MCK/ TIM8_CH2/SDIO_D7	TIM3_CH2
F11	F9	E3	39	65	98	PC8	I/O	FT	PC8	TIM8_CH3/SDIO_D0	TIM3_CH3
E11	E9	D1	40	66	99	PC9	I/O	FT	PC9	TIM8_CH4/SDIO_D1	TIM3_CH4
E12	D9	E4	41	67	100	PA8	I/O	FT	PA8	USART1_CK/ TIM1_CH1 <sup>(7)</sup> /MCO	
D12	C9	D2	42	68	101	PA9	I/O	FT	PA9	USART1_TX <sup>(7)</sup> / TIM1_CH2 <sup>(7)</sup>	
D11	D10	D3	43	69	102	PA10	I/O	FT	PA10	USART1_RX <sup>(7)</sup> / TIM1_CH3 <sup>(7)</sup>	
C12	C10	C1	44	70	103	PA11	I/O	FT	PA11	USART1_CTS/USBDM CAN_RX <sup>(7)</sup> /TIM1_CH4 <sup>(7)</sup>	
B12	B10	C2	45	71	104	PA12	I/O	FT	PA12	USART1_RTS/USBDP/ CAN_TX <sup>(7)</sup> /TIM1_ETR <sup>(7)</sup>	
A12	A10	D4	46	72	105	PA13	I/O	FT	JTMS- SWDIO		PA13

Table 5. High-density STM32F103xx pin definitions (continued)

		Pir	าร					(2)		Alternate functions		
BGA144	BGA100	WLCSP64	LQFP64	LQFP100	LQFP144	Pin name	Type <sup>(1)</sup>	1/0 Level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Default	Remap	
C11	F8	-	-	73	106				Not connected	d		
G9	E6	B1	47	74	107	$V_{SS_2}$	S		V <sub>SS_2</sub>			
F9	F6	A1	48	75	108	$V_{DD_2}$	S		V <sub>DD_2</sub>			
A11	<b>A</b> 9	B2	49	76	109	PA14	I/O	FT	JTCK- SWCLK		PA14	
A10	A8	СЗ	50	77	110	PA15	I/O	FT	JTDI	SPI3_NSS/ I2S3_WS	TIM2_CH1_ETR PA15 / SPI1_NSS	
B11	В9	A2	51	78	111	PC10	I/O	FT	PC10	UART4_TX/SDIO_D2	USART3_TX	
B10	В8	ВЗ	52	79	112	PC11	I/O	FT	PC11	UART4_RX/SDIO_D3	USART3_RX	
C10	C8	C4	53	80	113	PC12	I/O	FT	PC12	UART5_TX/SDIO_CK	USART3_CK	
E10	D8	D8	5	81	114	PD0	I/O	FT	OSC_IN <sup>(8)</sup>	FSMC_D2 <sup>(9)</sup>	CAN_RX	
D10	E8	D7	6	82	115	PD1	I/O	FT	OSC_OUT <sup>(8)</sup>	FSMC_D3 <sup>(9)</sup>	CAN_TX	
E9	В7	А3	54	83	116	PD2	I/O	FT	PD2	TIM3_ETR/UART5_RX SDIO_CMD		
D9	C7	-	-	84	117	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS	
C9	D7	-	-	85	118	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS	
В9	В6	-	-	86	119	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX	
E7	-	-	-	-	120	V <sub>SS_10</sub>	S		V <sub>SS_10</sub>			
F7	-	-	-	-	121	V <sub>DD_10</sub>	S		V <sub>DD_10</sub>			
A8	C6	-	-	87	122	PD6	I/O	FT	PD6	FSMC_NWAIT	USART2_RX	
A9	D6	-	-	88	123	PD7	I/O	FT	PD7	FSMC_NE1/FSMC_NCE2	USART2_CK	
E8	-	-	-	-	124	PG9	I/O	FT	PG9	FSMC_NE2/FSMC_NCE3		
D8	-	-	-	-	125	PG10	I/O	FT	PG10	FSMC_NCE4_1/ FSMC_NE3		
C8	-	-	-	-	126	PG11	I/O	FT	PG11	FSMC_NCE4_2		
В8	-	-	-	-	127	PG12	I/O	FT	PG12	FSMC_NE4		
D7	-	-	-	-	128	PG13	I/O	FT	PG13	FSMC_A24		
C7	-	-	-	-	129	PG14	I/O	FT	PG14	FSMC_A25		
E6	-	-	-	-	130	V <sub>SS_11</sub>	S		V <sub>SS_11</sub>			
F6	-	-	-	-	131	V <sub>DD_11</sub>	S		V <sub>DD_11</sub>			
B7	-	-	-	-	132	PG15	I/O	FT	PG15			
A7	A7	A4	55	89	133	PB3/	I/O	FT	JTDO	SPI3_SCK / I2S3_CK/	PB3/TRACESWO TIM2_CH2 / SPI1_SCK	

Table 5.	High-density	/ STM32F103xx	pin definitions (	(continued)

		Pir	าร					(2)	B4	Alternate functions		
BGA144	BGA100	WLCSP64	LQFP64	LQFP100	LQFP144	Pin name	Type <sup>(1)</sup>	I / O Level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Default	Remap	
A6	A6	B4	56	90	134	PB4	I/O	FT	NJTRST	SPI3_MISO	PB4 / TIM3_CH1 SPI1_MISO	
В6	C5	<b>A</b> 5	57	91	135	PB5	I/O		PB5	I2C1_SMBA/ SPI3_MOSI I2S3_SD	TIM3_CH2 / SPI1_MOSI	
C6	B5	B5	58	92	136	PB6	I/O	FT	PB6	I2C1_SCL <sup>(7)</sup> / TIM4_CH1 <sup>(7)</sup>	USART1_TX	
D6	<b>A</b> 5	C5	59	93	137	PB7	I/O	FT	PB7	I2C1_SDA <sup>(7)</sup> / FSMC_NADV / TIM4_CH2 <sup>(7)</sup>	USART1_RX	
D5	D5	A6	60	94	138	ВООТ0	I		воото			
C5	B4	D5	61	95	139	PB8	I/O	FT	PB8	TIM4_CH3 <sup>(7)</sup> /SDIO_D4	I2C1_SCL/ CAN_RX	
B5	A4	В6	62	96	140	PB9	I/O	FT	PB9	TIM4_CH4 <sup>(7)</sup> /SDIO_D5	I2C1_SDA / CAN_TX	
A5	D4	-	-	97	141	PE0	I/O	FT	PE0	TIM4_ETR / FSMC_NBL0		
A4	C4	-	-	98	142	PE1	I/O	FT	PE1	FSMC_NBL1		
E5	E5	A7	63	99	143	$V_{SS\_3}$	S		V <sub>SS_3</sub>			
F5	F5	A8	64	100	144	$V_{DD\_3}$	S		V <sub>DD_3</sub>			

- 1. I = input, O = output, S = supply, HiZ = high impedance.
- 2. FT = 5 V tolerant.
- 3. Function availability depends on the chosen device.
- 4. PC13, PC14 and PC15 are supplied through the power switch and since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 is restricted: only one I/O at a time can be used as an output, the speed has to be limited to 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
- 5. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
- 6. Unlike in the LQFP64 package, there is no PC3 in the WLCSP package. The V<sub>REF+</sub> functionality is provided instead.
- 7. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
- 8. For the LQFP64 package, the pins number 5 and 6 are configured as OSC\_IN/OSC\_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100/BGA100 and LQFP144/BGA144 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
- 9. For devices delivered in LQFP64 packages, the FSMC function is not available.

Table 6. FSMC pin definition

lable 6.	L2MC b	oin aetiniti	OII				
			FSM	C		LOED100	
Pins	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	LQFP100 BGA100 <sup>(1)</sup>	
PE2			A23	A23		Yes	
PE3			A19	A19		Yes	
PE4			A20	A20		Yes	
PE5			A21	A21		Yes	
PE6			A22	A22		Yes	
PF0	A0	A0	A0			-	
PF1	A1	A1	A1			-	
PF2	A2	A2	A2			-	
PF3	А3		A3			-	
PF4	A4		A4			-	
PF5	A5		A5			-	
PF6	NIORD	NIORD				-	
PF7	NREG	NREG				-	
PF8	NIOWR	NIOWR				-	
PF9	CD	CD				-	
PF10	INTR	INTR				-	
PF11	NIOS16	NIOS16				-	
PF12	A6		A6			-	
PF13	A7		A7			-	
PF14	A8		A8			-	
PF15	A9		A9			-	
PG0	A10		A10			-	
PG1			A11			-	
PE7	D4	D4	D4	DA4	D4	Yes	
PE8	D5	D5	D5	DA5	D5	Yes	
PE9	D6	D6	D6	DA6	D6	Yes	
PE10	D7	D7	D7	DA7	D7	Yes	
PE11	D8	D8	D8	DA8	D8	Yes	
PE12	D9	D9	D9	DA9	D9	Yes	
PE13	D10	D10	D10	DA10	D10	Yes	
PE14	D11	D11	D11	DA11	D11	Yes	
PE15	D12	D12	D12	DA12	D12	Yes	
PD8	D13	D13	D13	DA13	D13	Yes	
			1	1	I	l	

Table 6. FSMC pin definition (continued)

			FSM	C		LOED100
Pins	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	LQFP100 BGA100 <sup>(1)</sup>
PD9	D14	D14	D14	DA14	D14	Yes
PD10	D15	D15	D15	DA15	D15	Yes
PD11			A16	A16	CLE	Yes
PD12			A17	A17	ALE	Yes
PD13			A18	A18		Yes
PD14	D0	D0	D0	DA0	D0	Yes
PD15	D1	D1	D1	DA1	D1	Yes
PG2			A12			-
PG3			A13			-
PG4			A14			-
PG5			A15			-
PG6					INT2	-
PG7					INT3	-
PD0	D2	D2	D2	DA2	D2	Yes
PD1	D3	D3	D3	DA3	D3	Yes
PD3			CLK	CLK		Yes
PD4	NOE	NOE	NOE	NOE	NOE	Yes
PD5	NWE	NWE	NWE	NWE	NWE	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	NWAIT	Yes
PD7			NE1	NE1	NCE2	Yes
PG9			NE2	NE2	NCE3	-
PG10	NCE4_1	NCE4_1	NE3	NE3		-
PG11	NCE4_2	NCE4_2				-
PG12			NE4	NE4		-
PG13			A24	A24		-
PG14			A25	A25		-
PB7			NADV	NADV		Yes
PE0			NBL0	NBL0		Yes
PE1			NBL1	NBL1		Yes

<sup>1.</sup> Ports F and G are not available in devices delivered in 100-pin packages.

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## 4 Memory mapping

The memory map is shown in Figure 9.

Figure 9. Memory map

