Software Requirement Specification (SWE1)

Revisions

Version	Author	Description	Date
v1.0.0	*Hairu Mossa*		*28/09/2025*

Document Approvals

Role	Name	Signature	Date

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1. Introduction

1.1 Purpose

The purpose of this document is to specify the software-level requirements derived from the system requirements for the Buck Converter Control System.

1.2 Scope

This specification covers the software components implemented in layered architecture:

- Application Layer (state machine, error handling, telemetry scheduler).
- Controller Layer (PI/PID control logic).
- Interface Layer (abstraction for ADC, PWM, CAN, Timer).
- System Layer (hardware drivers and HAL functions).

1.5 Overview

[Instruction: Describe the content and organization of the rest of the SyRS document. Explain how the document is structured to help the reader understand it.]

2. Specific Requirements

2.1 Functional Requirements

SWR_0001: The software shall read output voltage and output current from ADC via *adc_controller_get_output_voltage()* and *adc_controller_get_output_current()* function.
SWR_0002: The software shall implement a PI/PID algorithm in *pid_controller_update*() to compute the PWM duty cycle.
SWR_0003: The software shall clamp PWM duty cycle values between 0% and 95% before writing to hardware via *if_pwm_set_duty_cycle*().
SWR_0004: The software shall limit output current by reducing duty cycle if measured current > 10A.
SWR_0005: The software shall package telemetry data (voltages, currents, temperature, state, error flags) into a CAN frame and transmit every 100 ms.
SWR_0006: The software shall log abnormal conditions in a global error handler and periodically transmit error status via CAN.

2.3 Performance Requirements

SWR_0007: The control task shall execute at 10 kHz, triggered by *if_timer_check_control_flag*()
SWR_0008: The PWM carrier shall run at 20 kHz.
SWR_0010: ADC sampling resolution shall be 12-bit

2.4 Error Handling

SWR_0011: The software shall detect overcurrent, ADC failure, and PID instability and transition system state to ERROR.
SWR_0012: The system shall continue broadcasting error telemetry while in ERROR state.

3. Traceability Matrix

Software Requirement (SWR)	Description	Parent System Requirement (SYS)
SWR_0001	Read voltage/current from ADC	SYS_0001
SWR_0002	Implement PI/PID controller	SYS_0002
SWR_0003	Clamp duty cycle 0–95%	SYS_0003
SWR_0004	Current limiting at 10A	SYS_0004
SWR_0005	CAN telemetry @ 100 ms	SYS_0005
SWR_0006	Global error handling + CAN report	SYS_0006
SWR_0007	Control loop @ 10 kHz	SYS_0010
SWR_0008	PWM frequency @ 20 kHz	SYS_0011
SWR_0009	Telemetry loop @ 10 Hz	SYS_0012
SWR_0010	ADC resolution = 12-bit	SYS_0013
SWR_0011	Error detection & state transition	SYS_0018
SWR_0012	Error telemetry in ERROR mode	SYS_0019