Assignment 3

Haiyu Wang

1. Configuration File:

hw3opts.py

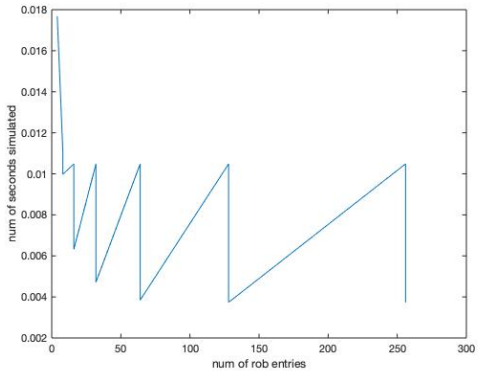
```
from m5 import fatal
import m5.objects
from textwrap import TextWrapper

#add options for number of ROB entries, IQ entries, and number of
physical
#floating point registers
def addHW3Opts(parser):
  parser.add_option("--num-rob-entries", type="int",
default=192,dest="num_rob_entries");
  parser.add_option("--num-iq-entries", type="int",
default=64,dest="num_iq_entries");
  parser.add_option("--num-phys-float-regs", type="int",
default=256,dest="num_phys_float_regs");

#set parameters taken in from options on command line
def set_config(cpu_list, options):
  for cpu in cpu_list:
    cpu.numROBEntries = options.num_rob_entries
    cpu.numIQEntries = options.num_iq_entries
    cpu.numPhysFloatRegs = options.num_phys_float_regs
    # set parameters for each thing
```

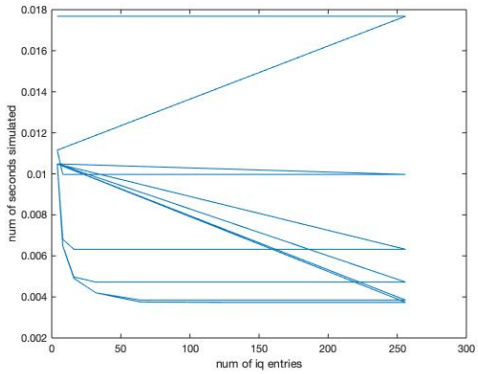
script

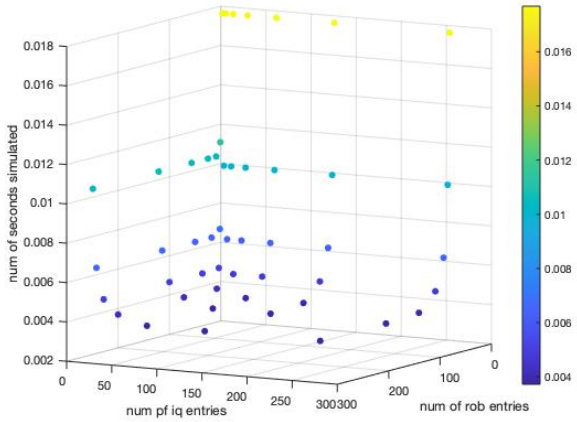
```
for i in 4 8 16 32 64 128 256
do
    for j in 4 8 16 32 64 128 256
    do
        for k in 256 512 1024 2048 4096
        do
        $GEM5/build/ARM/gem5.opt          --outdir=out${i}_${j}_${k}
hw3config.py  -c  $GEM5/../test_progs/daxpy/daxpy_arm_big  --cpu-
type="DerivO3CPU" --caches --l2cache --num-phys-float-regs=$k --
num-rob-entries=$i --num-iq-entries=$j
        done
    done
done
```

2. Result

a) Simulated time

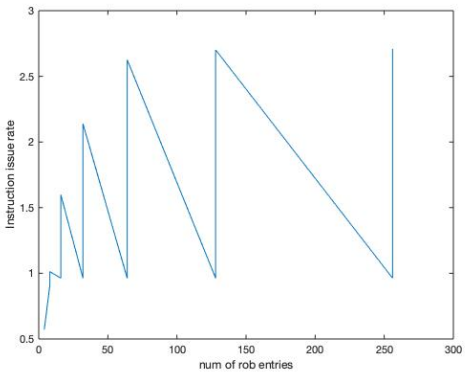


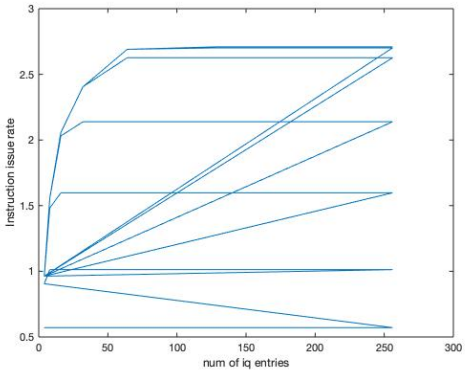


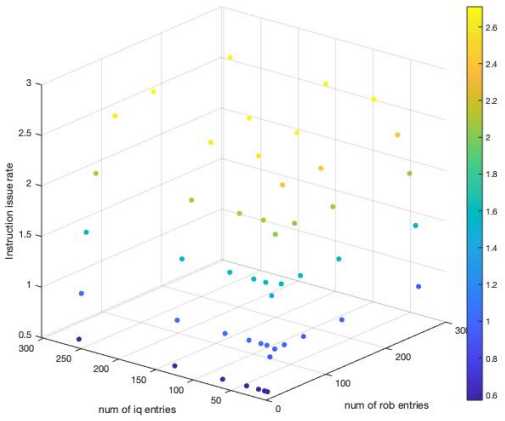


As we can see from the diagram, simulated time is influenced by both the number of ROB entries and number of issue queue entries. With the increase of the number of ROB entries and number of issue queue entries, the simulated time decreases. When the number of issue queue entries is smaller than the number of ROB entries, the simulated time decrease with the increase of the number of issue queue entries. After the number of the issue queue entries surpass the number of the ROB entries, the simulated time will remain the same.

b) Instructions Issue Rate

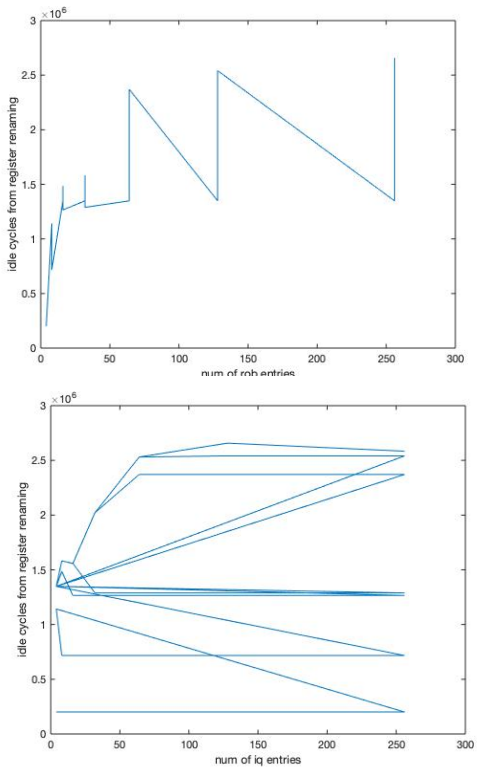


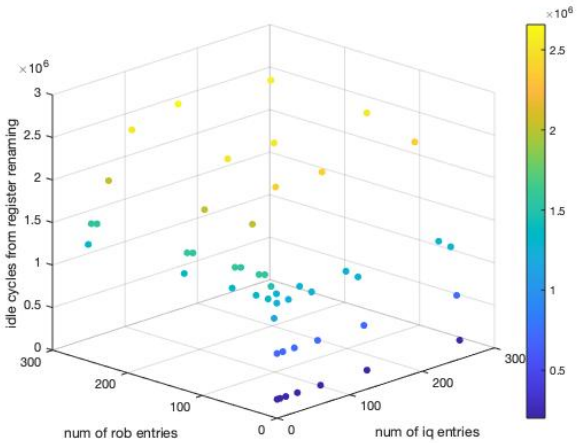




As we can see from the diagrams, the instruction issue rate is also determined by the number of ROB entries and the number of issue queue entries. With the increase of these 2 parameters, the instruction issue rate also increases. Also, the ROB entries and the issue queue entries place some limits to each other, which means, when one of the parameters surpasses the other one, the instruction of issue rate will not increase though the larger parameter still increase.

c) Idle Cycles from Register Renaming





As we can see from the diagrams, the idle cycles from register renaming also increase when the number of ROB entries and the number of issue queue entries increase. The trend of the idle cycles from register renaming is almost the same as above.

3. Conclusion

The simulated time decrease, the instructions issue rate and the idle cycles from register renaming increase when the number of ROB entries and the number of issue queue entries increase, because more ROB entries and more issue queue entries means more instruction able to be issued. Thus, the instructions issue rate will definitely increase and then lead to the simulated time decrease. However, these 2 parameters also place some limits to each other. When one of the parameters surpasses the other one, the simulated time, the instructions issue rate and the idle cycles from register renaming will remain the same even though the larger one still increases, because these 2 parameters decide the instructions issued in a unit of time jointly.

In the simulation the number of physical floating registers has little impact on

the chosen parameters, but as the parameter fp_rename_lookups is missing, the impact of the number of physical floating registers needs more strategies to analyze.