Hakam Atassi

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Research Interests Computer Architecture, High Performance Computing, Architecture for Sparsity, Model Compression, Hardware Security, FPGAs

Education

McMaster University, Hamilton, ON — Sept 2020 - Apr 2025
B.Eng, Computer Engineering & CO-OP, Year 4 — GPA: 11.6/12.0

Awards & Grants Provost 2022, Dean's List 2022, Deans List 2021

Conferences Micro 56, Toronto, ON

Tools & Frameworks Xilinx Vivado, Cadence Xcelium & Virtuoso, Synopsys Design Compiler, Gem5, Chipyard, Verilator, OpenCL

Courses MIT 6.888- Secure Hardware Design, MIT 6.5940- Efficient Deep Learning Computing

Publications Hakam Atassi "Adapting CISC Style Structured SPMM kernels for RVV 1.0" ArcXiv etc…

Research Experience

SwiftWare Lab, Supervised by Dr. Cheshmi

- ◊ Extended an open source RISC-V core to support vector multiply & fused-multiply add instructions
- ◊ Modelled the performance of single threaded SIMD and SISD GEMM kernels on the core in simulation
- ◊ Compared the resulting performance metrics against a similar configuration in Gem5 to confirm validity of the results
- ◊ Modeled the performance of a Gustavson based SIMD SPMM kernel for use as a baseline
- ◊ Extended the core to support a custom *vindexmac* instruction based on a "DATE" publication to enable a B stationary SPMM kernel
- ◊ Adapted the *vindexmac* algorithm through binning and dynamic tiling to optimize performance on the proposed RVV 1.0 specification

Work Experience

The Six Semiconductor

- ◊ Developed firmware for an LPDDR5 PHY test chip to minimize bring up & signal integrity latency
- ◊ Developed a software simulation and verification tool to aid in the optimization of an analog phase detection and correction circuit
- ◊ Developed and deployed various clock gating scripts, tool updates/workarounds and workflow scripts

Projects

RISC-V, Supervised by Dr. Nicolici

- ◊ Contributed to the design of a fully parameterizable L1 cache subsystem for a dual core RISC-V CPU for synthesis on an Altera FPGA
- ◊ Built a golden model for the cache in python for verification using the Cocotb framework
- ◊ Gave an extended workshop on the Chipyard flow, starting with an intro to Chisel and ending with simulating a custom Boom core with Verilator
- ◊ Invited and hosted Matt Venn from the open source EDA community to introduce FOSS ASIC tools

Image Decompression Core

- ◊ Implemented a Verilog DSP core to decompress a JPEG image received via bitstream and buffered in on chip SRAM
- ◊ Fully pipelined the design to achieve a multiplier utilization of 80% between at stages
- ◊ Applied fundamental DSP concepts, including converting images from the frequency domain to the chrominance and ultimately spatial domain through cosine transforms