ISTANBUL TECHNICAL UNIVERSITY
COMPUTER ENGINEERING DEPARTMENT

BLG 222E

Computer Organization
Project 1

PROJECT DATE : 24.05.2023

GROUP MEMBERS:

150220762 : Muhammed Yusuf Mermer (Group Representative)

150210071 : Emre Çamlıca

150200091 : Hakan Duran

SPRING 2023

Contents

1 INTRODUCTION

In this project our purpose was to design a hardwired control unit. To achive this we firstly implemented small components of this system. Yusuf did the fetch and decode parts, Hakan did the instructions without memory reference and Emre did the instructions with memory reference. Yusuf also wrote the test bench and tested the system with Hakan.

At first, Yusuf has designed the fetch cycle. Then Hakan and Emre designed the execute part. Hakan and Yusuf then tested the project and corrected the errors.

2 IMPLEMENTATIONS AND EXPLANATIONS

2.1 Fetch Cycle, Counter and Decoding

In our implementations, we made only counter module seperated from the combined system. It could have also been designed inside of overall combined system as a register, but this was our design choice. It takes clock as input, because at every positive edge we increase our timing signal by 1. However, to prevent unexpected result in the current postive edge we wait for 0.25 ns in our implementation.

Not only clock, but also reset signal taken as input for this module to return inital value for the timing signal. When it reset, it returns value 4 bit binary 1111 which is equal to -0001, this is been made because reset signal does not depend on clock; therofore, after the reset we wait for new clock signal to start new operations. New operations will be started with timing signal 0.

INtial ve ilk always blcoklarından bahset**********

For our combined module, we have after making all necesessary connections,

When timing signal 0 arrives to our combined system, it starts to fetch cycle. Our fetch cycle is totally takes 3 cycles. It has been made 3 cycles to prvent changes unintended changes on the PC and IR.

At first (0th) cycle of the fetch, we made

2.2 Instructions With Address Reference

2.3 Instructions Without Address Reference

3 OVERALL DESIGN PHOTO

4 SIMULATION RESULTS

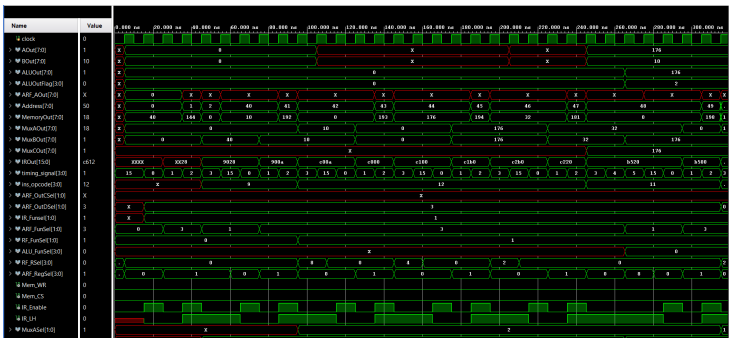

Figure 1: implementation of system

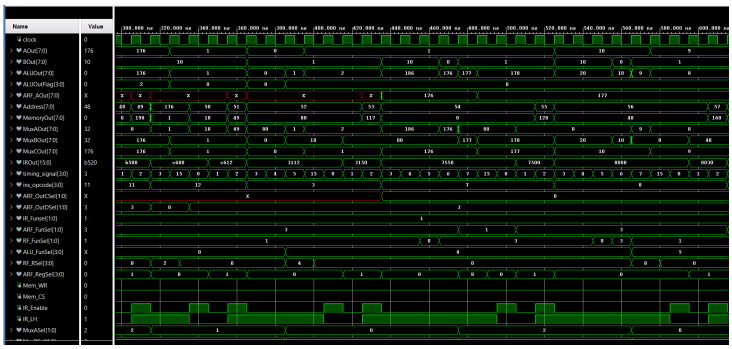

Figure 2: implementation of system

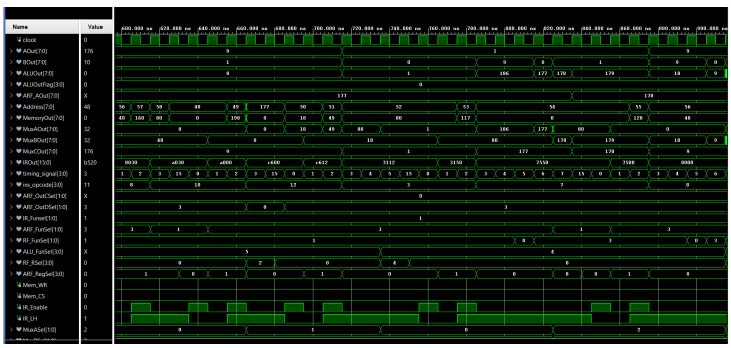

Figure 3: implementation of system

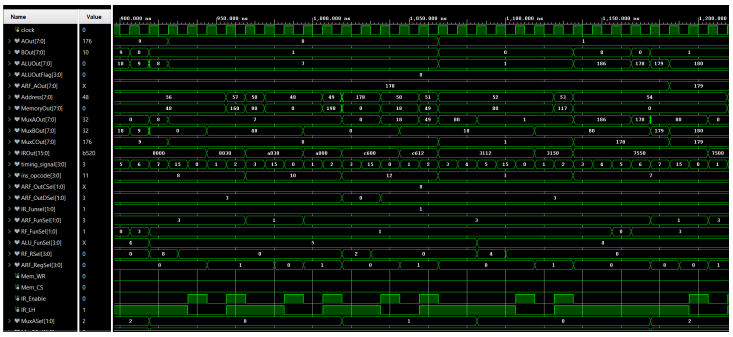

Figure 4: implementation of system

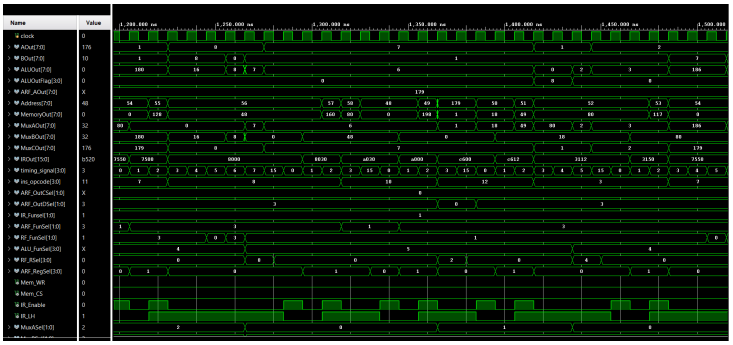

Figure 5: implementation of system

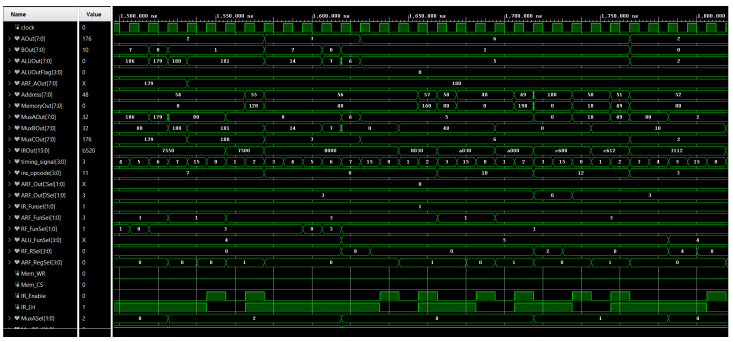

Figure 6: implementation of system

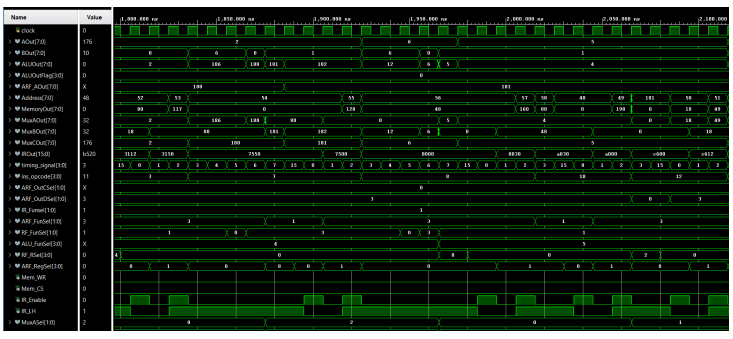

Figure 7: implementation of system

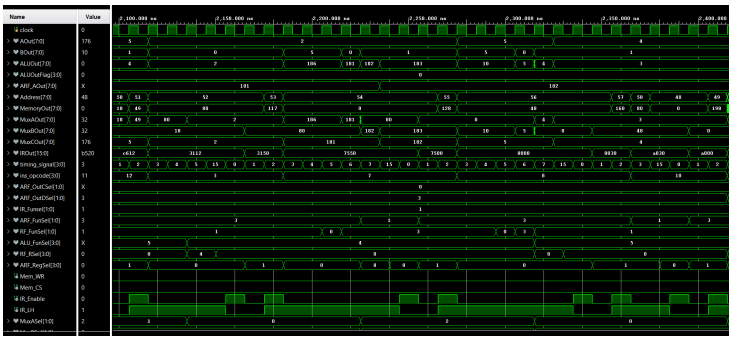

Figure 8: implementation of system

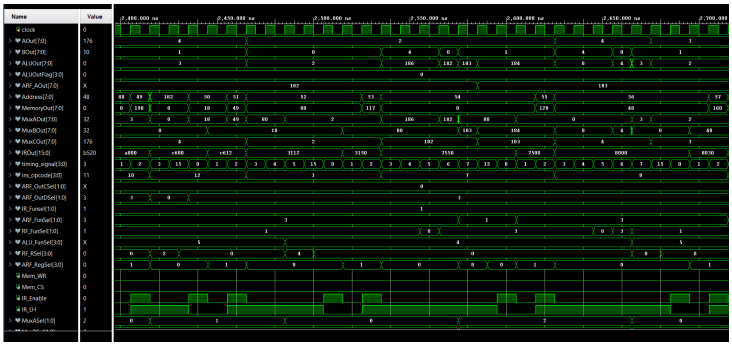

Figure 9: implementation of system

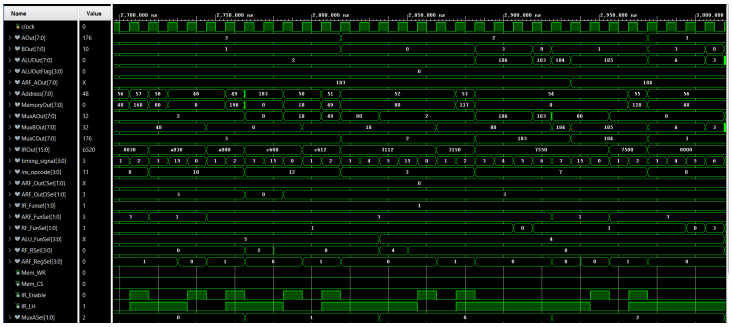

Figure 10: implementation of system

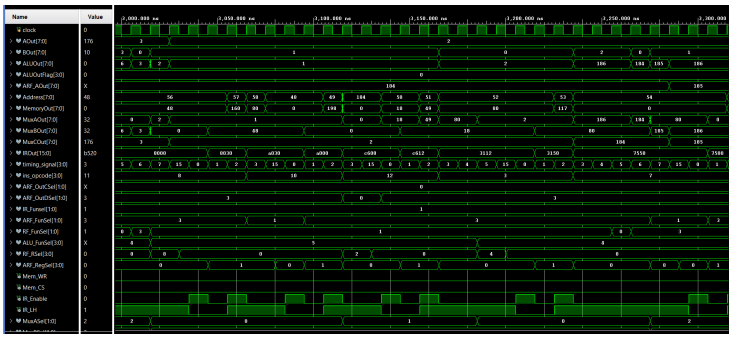

Figure 11: implementation of system

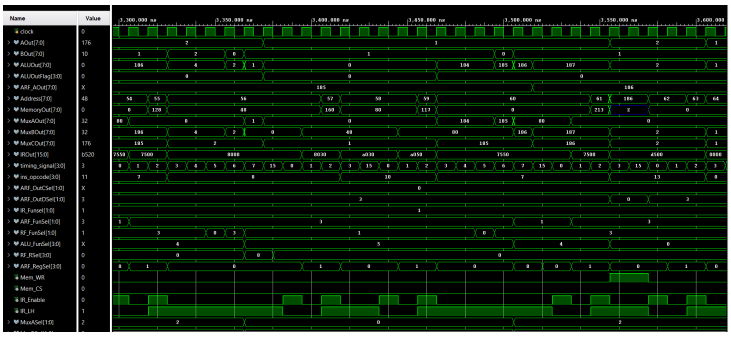

Figure 12: implementation of system

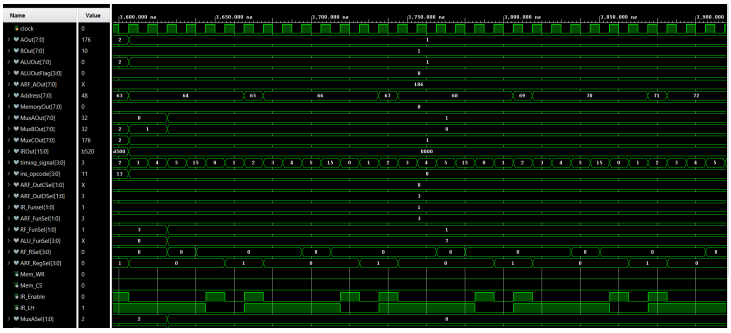

Figure 13: implementation of system

5 DISCUSSION

ilk önce nasıl fetch cycle yaptığından bahset.

6 CONCLUSION

In this project we designed a hardwired control unit with the help of the ones we created in the first project.