1. 单选题 （2.0分）

In a P-type semiconductor material, the majority carriers are _____.

- A.free electrons
- B.holes
- C.impurity irons
- D.valence elections

2. 单选题 （2.0分）

In a semiconductor diode, the region near the PN junction consisting of positive and negative ions is called the _____.

- A.neutral zone
- B.recombination region
- C.depletion region
- D.diffusion area

3. 单选题 （2.0分）

To form the positive material in the semiconductor, which element can be doped? _____.

- A.group IV elements
- B.group V elements
- C.group III elements
- D.group VI elements

4. 单选题 （2.0分）

For a Zener diode, in the Zener region the current _____ and the voltage across the diode _____.

- A.is almost constant; is almost constant
- B.can increase a lot; is almost constant
- C.is almost constant; can increase a lot
- D.can increase a lot; can increase a lot

5. 单选题 （2.0分）

For circuit shown in **Figure 1**, the diode is ideal; if the input DC voltage v_i>0, the output is _____.

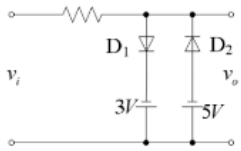

Figure 1

- A.-8V
- B.-2V
- C.-5V
- D.-3V

6. 单选题 （2.0分）

For an PNP transistor working in active region, the DC voltages at three pins are -2V, -2.7V and-6V. The pins are _____ terminal.

- A.Base, Collector, Emitter
- B.Base, Emitter, Collector
- C.Collector, Base, Emitter
- D.Emitter, Base, Collector

7. 单选题 （2.0分）

To be employed as linear (undistorted) amplifiers for NPN transistor， the B-E junction of BJTs should be _____ biased and the B-C junction of BJTs should be _____ biased.

- A.forward, forward
- B.forward, reverse
- C.reverse, reverse
- D.reverse, forward

8. 单选题 （2.0分）

Which of the following is not true for the BJT circuit in **Figure 2** _____? (Assuming the knee voltage of B-E junction is 0.7V)

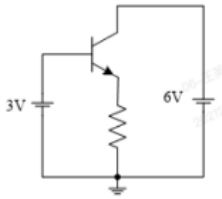

Figure 2

- A.The base voltage is 3V.
- B.The voltage between collector and emitter is 3.7V.
- C.The emitter voltage is 0.7V.
- D.The collector voltage is 6V.

9. 单选题 （2.0分）

In a common emitter amplifier, the output voltage is always_____ with the input voltage in full frequency band.

- A.45^{o} out of phase
- B.90^{o} out of phase
- C.180^{o} out of phase
- D.None of above

10. 单选题 （2.0分）

For an emitter follower, the input impedance is relatively _____ and the output impedance quite _____.

- A.high, small
- B.small, high
- C.small, small
- D.high, high

11. 单选题 (2.0分)

For the transistor amplifier circuit, if the quiescent point is low, then_____ happens, if the quiescent point is high, then _____happens.

- A.Saturation distortion, Cut-off distortion
- B.Cut-off distortion, Saturation distortion
- C.Saturation distortion, Saturation distortion
- D.Cut-off distortion, Cut-off distortion

12. 单选题 (2.0分)

The region of the characteristic curve family for the FETs that is normally used for linear amplification is _____.

- A.the linear-resistance region
- B.the Ohmic region
- C.the saturation region
- D.All of the above

13. 单选题 (2.0分)

The minimum current in a JFET occurs when V_{GS} is equal to _____.

- A.pinch-off voltage
- B.zero Voltage
- C.a voltage greater than the pinch-off voltage
- D.a small positive voltage

14. 单选题 (2.0分)

A _____ is a voltage-controlled device and a _____ is a current-controlled device.

- A.BJT, FET
- B.BFT, FFT
- C.FET, BJT
- D.BCE, FJT

15. 单选题 （2.0分）

For the voltage divider circuit, the NPN BJT common emitter configuration, the voltage gain is_.

- A.Au=-(R_C||r_o)/r_e
- B.Au=-(R_1||r_o)/r_e
- C.Au=-(R_2||r_o)/r_e
- D.None of above

16. 单选题 （2.0分）

Calculate the JFET amplifier with load in **Figure 3**. Assume that g_m=2mS, R_D=4kΩ, R_L=4kΩ_____.

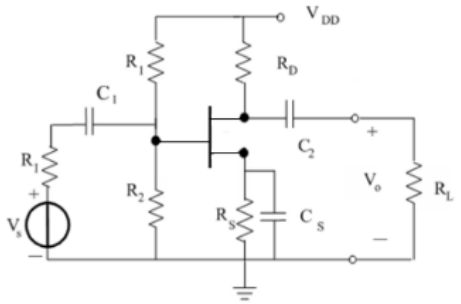

Figure 3

- A.Au= 4
- B.Au= 1
- C.Au= -4
- D.Au= -1

17. 单选题 （2.0分）

For the common emitter amplifier, ___ capacitors do not affect the low frequency response.

- A.bypass
- B.input coupling
- C.output coupling
- D.interelectrode

18. 单选题 (2.0分)

For BJT amplifiers, the high frequency and low-frequency gain is _____.

- A.decreased
- B.increased
- C.constant
- D.None of above

19. 单选题 (2.0分)

When a BJT transistor is used in a switching circuit, it operates in the _____.

- A.saturation and active regions
- B.active and cutoff regions
- C.saturation and cutoff regions
- D.active region only

20. 单选题 (2.0分)

If a resistor is added in the emitter for the CE amplifier, which is not bypassed by a capacitor, then the voltage gain of the small signal CE amplifier will _____.

- A.decrease
- B.increase
- C.increase in some cases and decrease in other cases
- D.stay the same

21. 单选题 (2.0分)

When comparing the common emitter and the common collector amplifiers, the input impedance of the common _____ is much larger and the output impedance of the common _____ is much smaller.

- A.emitter; emitter
- B.emitter; collector
- C.collector; emitter
- D.collector; collector

22. 单选题 （2.0分）

The common-base amplifier is characterized as having a relatively _____ input impedance and relatively _____ output impedance.

- A.high; low
- B.low; low
- C.low; high
- D.high; high

23. 单选题 （2.0分）

For an unload BJT amplifier, voltage gain is -100, output impedance is 20, terminal load is 80, the loaded voltage gain is _____.

- A.-20
- B.+20
- C.+80
- D.-80

24. 单选题 （2.0分）

Crossover distortion in class B power amplifiers can be prevented by _____.

- A.biasing the transistors slightly above cutoff.
- B.biasing the transistors deeply into cutoff.
- C.using complementary-symmetry transistors.
- D.increasing the load resistance.

25. 单选题 （2.0分）

Ideally, the _____amplifier has larger gain for the differential mode signal, and has no gain for the common mode signal.

- A.transistor
- B.power
- C.common
- D.differential

26. 简答题 （10.0分）

For the network shown in **Figure 4**, V_T=26mV (at room temperature):

1) Describe how to get the DC equivalent circuit. **(1 marks)**

2) Assume $V_{BE(on)}$=0.7V, determine the Q point： V_B, I_E , r_e . **(3 marks)**

3) Describe how to get the AC equivalent circuit. **(2 marks)**

4) Find the A_u , Z_i and Z_o with r_0= ∞ Ohm. **(3 marks)**

5) If the load R_L=3.9kΩ is added to the output, calculate the voltage gain A_u. **(1 marks)**

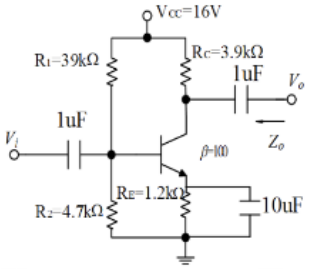

Figure 4

27. 简答题 （12.0分）

A differential amplifier is shown in **Figure 5**. For the transistors T_1 and T_2, β=100, $r_{ce}=\infty$, $U_{BE}(on)=0.6V$, $V_T=26mV$ (at room temperature).

1) Calculate static collector current I_{CQ1} and I_{CQ2}. **(2 marks)**
2) Calculate static voltage V_{C1} and V_{C2}. **(1 marks)**
3) Calculate the r_e parameter of the ac equivalent model. **(2 marks)**
4) For a double output, calculate the differential mode voltage gain. **(2 marks)**
5) For a double output, calculate the differential mode input resistance. **(2 marks)**
6) For a double output, calculate the differential mode output resistance. **(1 marks)**
7) For a double output, calculate the common mode voltage gain. **(1 marks)**
8) For a double output, calculate the CMRR. **(1 marks)**

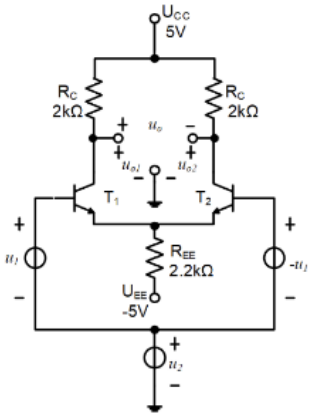

Figure 5

28. 简答题 （5.0分）

For the negative feedback circuit in **Figure 6,** answer the questions.
1) Determine the type of the negative feedback. **(1 marks)**
2) If the AC negative feedback is strong enough, calculate the voltage gain by approximate analysis method. **(2 marks)**
3) If the AC negative feedback is strong enough, calculate the input impedance and output impedance. **(2 marks)**

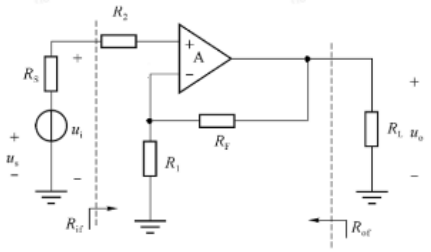

Figure 6

29. 简答题 （5.0分）

For the negative feedback circuit in **Figure 7**, answer the questions.
1) Determine the type of the negative feedback. **(1 marks)**
2) If the AC negative feedback is strong enough, calculate the voltage gain by approximate analysis method. **(2 marks)**
3) If the AC negative feedback is strong enough, calculate the input impedance and output impedance. **(2 marks)**

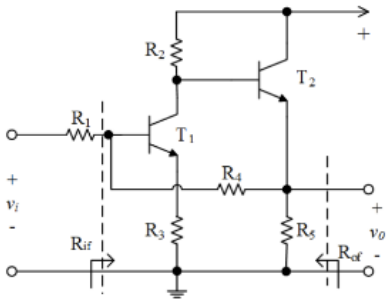

Figure 7

30. 简答题 （8.0分）

For complementary symmetric power amplifier circuit shown in **Figure 8,** the base bias circuit is omitted. VT_2 and VT_3 are output transistors. Assume that the saturation voltages of VT_2 and VT_3 are negligible. The voltage on R4 and R5 are negligible.

1) Determine the static voltage of point A. **(1 marks)**
2) What are the role of the connection of D_1 and D_2? **(1 marks)**
3) Find the maximum AC output power.**(2 marks)**
4) Find the maximum input power from the DC supply. **(2 marks)**
5) Find the maximum power efficiency. **(1 marks)**
6) Find the power dissipation by both T2 and T3 when the output power is maximum.**(1 marks)**

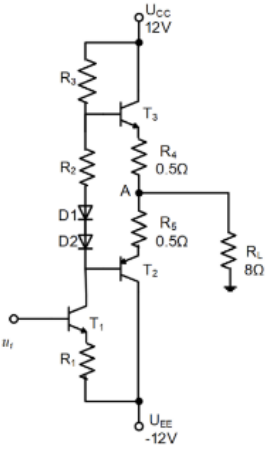

Figure 8

31. 简答题 （10.0分）

In the circuit of **Figure 9**, the op-amp are ideal. Zener Diode with V_Z=±10V, R_1=100KΩ, R_2=2KΩ, R=10KΩ, C=1μF, v_{i1}=-5V, v_{i2}=5.1V, V_R= -7V, Power supply Vcc=±15V, at t=0, v_c=0V. If connected to power supply at t=0， determine the function of each stage, and calculate the voltage output of each stage at t=5.1s. (note: calculate v_{o1}, v_{o2}, v_{o3}, v_{o4}, v_{o5}, v_{o6}, v_o)