Chapter 2:
Bipolar Junction Transistors and Basic BJT Amplifiers

Contents

2.1.1 Transistor Construction

There are two types of transistors:

- *pnp*
- *npn*

The terminals are labeled:

- E – Emitter
- B – Base
- C – Collector

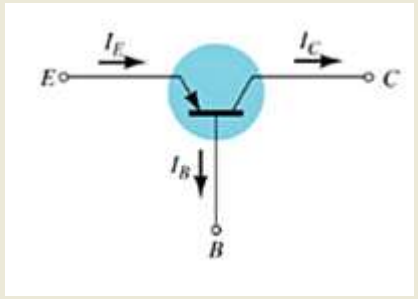
Features of each doped region:

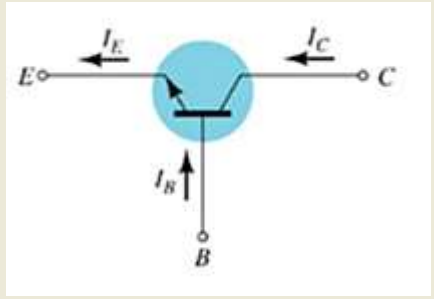
- E – Highly doped
- B – Very narrow, lowest doped
- C – lower doped, large surface

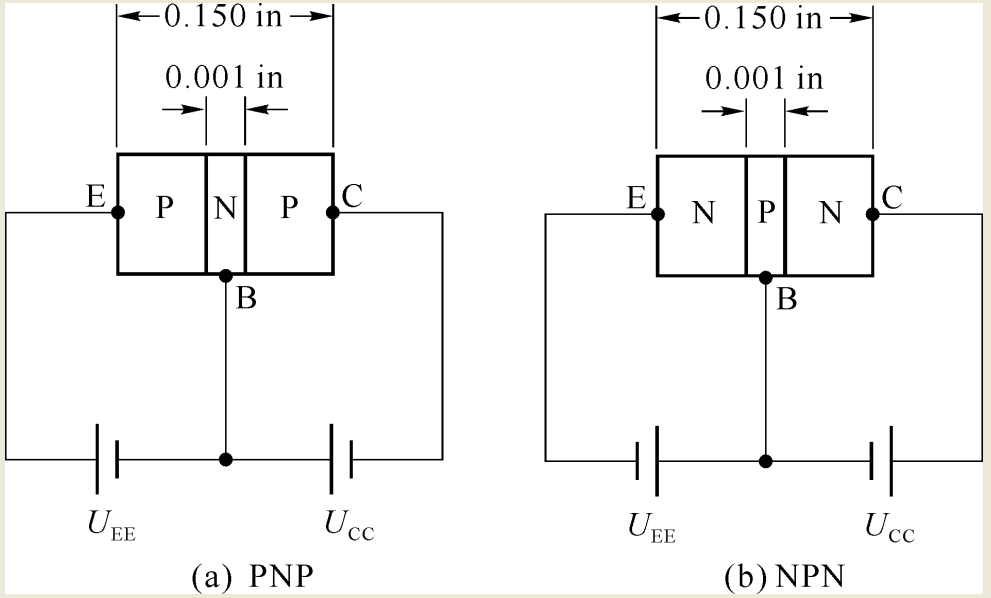
There are two p-n junctions:

- Base-Emitter junction
- Base-Collector junction

pnp *npn*







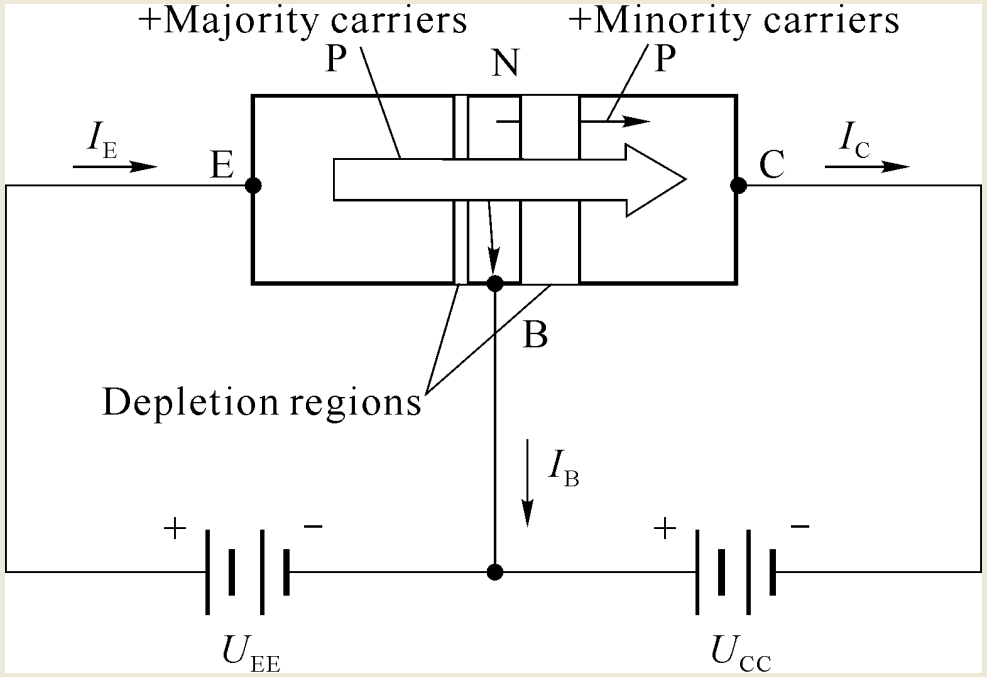
2.1.2 BJT Characteristics

Magic!

With the external sources, U_{EE} and U_{CC}, connected as shown below:

- **The emitter-base junction is forward biased**
- **The base-collector junction is reverse biased**

PNP



Emitter current is the sum of the Collector and Base currents:

$$I_E = I_C + I_B$$

The Collector current is comprised of two currents:

$$I_C = I_{Cmajority} + I_{COminority}$$

$$I_{COminority} = I_{CBO}$$

2.1.3 Modes of Operation

There are four operation modes depending on the bias condition of each pn junction:

	Emitter-Base junction	Base-Collector junction
Active region *(Linear Amplification)*	Forward bias	Reverse bias
Saturation region	Forward bias	Forward bias
Cutoff region	Reverse bias	Reverse bias
Reverse operation	Reverse bias	Forward bias

The active operation region is normally employed for linear (undistorted) amplifiers.

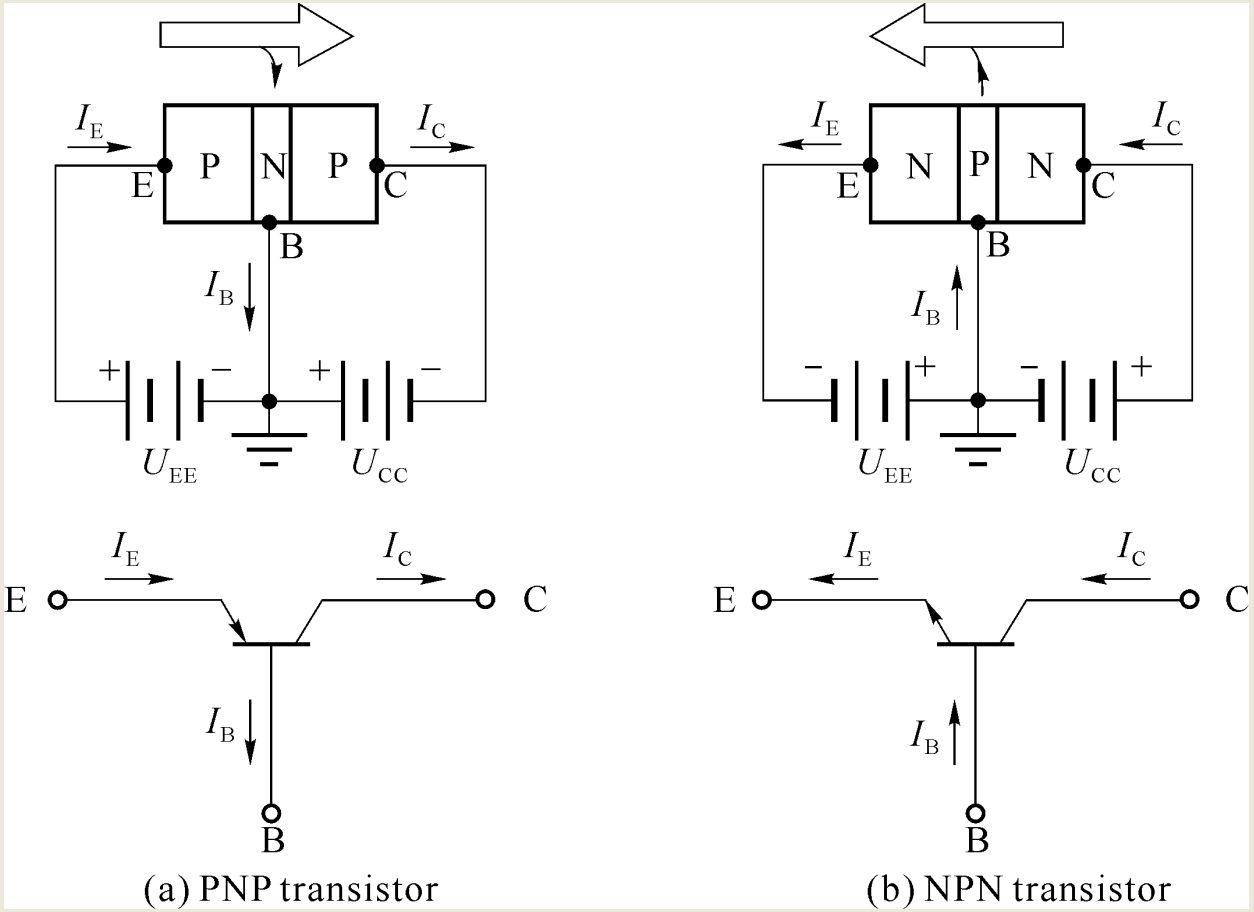
Three Basic Configuration of BJTs

Three basic configurations of a BJT according to the common terminal:

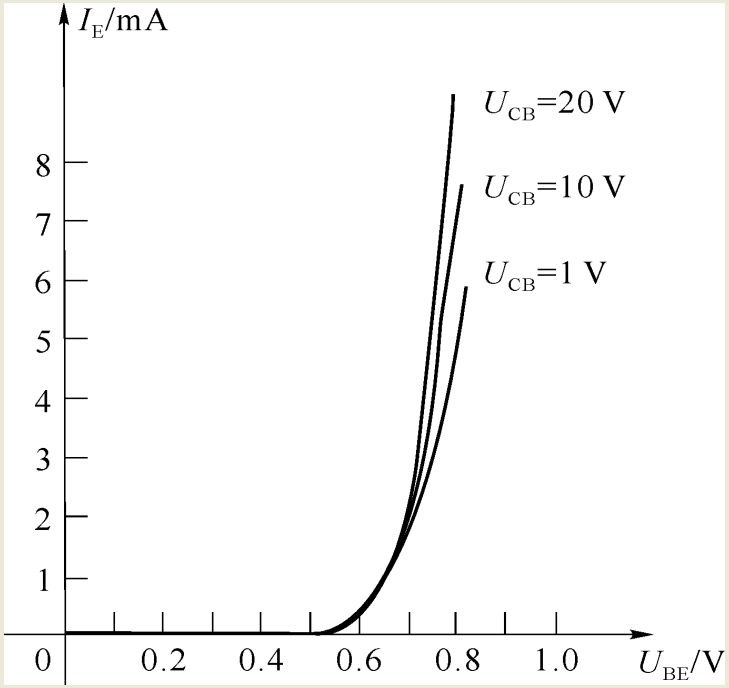
	Input terminal	Common terminal	Output terminal
Common-Base (CB)	Emitter	*Base*	Collector
Common-Emitter (CE)	Base	*Emitter*	Collector
Common-Collector (CC)	Base	*Collector*	Emitter

Common-Base Configuration

CB: The Base is common to both input (Emitter–Base) and output (Collector–Base) of the transistor.



Common-Base Configuration

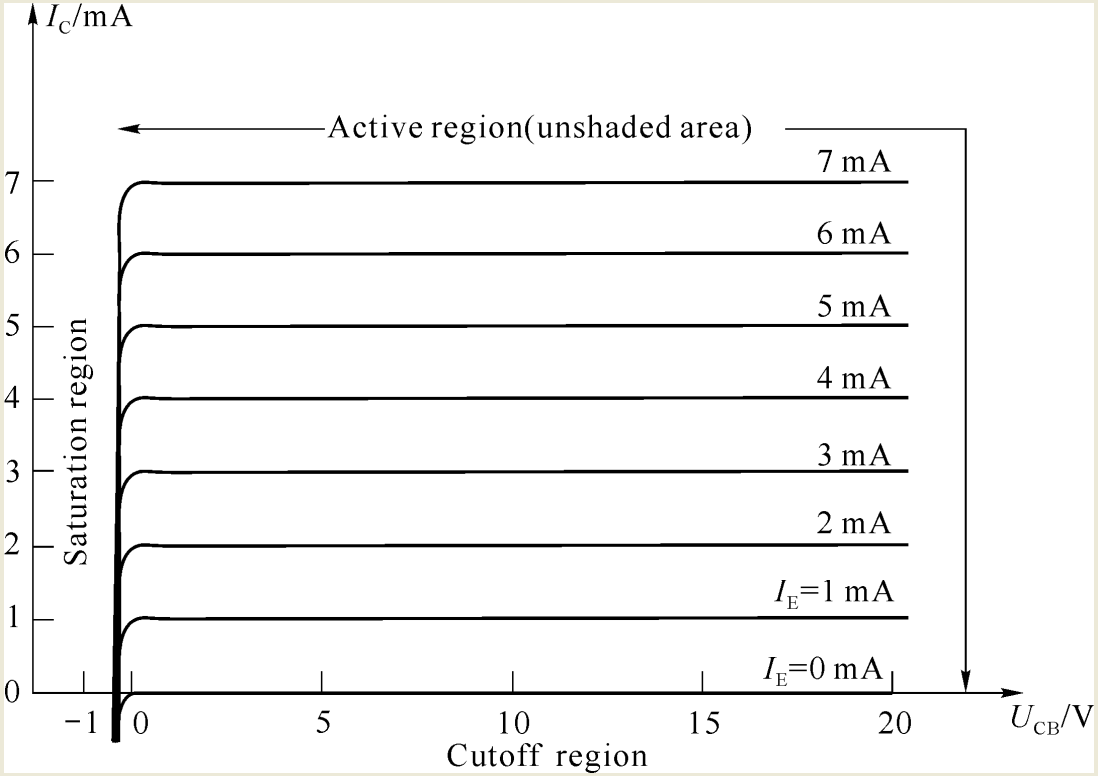


Input Characteristics:

This curve shows the relationship between input current (I_E) and input voltage (U_{BE}) for various levels of output voltage (U_{CB}).

Output Characteristics:

This graph demonstrates the output current (I_C) to an output voltage (U_{CB}) for various levels of input current (I_E).



Operating Regions

- **Cutoff region—The amplifier is basically off. There is voltage, but little current.**
- **Saturation region—The amplifier is full on. There is current, but little voltage.**
- **Active region—Operating region of the amplifier.**

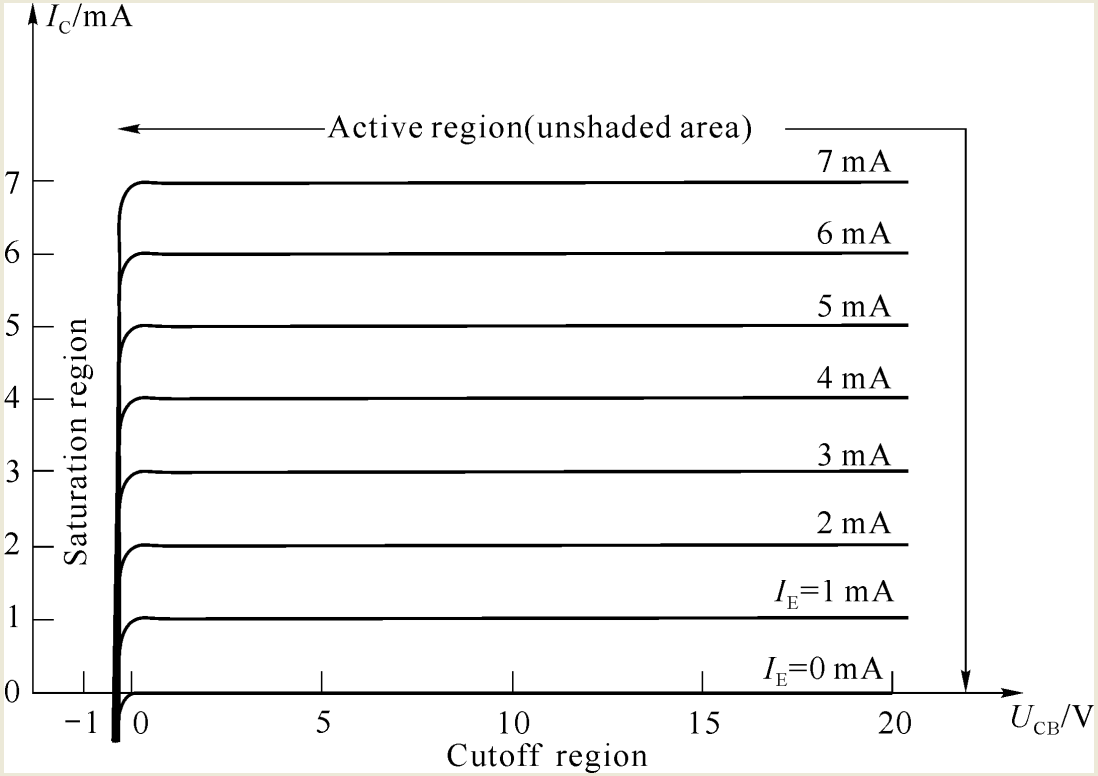
In active region:

Emitter and collector currents:

$$I_C \cong I_E$$

Base-emitter voltage:

$$U_{BE} = 0.7V$$



I_{CBO} = minority collector current, which is usually so small that it can be ignored

Alpha (α)

Alpha (α) in the DC mode relates the currents I_C and I_E :

$$\alpha_{dc} = \frac{I_C}{I_E}$$

Ideally: $\alpha = 1$

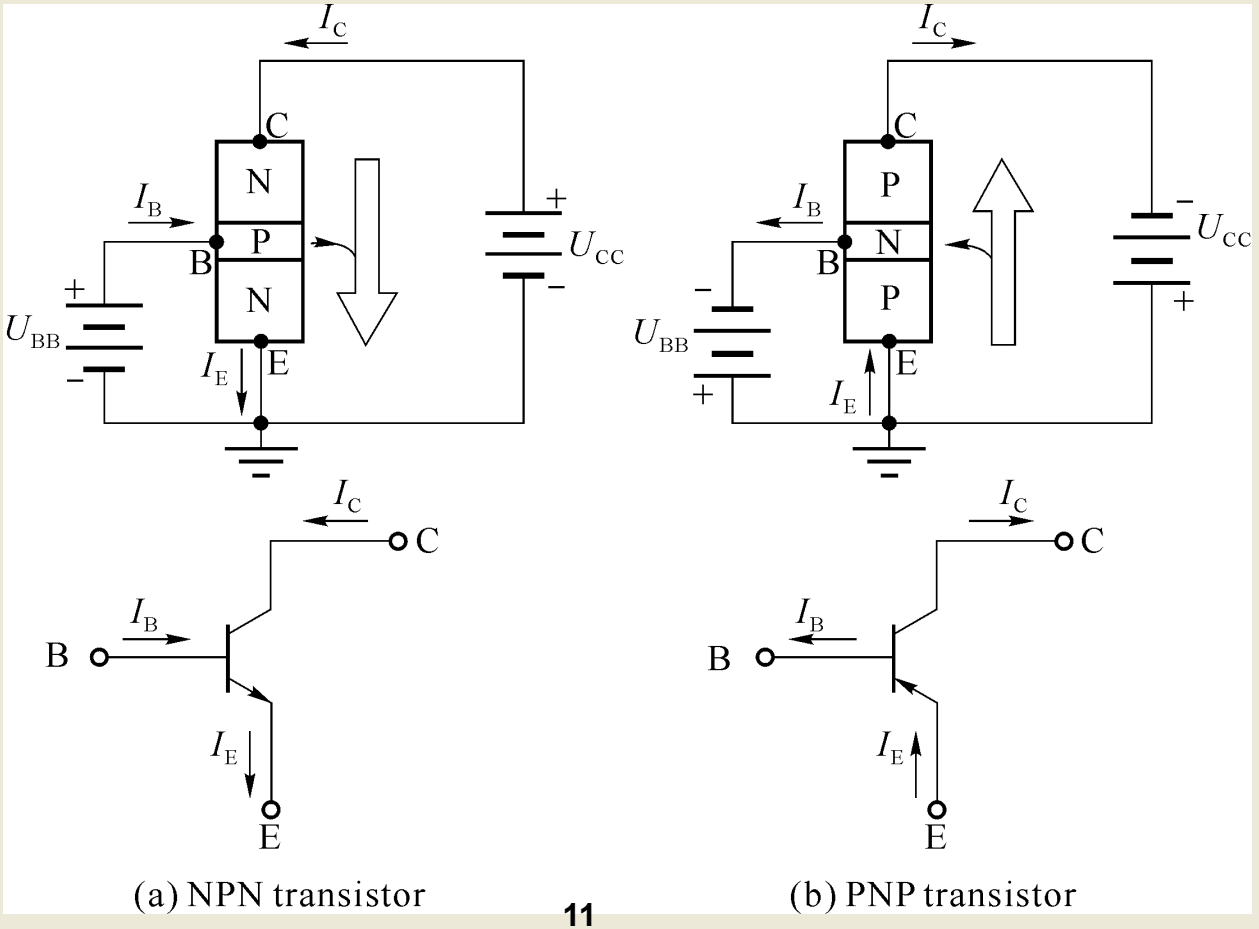
In reality: α is between 0.9 and 0.998

Alpha (α) in the AC mode:

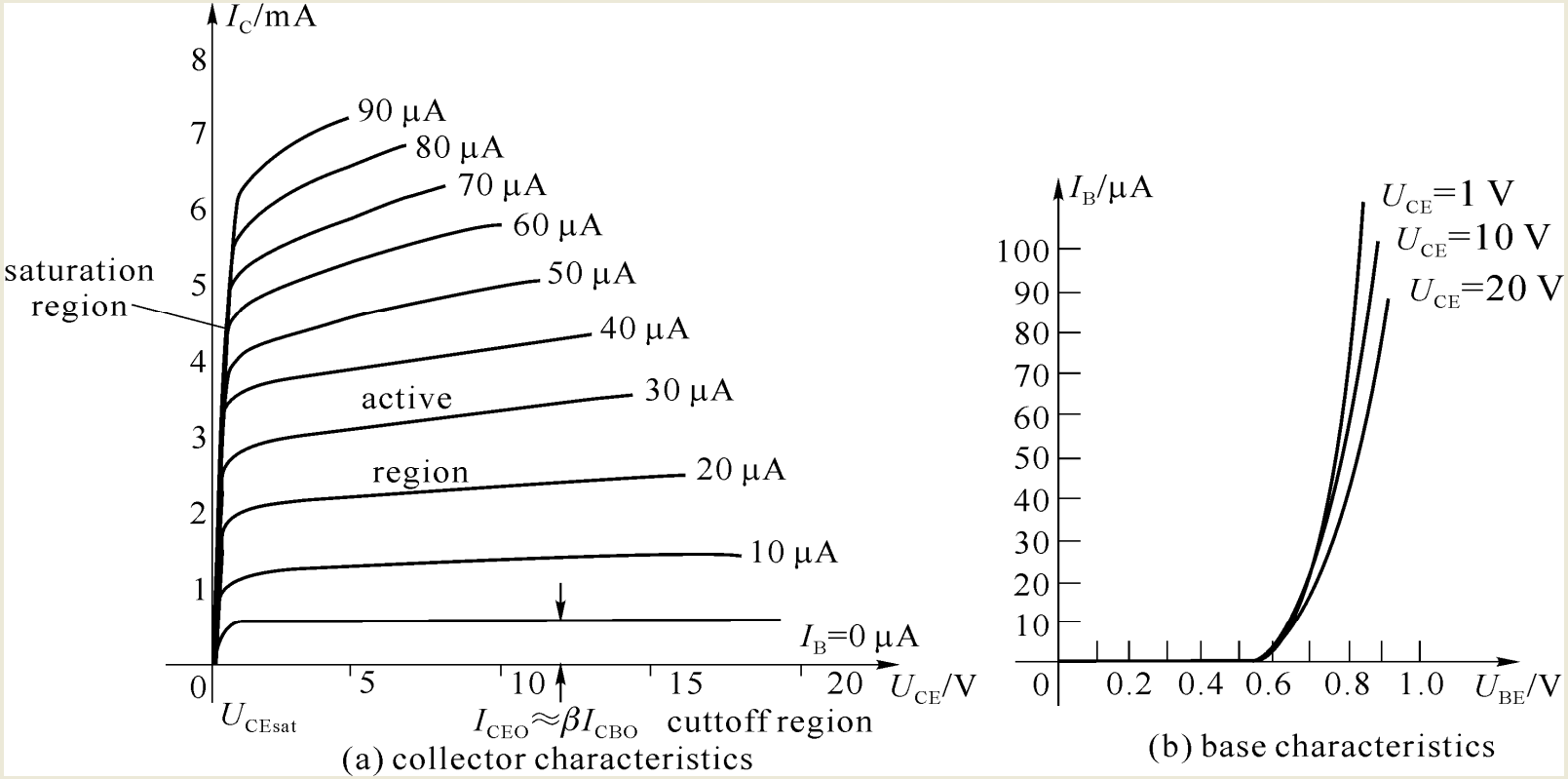
$$\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E}$$

Common–Emitter Configuration

CE: The Emitter is common to both input (Base-Emitter) and output (Collector-Emitter).
The input is on the Base and the output is on the Collector.



Common-Emitter Characteristics



Output Characteristics

This graph demonstrates the output current (I_C) to an output voltage (U_{CE}) for various levels of input current (I_B).

Input Characteristics

This curve shows the relationship of input current (I_B) to input voltage (U_{BE}) for various levels of output voltage (U_{CE}).

Beta (β)

β represents the Amplification factor of a transistor. (β is sometimes referred to as h_{fe}, a term used in transistor modeling calculations)

In DC mode:

$$\beta_{dc} = \frac{I_C}{I_B}$$

In AC mode:

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}\Big|_{V_{CE}=\text{constant}}$$

Beta (β)

Determining β from a Graph

$$\beta_{ac} = \frac{(3.2\,\text{mA} - 2.2\,\text{mA})}{(30\,\mu\text{A} - 20\,\mu\text{A})}$$

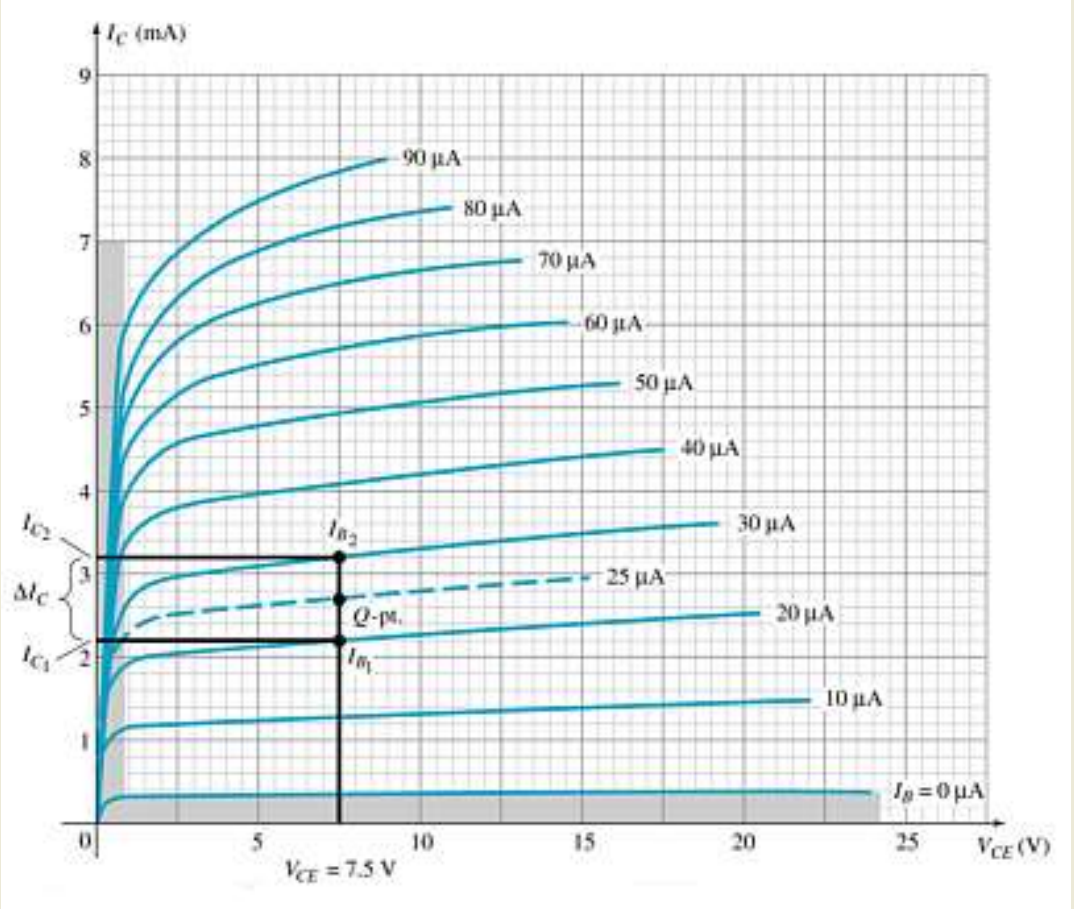
$$= \frac{1\,\text{mA}}{10\,\mu\text{A}}\bigg|_{V_{CE}=7.5}$$

$$= 100$$

$$\beta_{dc} = \frac{2.7\ \text{mA}}{25\ \mu\text{A}}\bigg|_{V_{CE}=7.5}$$

$$= 108$$

Note: $\beta_{AC} \approx \beta_{DC}$



Beta (β)

Relationship between amplification factors β and α

$$\alpha = \frac{\beta}{\beta + 1} \qquad \beta = \frac{\alpha}{1 - \alpha}$$

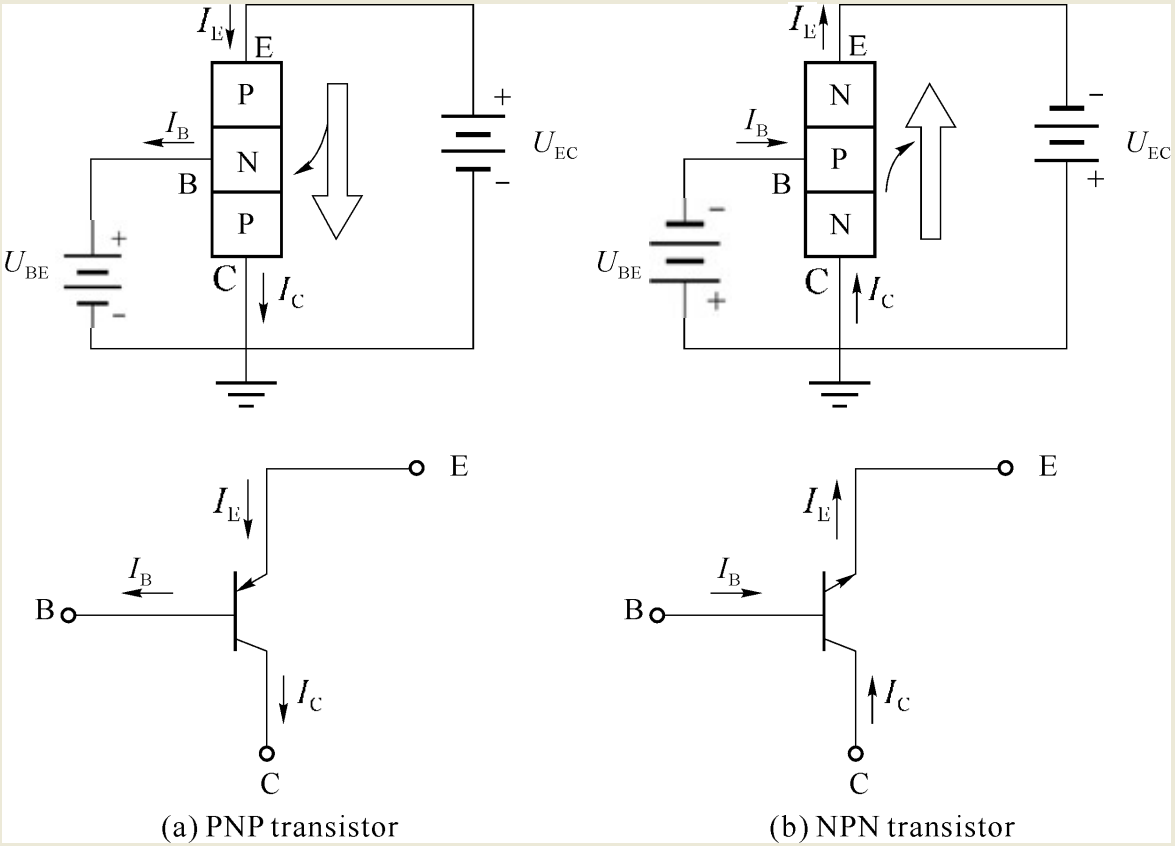
Relationship Between Currents

$$I_C = \beta I_B \qquad I_E = (\beta + 1) I_B$$

Common-Collector Configuration

CC: The collector is common to both input (Base-Collector) and output (Emitter-Collector).

The input is on the base and the output is on the emitter.



The characteristics are similar to those of the common-emitter (CE) configuration, except the vertical axis is I_E.

Limitations of BJT Operation

U_{CE} is at maximum and I_C is at minimum ($I_{Cmin} = I_{CEO}$) in the cutoff region.

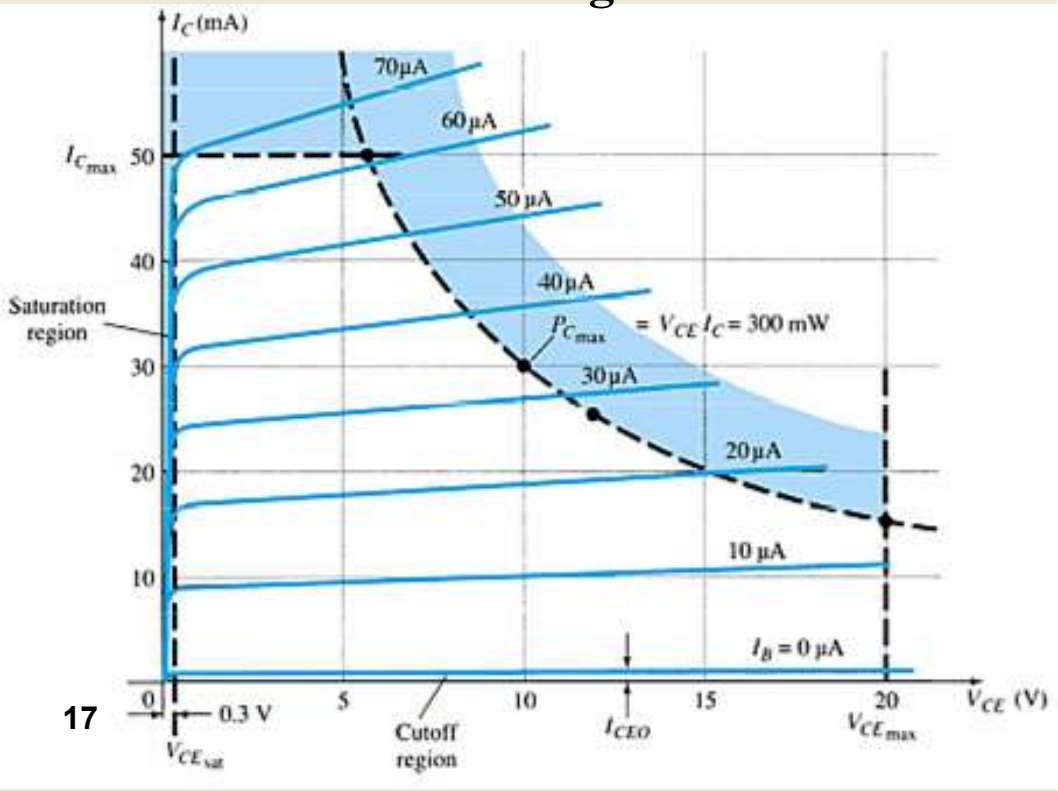
I_C is at maximum and U_{CE} is at minimum ($U_{CE\ min} = U_{CEsat} = U_{CEO}$) in the saturation region.

The transistor operates in the active region between saturation and cutoff.

Common-Emitter:

$$P_{Cmax} = U_{CE} I_C$$

CE Configuration



2.2 DC Biasing BJTs

Biasing **refers to the DC voltages applied to a transistor in order to turn it on so that it can amplify the AC signal.**

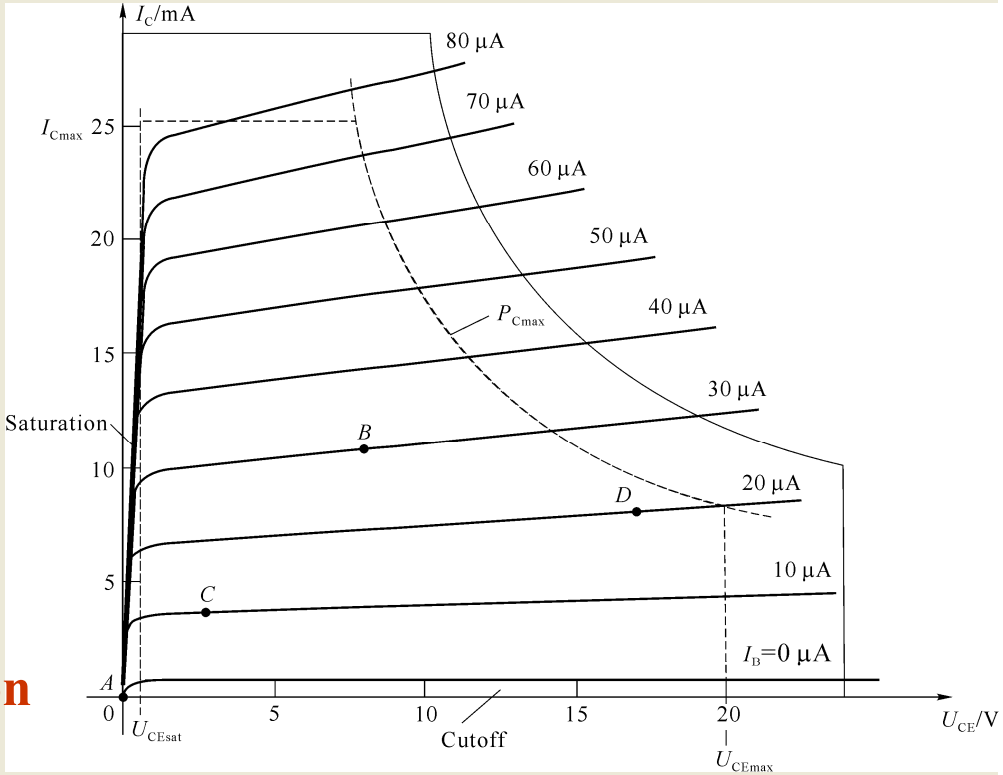
- ***To provide energy for amplification.***
- ***To provide a proper response to an input AC signal by determining the operating point.***

Nonlinear Devices

- ***DC and AC responses are different. So, DC analysis can be totally separated from the AC response.***
- ***The choice of parameters for DC levels will affect the AC response, and vice versa.***

Operating Point

The DC input establishes an operating or *quiescent operating point*, which is called the *Q-point*.



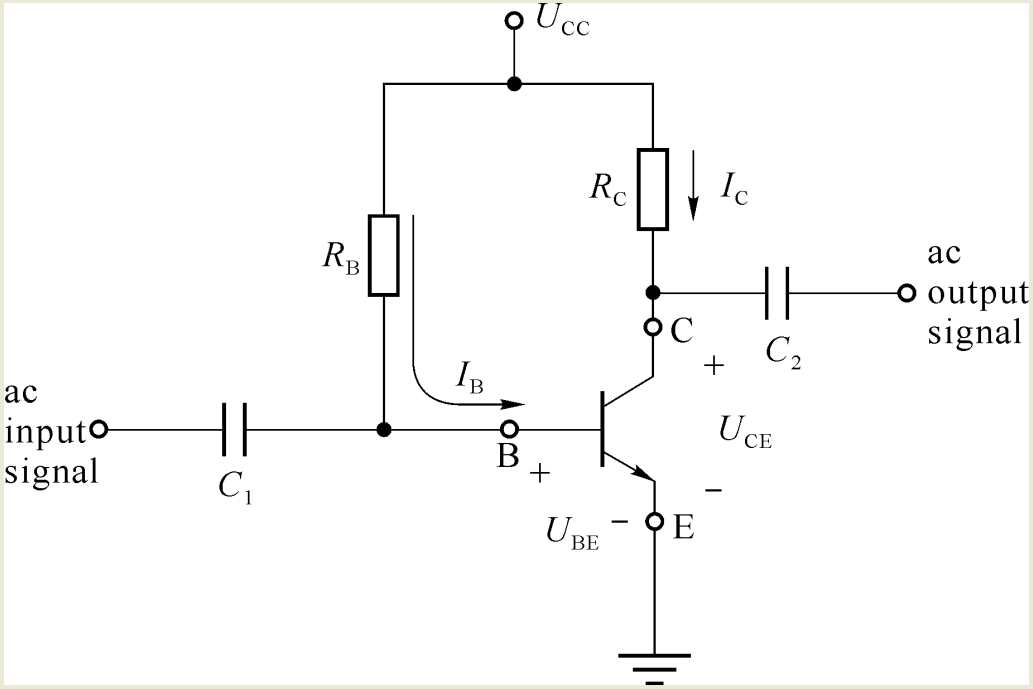
Biasing and Three States of Operation

- **Active/Linear Region**
  - Base–Emitter junction is *forward* biased
  - Base–Collector junction is *reverse* biased
- **Cutoff Region**
  - Both two junctions are *reverse* biased
- **Saturation Region**
  - Both two junctions are *forward* biased

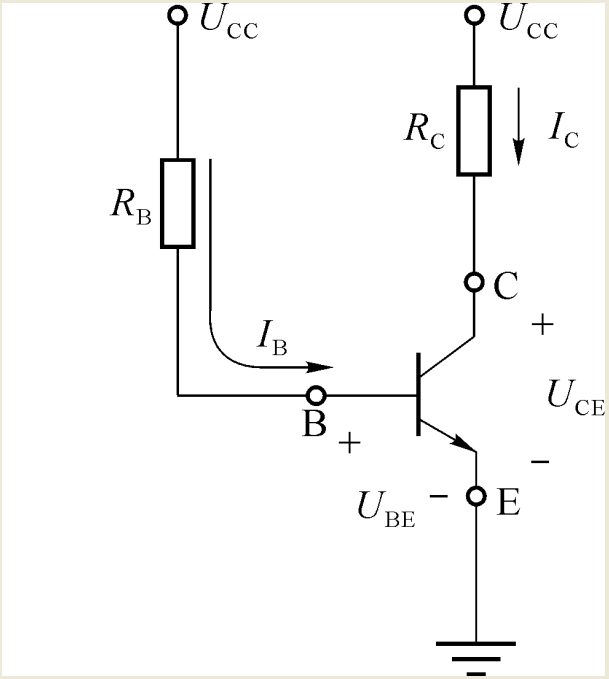
DC Biasing Circuits:

- Fixed-bias circuit
- Emitter-stabilized bias circuit
- Voltage divider bias circuit
- DC bias with voltage feedback

DC Analysis - Fixed Bias



Fixed-bias circuit



DC equivalent

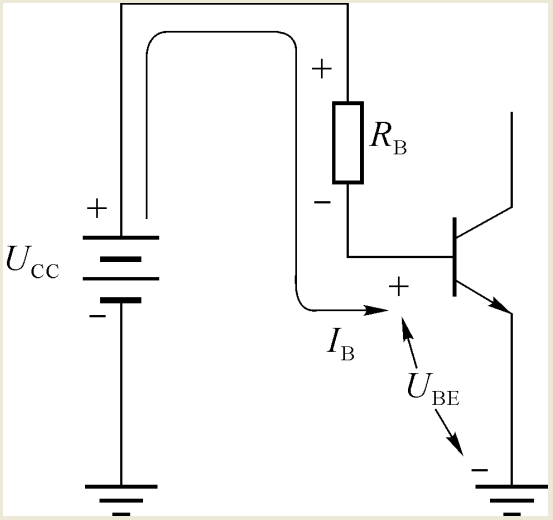
Sketching the DC equivalent is the first step for DC analysis:

1. **Replacing the capacitor with an open-circuit equivalent.**
2. **Replacing the inductor with a short-circuit equivalent.**
3. **DC supply can be separated for analysis purpose only.**

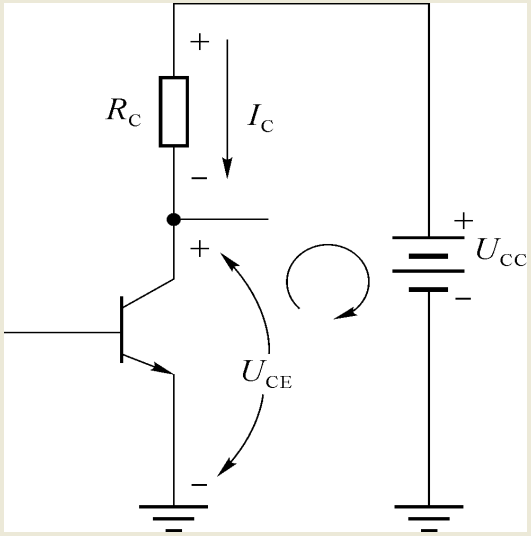
DC Analysis - Fixed Bias

Mathematical Analysis:

Base-Emitter loop



Collector-Emitter loop



From Kirchhoff's voltage law:

$$+U_{CC} - I_B R_B - U_{BE} = 0$$

Solution of the Base current:

$$I_B = \frac{U_{CC} - U_{BE}}{R_B}$$

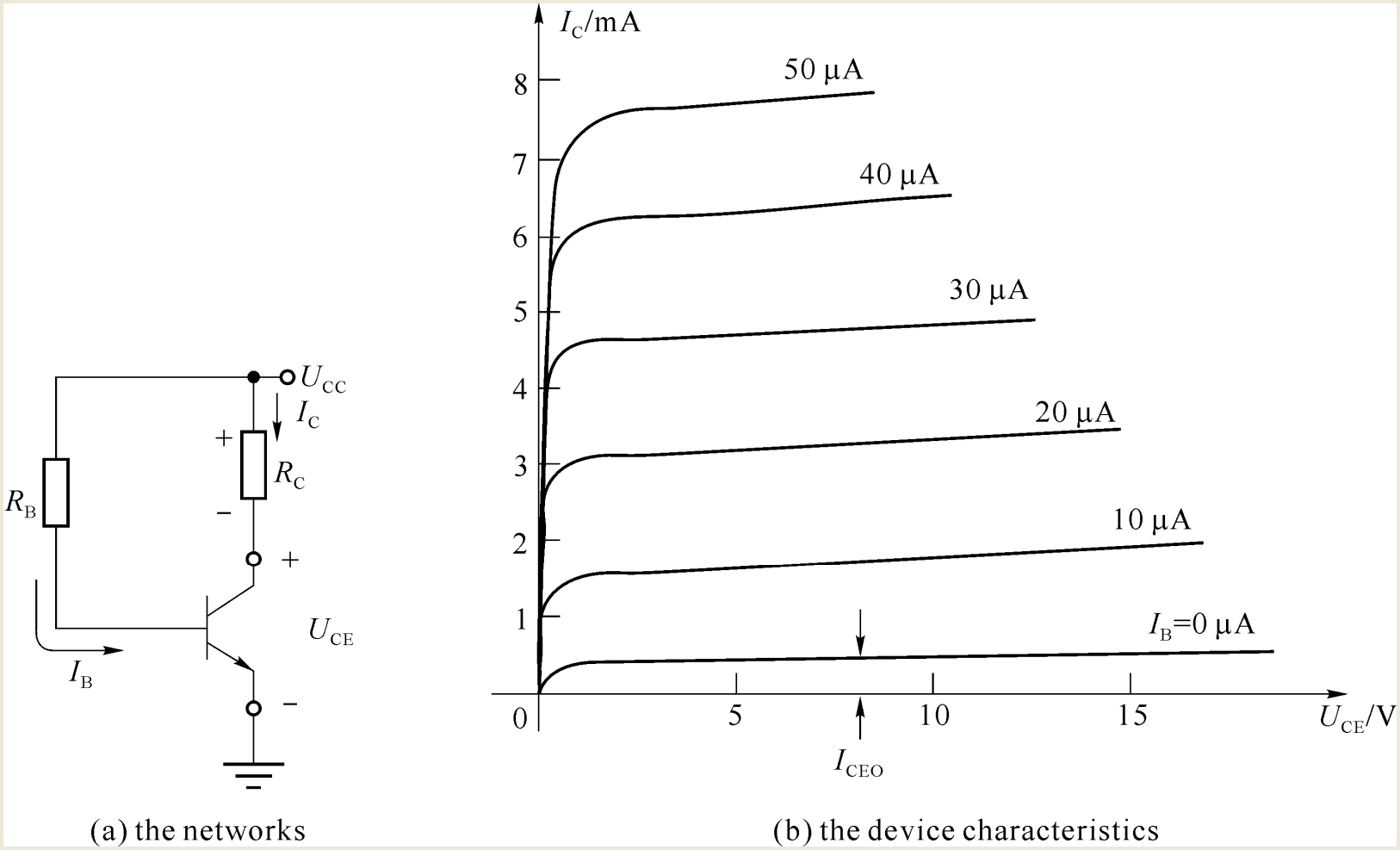
The Collector current is given by:

$$I_C = \beta I_B$$

From Kirchhoff's voltage law:

$$U_{CE} = U_{CC} - I_C R_C$$

Graphical Analysis



(a) the networks

(b) the device characteristics

Graphical Analysis: Load line

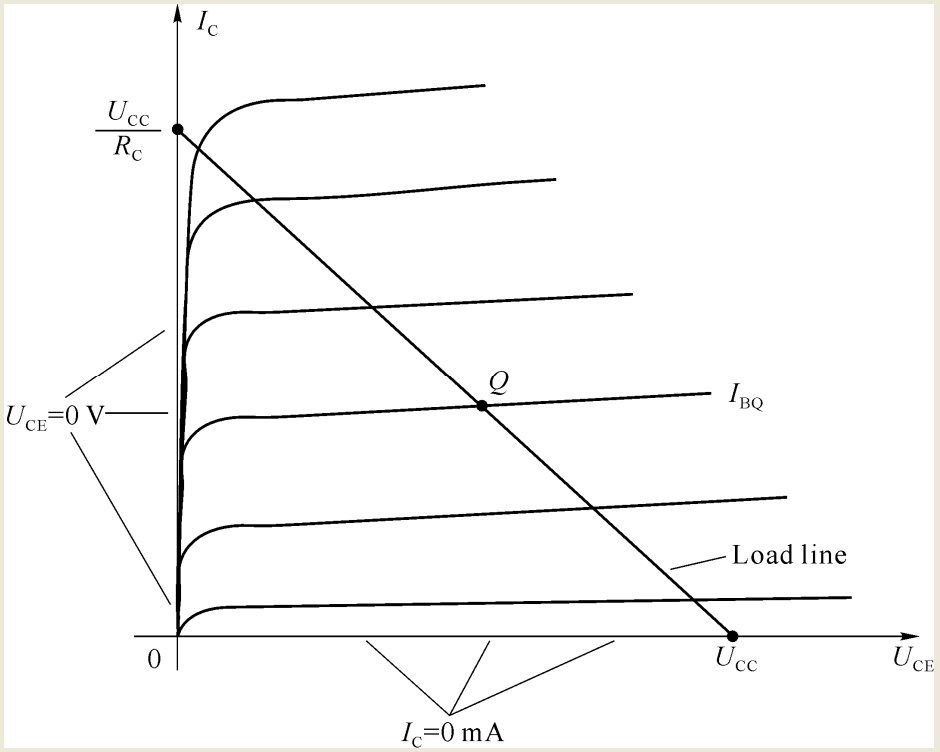
Load Line Analysis

Load equation by KVL:

$$U_{CE} = U_{CC} - I_C R_C$$

The end points of the load line are:

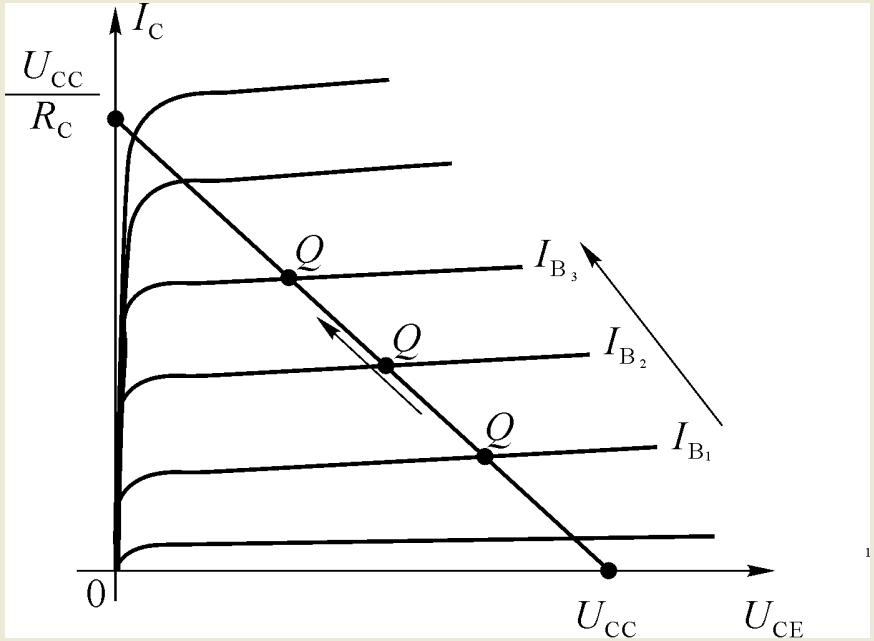
- I_{Csat}
  - $I_C = U_{CC} / R_C$
  - $U_{CE} = 0$ V
- $V_{CEcutoff}$
  - $U_{CE} = U_{CC}$
  - $I_C = 0$ mA

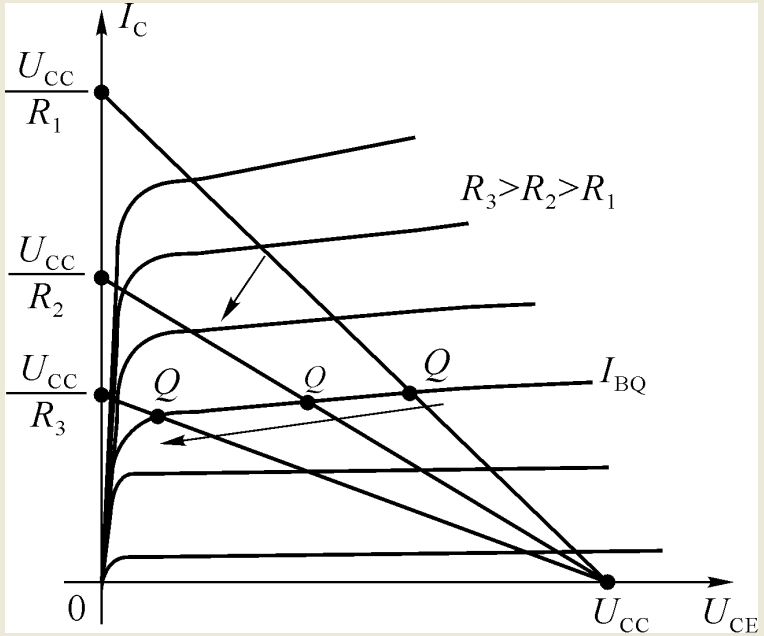


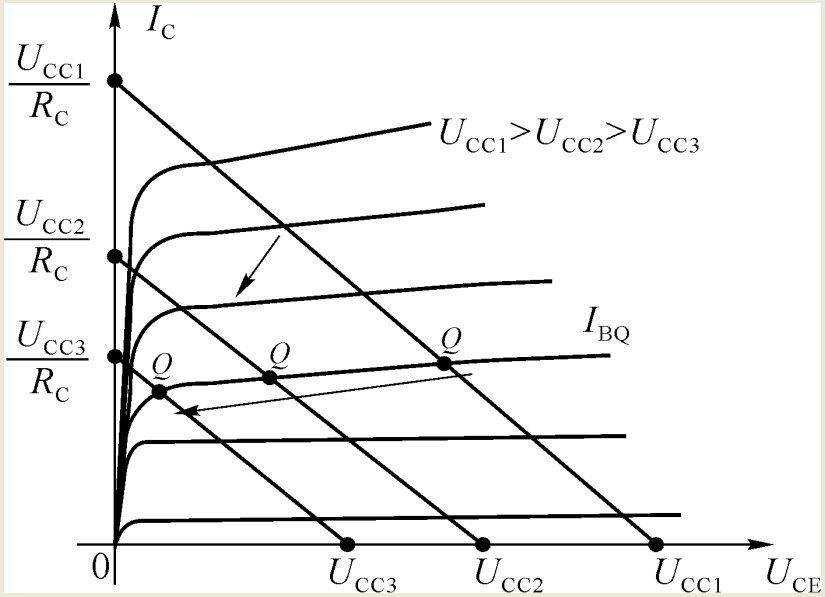
The *Q-point* is the operating point:

- where the value of R_B sets the value of I_B
- where I_B and the load line intersect
- that sets the values of U_{CE} and I_C

Circuit Values Affecting the Q-Point



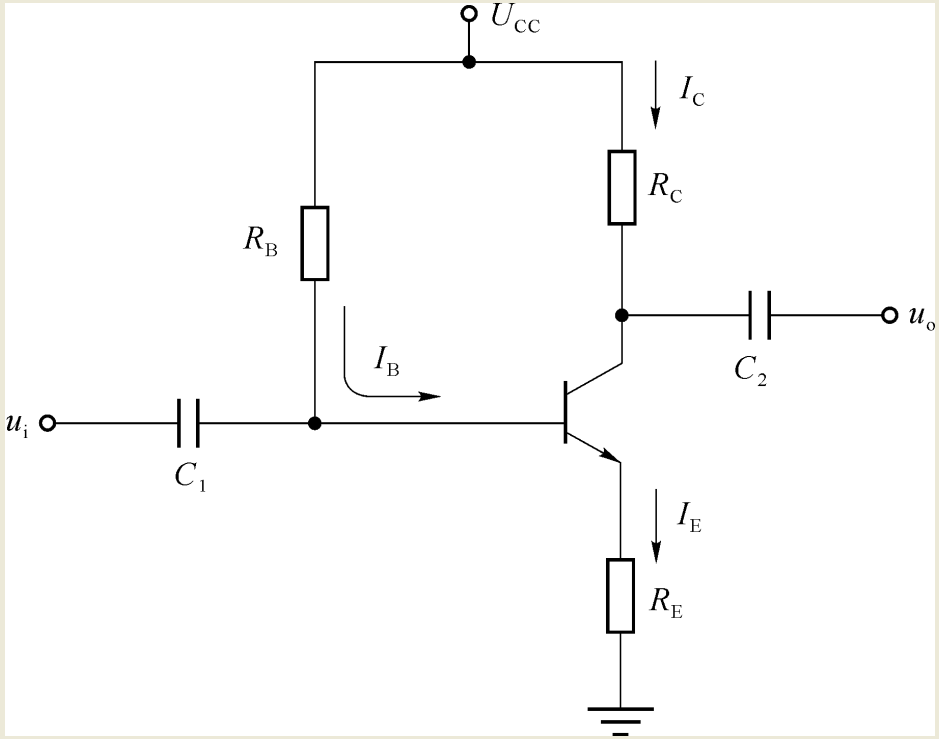




DC Analysis – Emitter Bias

Improve stability:

Adding a resistor (R_E) to the Emitter improves the *stability* of a transistor.



Stability **refers to a bias circuit in which the currents and voltages will remain fairly constant for a wide range of temperatures and transistor Beta (β) values.**

DC Analysis – Emitter Bias

Base-Emitter Loop

From Kirchhoff's voltage law :

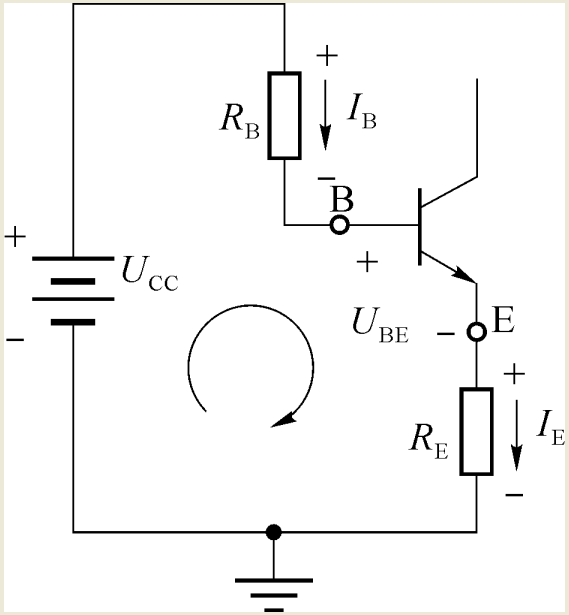
$$+U_{CC}-I_BR_B-U_{BE}-I_ER_E = 0$$

Since $I_E = (\beta + 1)I_B$:

$$U_{CC}-U_{BE}-I_BR_B-(\beta+1)I_BR_E = 0$$

Solving I_B:

$$I_B = \frac{U_{CC}-U_{BE}}{R_B+(\beta+1)R_E}$$



Collector-Emitter Loop

The collector current is given by:

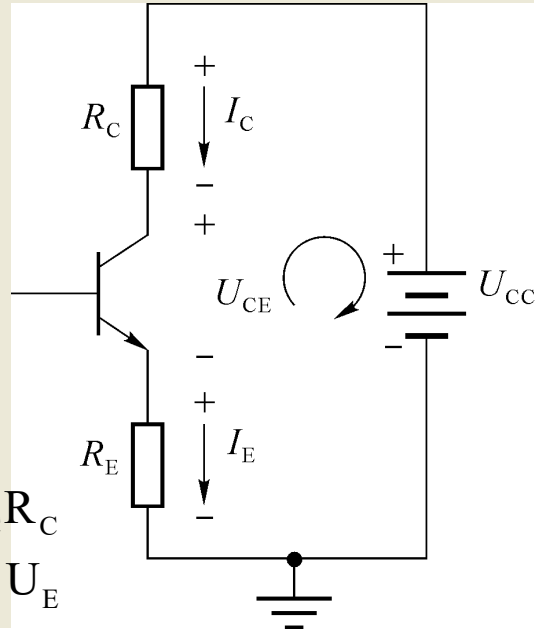
$$I_C = \beta I_B$$

From Kirchhoff's voltage law :

$$+I_ER_E + U_{CE} + I_CR_C - U_{CC} = 0$$

Since $I_E \cong I_C$:

$$U_{CE} = U_{CC} - I_C(R_C + R_E)$$



Also:

$$U_E = I_ER_E$$

$$U_C = U_{CE} + U_E = U_{CC} - I_CR_C$$

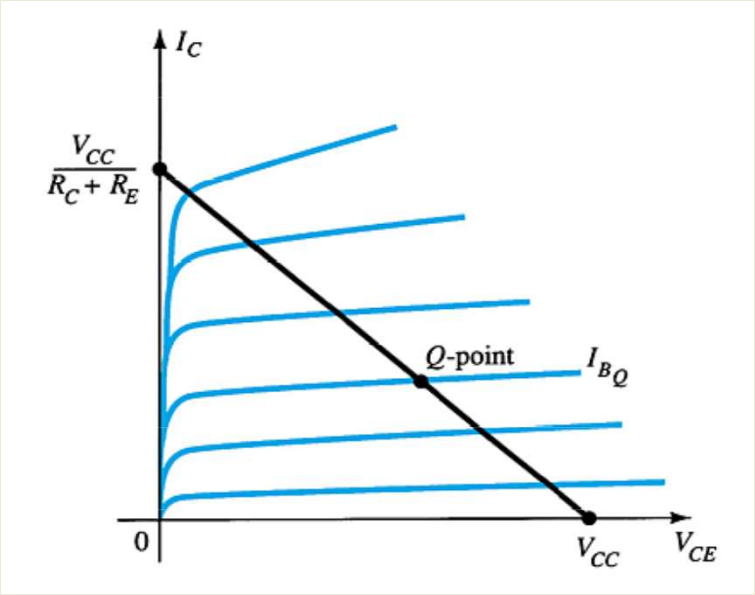
$$U_B = U_{CC} - I_RR_B = U_{BE} + U_E$$

The role of R_E?

Load line Analysis

Load equation by KVL:

$$U_{CE} = U_{CC} - I_C(R_C + R_E)$$



The endpoints can be determined from the load line.

$V_{CEcutoff}$:

$$U_{CE} = U_{CC}$$

$$I_C = 0 \text{ mA}$$

I_{Csat}:

$$U_{CE} = 0 \text{ V}$$

$$\mathbf{I_C = \frac{U_{CC}}{R_C + R_E}}$$

DC Analysis - Voltage Divider Bias

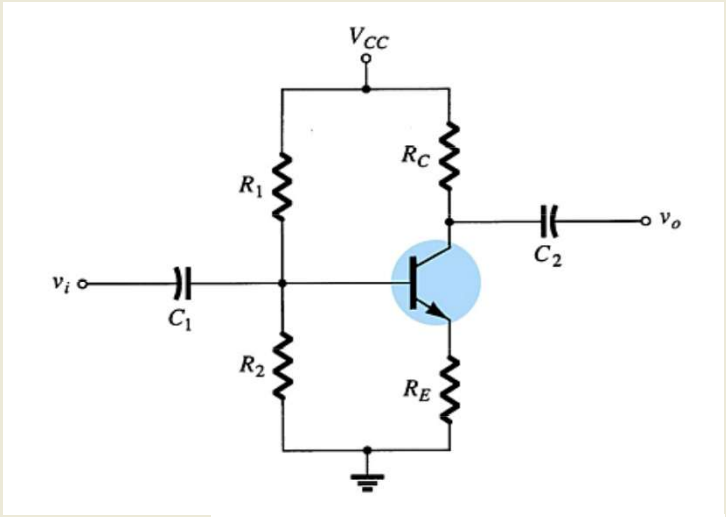
This is a very stable bias circuit.

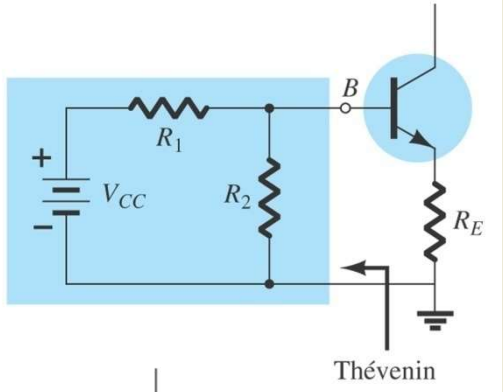
The currents and voltages are almost independent of variations in β.

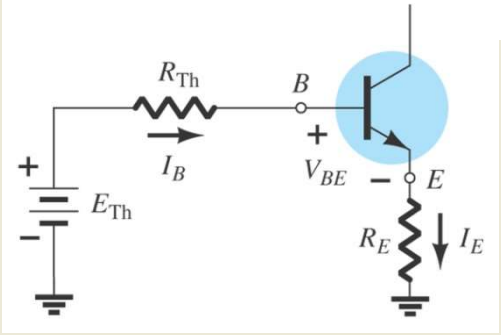
$$I_B = \frac{E_{Th} - U_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$I_C = \beta I_B = \frac{\beta(E_{Th} - U_{BE})}{R_{Th} + (\beta + 1)R_E}$$

$$U_{CE} = U_{CC} - I_C(R_C + R_E)$$







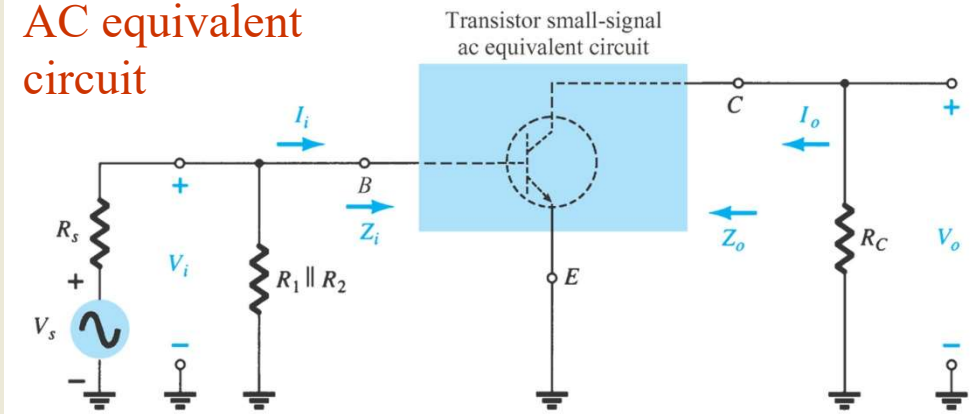
$$R_{Th} = R_1 \| R_2$$

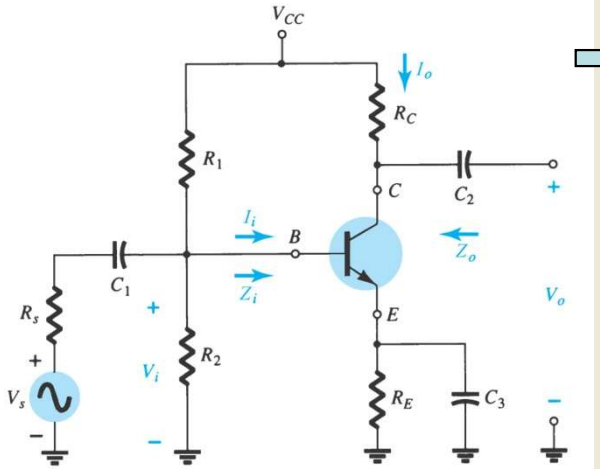
$$E_{Th} = \frac{R_2 U_{CC}}{R_1 + R_2}$$

AC Analysis: BJT Transistor Modeling

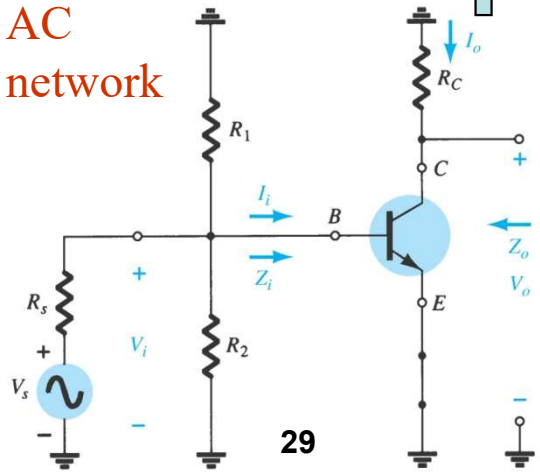
- **A model is an equivalent circuit that represents the AC characteristics of the transistor.**
- **A model uses circuit elements that approximate the behavior of the transistor.**
- **There are three models commonly used in small signal AC analysis of a transistor:**
  - **r_e model**
  - **Hybrid equivalent model**
  - **Hybrid ∏ model**

AC equivalent circuit





AC network



Sketch an AC network:

1. **Remove DC supplies (replaced by short).**
2. **The coupling capacitor and bypass capacitor can be replaced by a short.**

The r_e Transistor Model

BJTs are basically current-controlled devices, therefore the r_e model uses a diode and a current source to duplicate the behavior of the transistor.

One disadvantage to this model is its sensitivity to the DC level.

Common-Base Configuration

$$I_c = \alpha I_e \qquad r_e = \frac{26\,\text{mV}}{I_E}$$

Input impedance: Low

$$Z_i = r_e$$

Output impedance: High

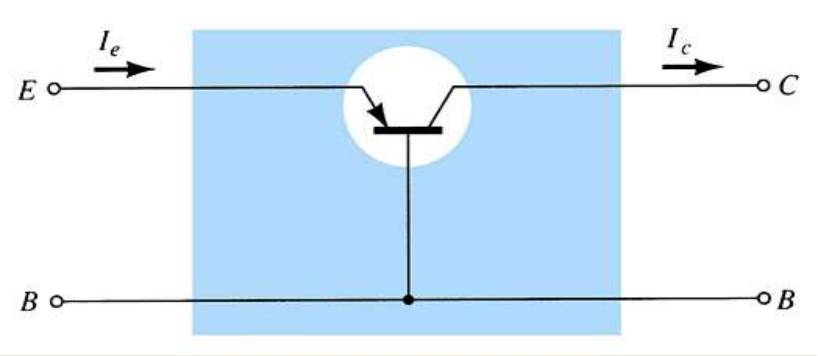
$$Z_o \cong \infty\Omega$$

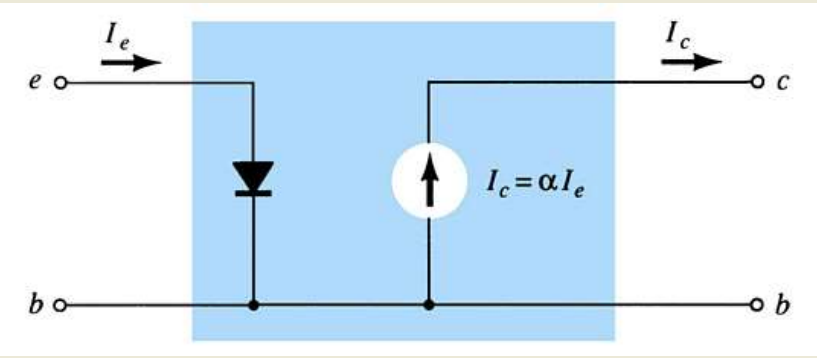
Voltage gain: voltage amplification

$$A_u = \frac{\alpha R_L}{r_e} \cong \frac{R_L}{r_e}$$

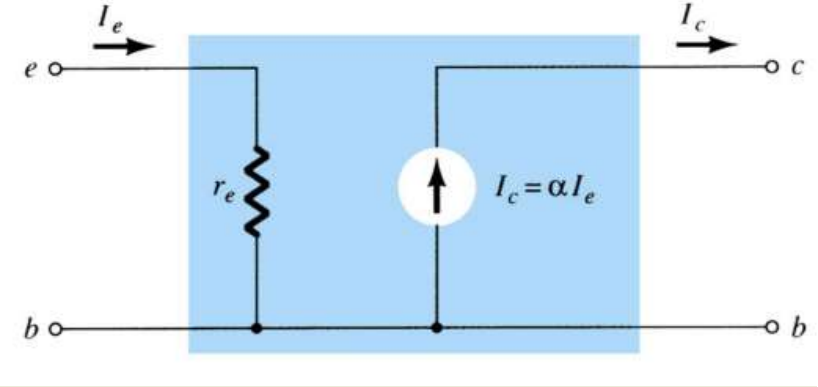
Current gain: No current amplification

$$A_i = -\alpha \cong -1$$





r_e model for CB configuration



Common-Emitter Configuration

The diode r_e model can be replaced by the resistor r_e.

$$I_e = (\beta + 1)I_b \cong \beta I_b$$

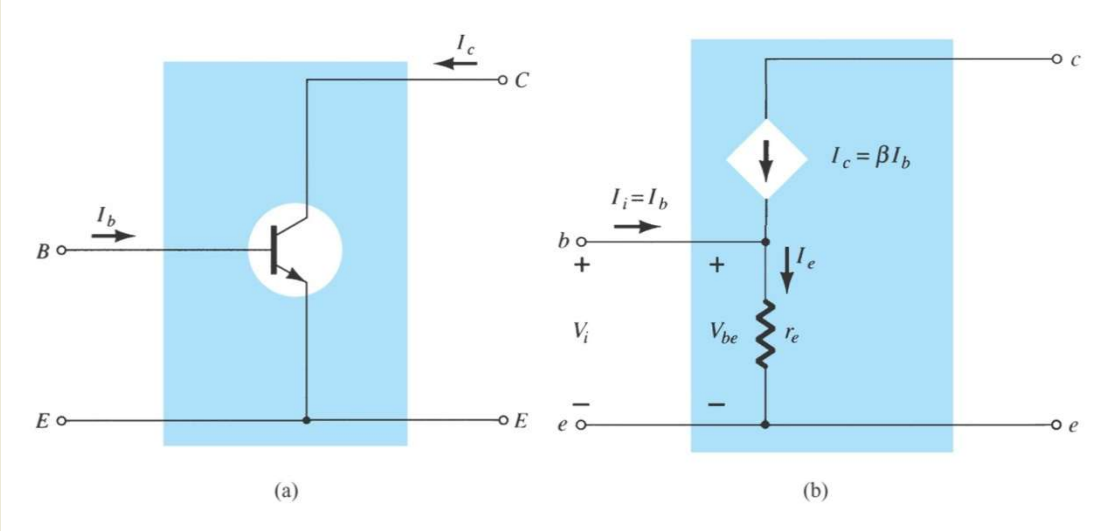
$$r_e = \frac{26\,\text{mV}}{I_e}$$

Input impedance: higher than CB

$$Z_i = \beta r_e$$

Output impedance: lower than CB

$$Z_o = r_o \cong \infty\Omega$$

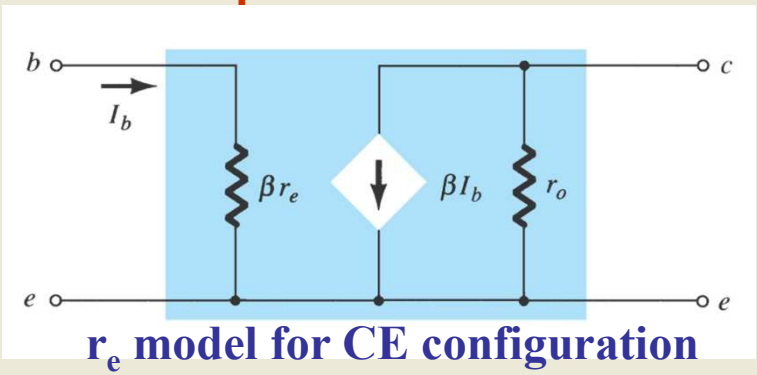


Voltage gain: Voltage amplification, u_o and u_i are 180° out of phase

$$A_u = -\frac{R_L}{r_e}$$

Current gain: Current amplification

$$A_i = \beta\big|_{r_o = \infty}$$



r_e model for CE configuration

CC: Use the Common-Emitter model for the Common-Collector configuration.

AC Analysis with Equivalent models

CE with Fixed-bias

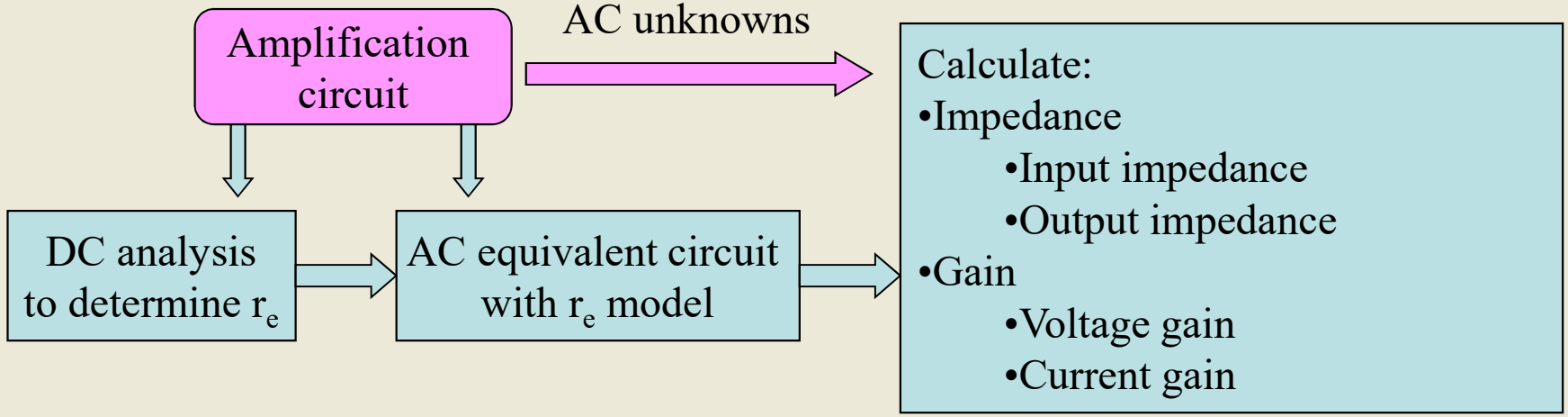
CE with Voltage-divider bias

CE with Emitter bias

} ***CE***

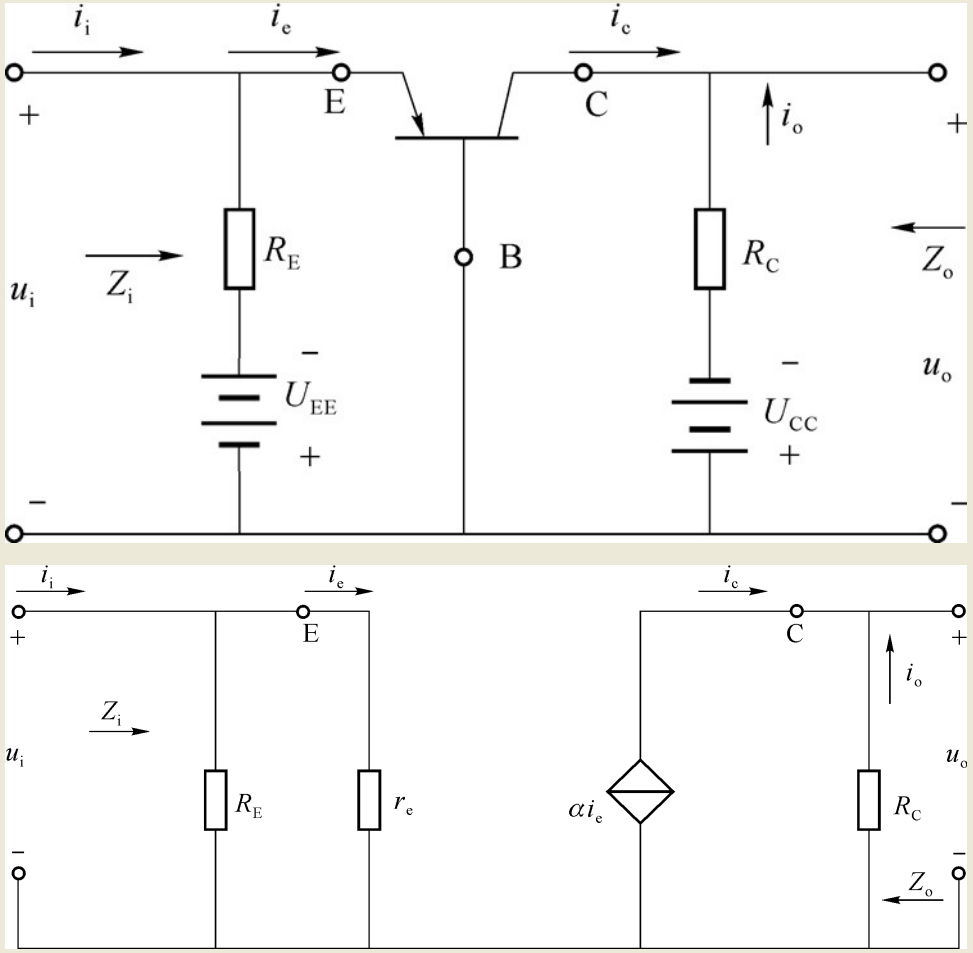
CC: Emitter follower

CB



Common-Base Configuration

- **The input is applied to the emitter**
- **The output is from the collector**
  - ***Low input impedance***
  - ***High output impedance***
  - ***Current gain less than unity***
  - ***Very high voltage gain***
  - ***No phase shift between input and output***



Input impedance:

$$Z_i = R_E \parallel r_e$$

Output impedance:

$$Z_o = R_C$$

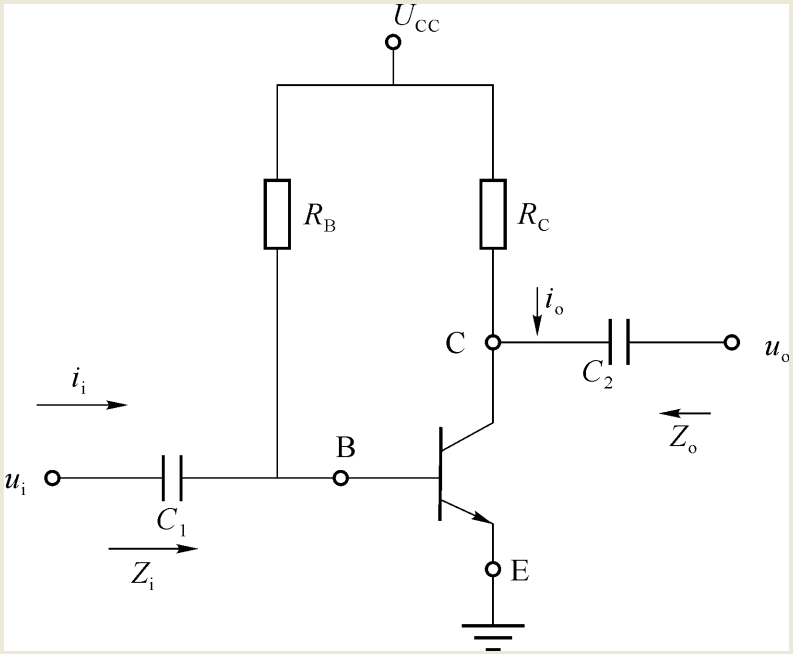
Voltage gain:

$$A_u = \frac{u_o}{u_i} = \frac{\alpha R_C}{r_e} \cong \frac{R_C}{r_e}$$

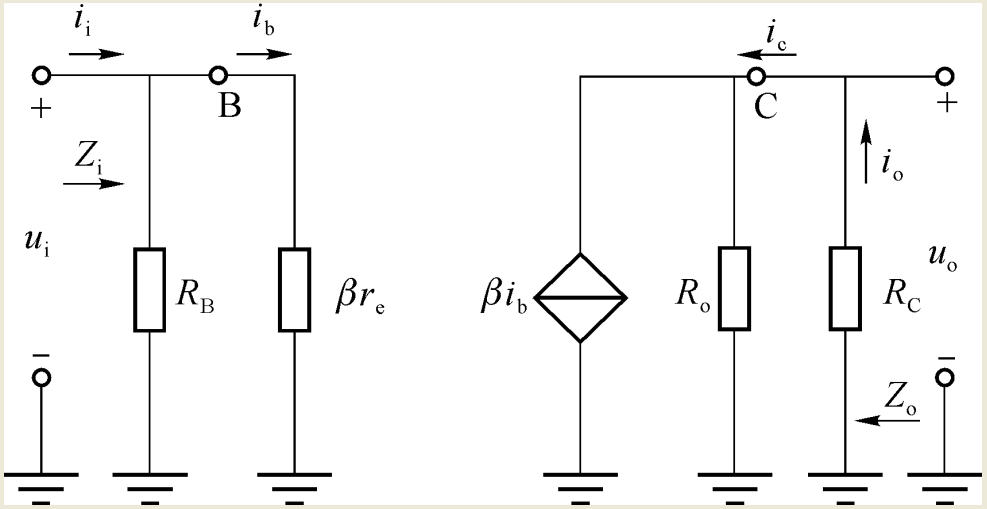
Current gain:

$$A_i = \frac{I_o}{I_i} = -\alpha \cong -1$$

Common-Emitter: Fixed-Bias Calculations



AC equivalent with r_e model



- **The input is applied to the Base**
- **The output is from the Collector**
  - ***High input impedance***
  - ***Low output impedance***
  - ***High voltage and current gain***
  - ***Phase shift between input and output is 180°***

Common-Emitter: Fixed-Bias Calculations

Input impedance:

$$Z_i = R_B \| \beta r_e$$

$$Z_i \cong \beta r_e \Big|_{R_B \geq 10 \beta r_e}$$

Output impedance:

$$Z_o = R_C \| r_O$$

$$Z_o \cong R_C \Big|_{r_o \geq 10 R_C}$$

Voltage gain:

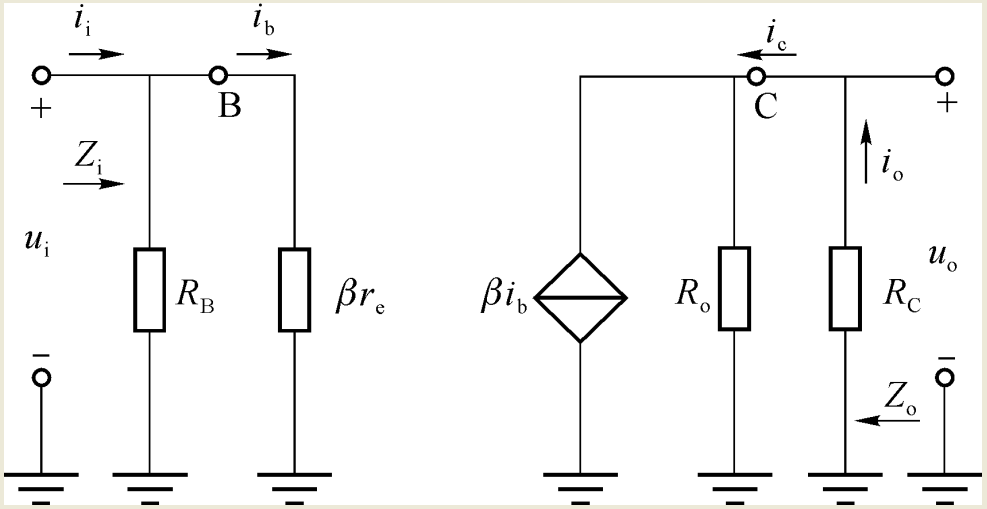
$$A_u = \frac{u_o}{u_i} = -\frac{(R_C \| r_o)}{r_e}$$

$$A_u = -\frac{R_C}{r_e} \Big|_{r_o \geq 10 R_C}$$

Current gain (from voltage gain):

$$A_i = -A_u \frac{Z_i}{R_C}$$

AC equivalent with r_e model



Common-Emitter: Emitter-Bias Configuration

Input impedance:

$$Z_i = R_B \,\|\, Z_b$$

$$Z_b = \beta r_e + (\beta + 1) R_E$$

Output impedance:

$$\mathbf{Z_o = R_C}$$

Voltage gain:

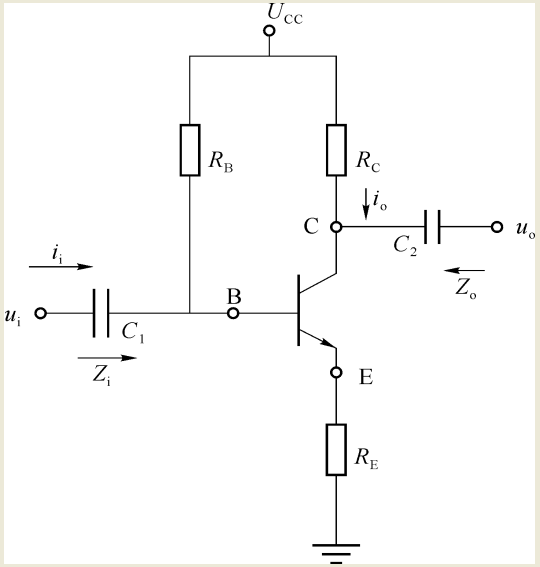
$$A_u = \frac{u_o}{u_i} = -\frac{\beta R_C}{Z_b}$$

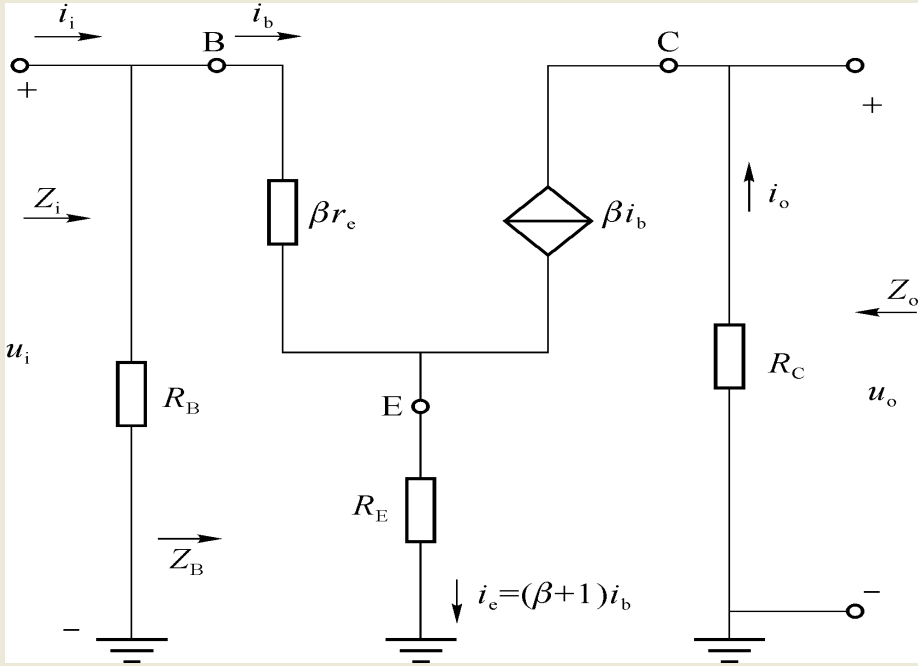
$$A_u = \frac{u_o}{u_i} = -\frac{R_C}{r_e + R_E}\bigg|_{Z_b = \beta(r_e + R_E)}$$

$$A_u = \frac{u_o}{u_i} \cong -\frac{R_C}{R_E}\bigg|_{Z_b \cong \beta R_E}$$

Current gain from voltage gain:

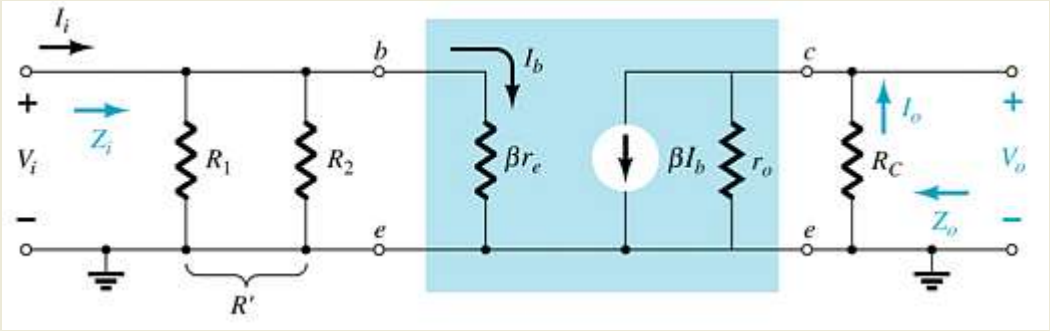
$$A_i = -A_u \frac{Z_i}{R_C}$$

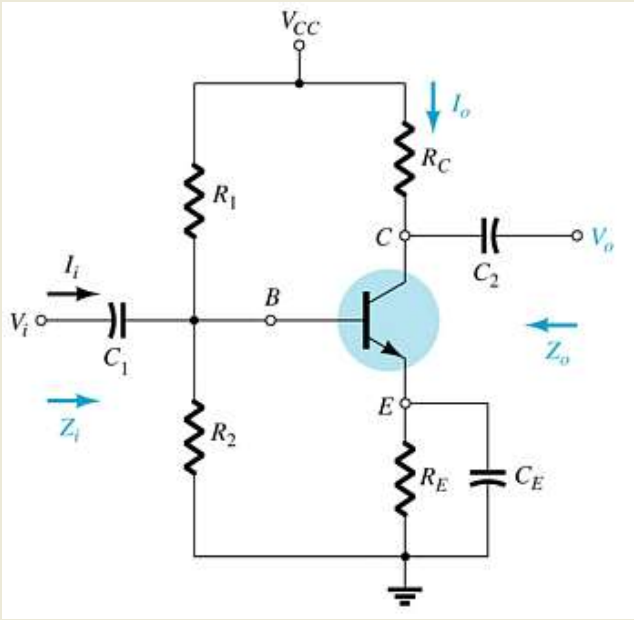




Common-Emitter: Voltage-Divider Bias

r_e model requires you to determine β and r_e.





Input impedance:

$$R' = R_1 \parallel R_2$$

$$Z_i = R' \parallel \beta r_e$$

Output impedance:

$$Z_o = R_C \parallel r_o$$

$$Z_o \cong R_C \Big|_{r_o \geq 10R_C}$$

Voltage gain:

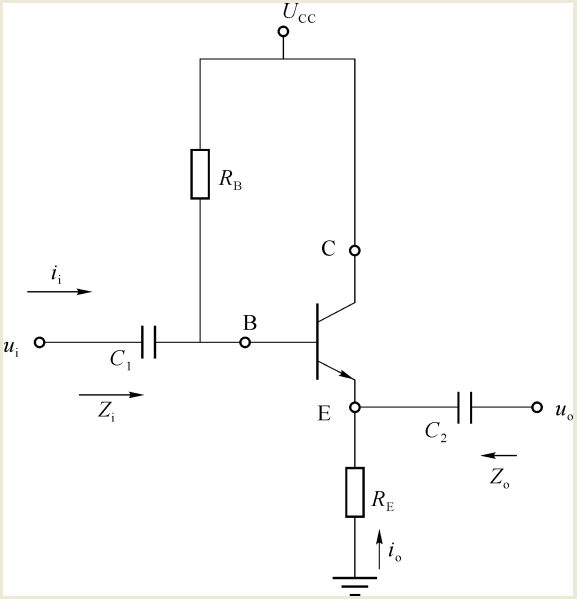
$$A_u = \frac{u_o}{u_i} = \frac{-R_C \parallel r_o}{r_e}$$

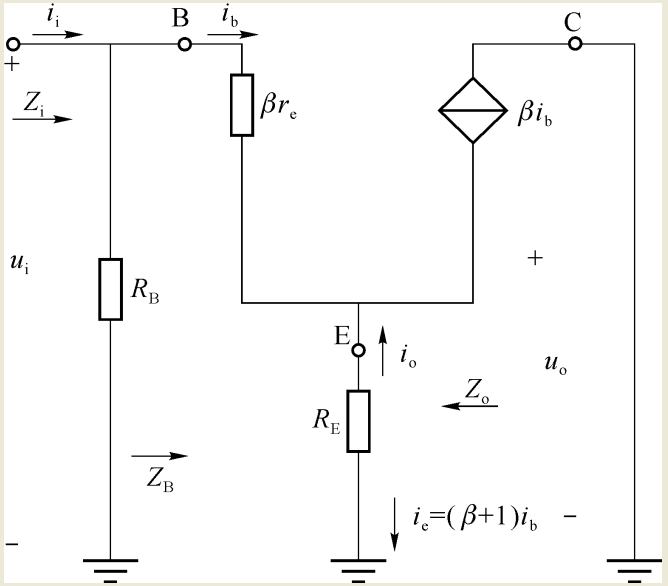
$$A_u = \frac{u_o}{u_i} \cong -\frac{R_C}{r_e}\Big|_{r_o \geq 10R_C}$$

Current gain from voltage gain:

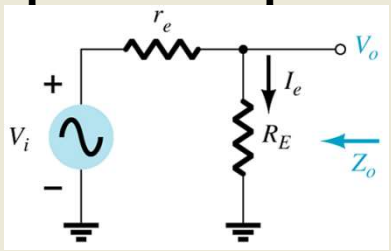
$$A_i = -A_u \frac{Z_i}{R_C}$$

CC: Emitter-Follower Configuration





- **Emitter-follower is also known as the CC configuration.**
- **The input is applied to the Base and the output is taken from the Emitter.**
- **There is no phase shift between input and output.**



Input impedance:

$$Z_i = R_B \parallel Z_b$$

$$Z_b = \beta r_e + (\beta + 1)R_E$$

$$Z_b \cong \beta(r_e + R_E)$$

$$Z_b \cong \beta R_E$$

Output impedance:

$$Z_o = R_E \parallel r_e$$

$$Z_o \cong r_e \Big| \; R_E >> r_e$$

Voltage gain:

$$A_u = \frac{u_o}{u_i} = \frac{R_E}{R_E + r_e}$$

$$A_u = \frac{u_o}{u_i} \cong 1 \Big| \; R_E >> r_e,\ R_E + r_e \cong R_E$$

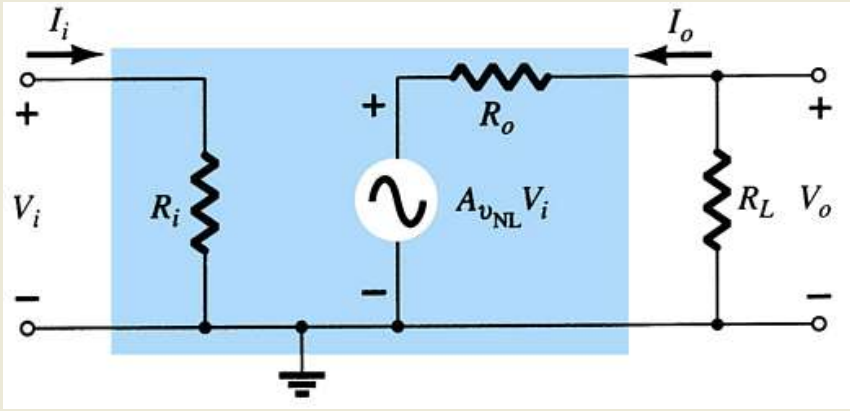
Current gain :

$$A_i = -A_u \frac{Z_i}{Z_o}$$

Effect of Load Impedance on Gain

This model can be applied to any current- or voltage-controlled amplifier.

Adding a load *reduces* the gain of the amplifier:

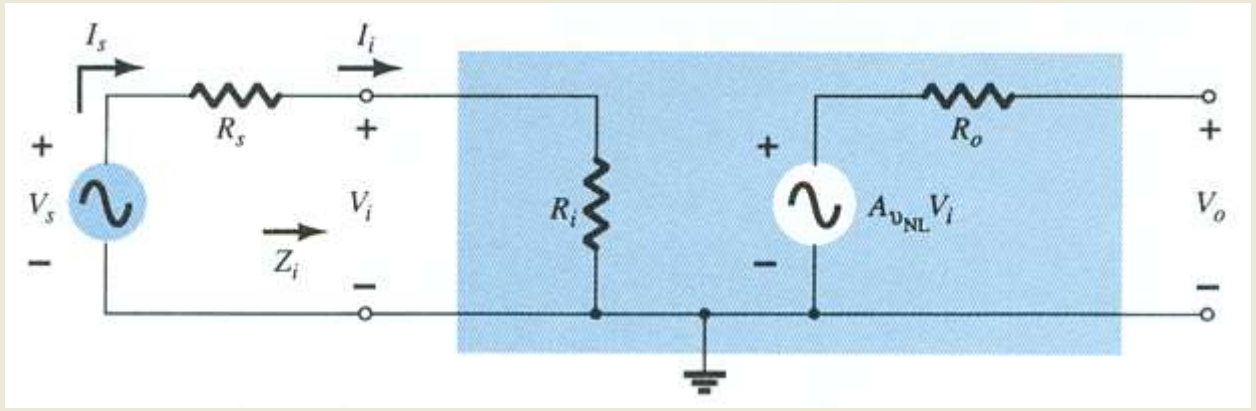


$$A_u = \frac{u_o}{u_i} = \frac{R_L}{R_L + R_o} A_{uNL}$$

$$u_o = \frac{\mathbf{R_L}}{\mathbf{R_L + R_o}} \mathbf{A}_{u_{NL}} u_i$$

Effect of Source Impedance on Gain

The fraction of applied signal that reaches the input of the amplifier is:



$$u_i = \frac{R_i u_s}{R_i + R_s}$$

$$u_o = \mathbf{A}_{u_{NL}} u_i = \mathbf{A}_{u_{NL}} \frac{\mathbf{R}_i u_s}{\mathbf{R}_i + \mathbf{R}_s}$$

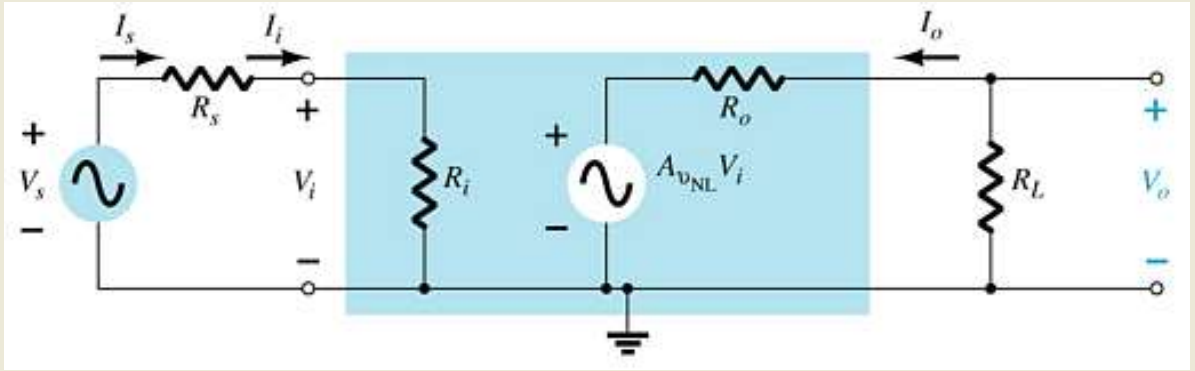
The internal resistance of the signal source *reduces* the gain:

$$A_{us} = \frac{u_o}{u_s} = \frac{R_i}{R_i + R_s} A_{uNL}$$

Combined Effects of R_S and R_L on Voltage Gain

Effects of R_L:

$$A_u = \frac{u_o}{u_i} = \frac{R_L A_{uNL}}{R_L + R_o}$$



$$u_o = \frac{R_L}{R_L + R_o} A_{u_{NL}} u_i = \frac{R_L}{R_L + R_o} A_{u_{NL}} \frac{R_i u_s}{R_i + R_s}$$

Effects of R_L and R_S:

$$A_{us} = \frac{u_o}{u_s} = \frac{R_i}{R_i + R_s} \frac{R_L}{R_L + R_o} A_{uNL}$$

Key Points of Chapter 2

- **Bipolar Junction Transistors**
  - Structures and Characteristics
- **DC Biasing BJTs**
  - DC Analysis
  - Graphical Analysis
- **BJT AC analysis**
  - Fundamental Principle of Amplifier
  - AC Small-Signal Equivalent Circuits
- **Basic BJT Amplifiers**
  - Basic BJT Amplifiers
  - Basic Amplifier Configurations
  - The Common-Emitter Amplifier
  - The Common-Collector Amplifier
  - The Common-Base Amplifier