Introduction to Electronic Systems

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Part 1: Resistive Circuit Analysis

1. Circuit Variables and Circuit Elements
2. **Simple Resistive Circuit Analysis**
3. Techniques of Circuit Analysis
4. Operational Amplifier

Chapter 2: Simple Resistive Circuit Analysis

- Kirchhoff's Laws
- Analysis of Simple Circuit Containing Controlled Sources
- Resistors in Series and in Parallel

2-1 Kirchhoff's Laws

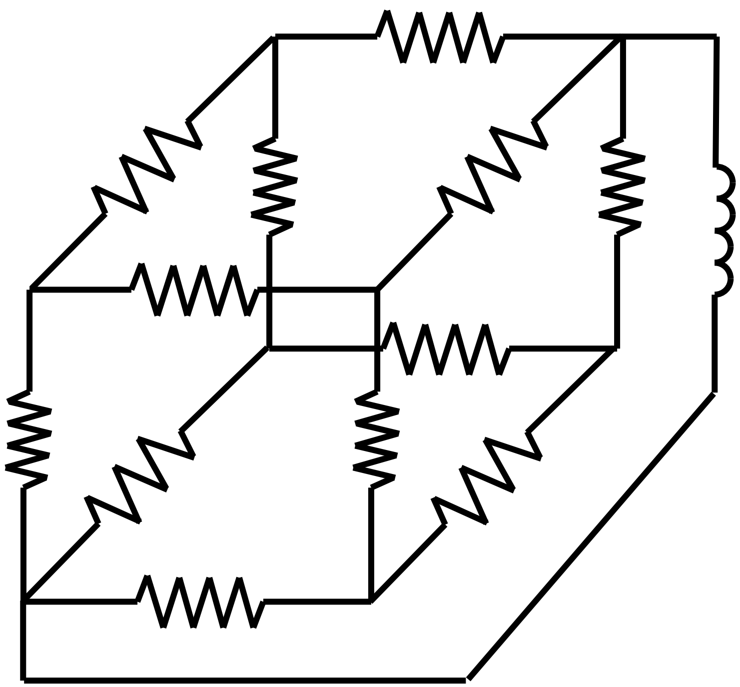
- Definitions for Circuit Topology
- Kirchhoff's Current Law (KCL)
- Kirchhoff's Voltage Law (KVL)

Some Definitions

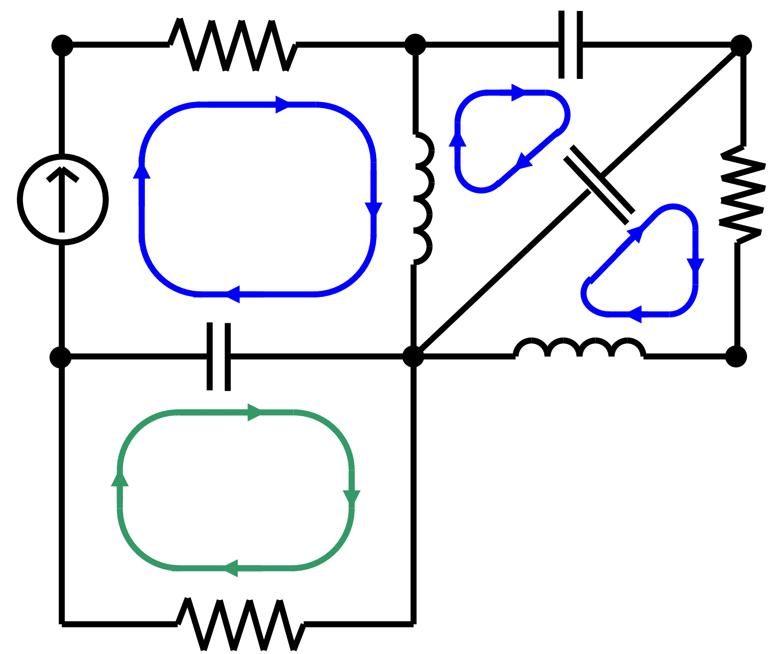
- Node
- Path
- Loop
- Branch
- Mesh

Planar circuit

A non-planar circuit



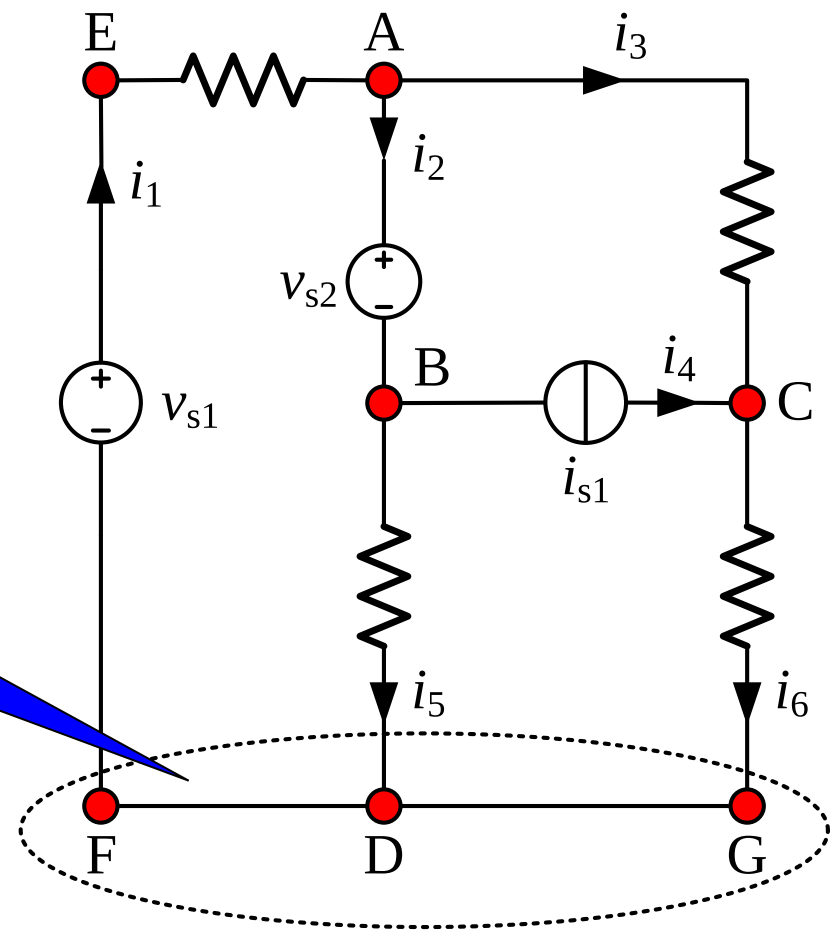
A planar circuit



Node (1)

- A point which two or more elements have
  conn
  calle

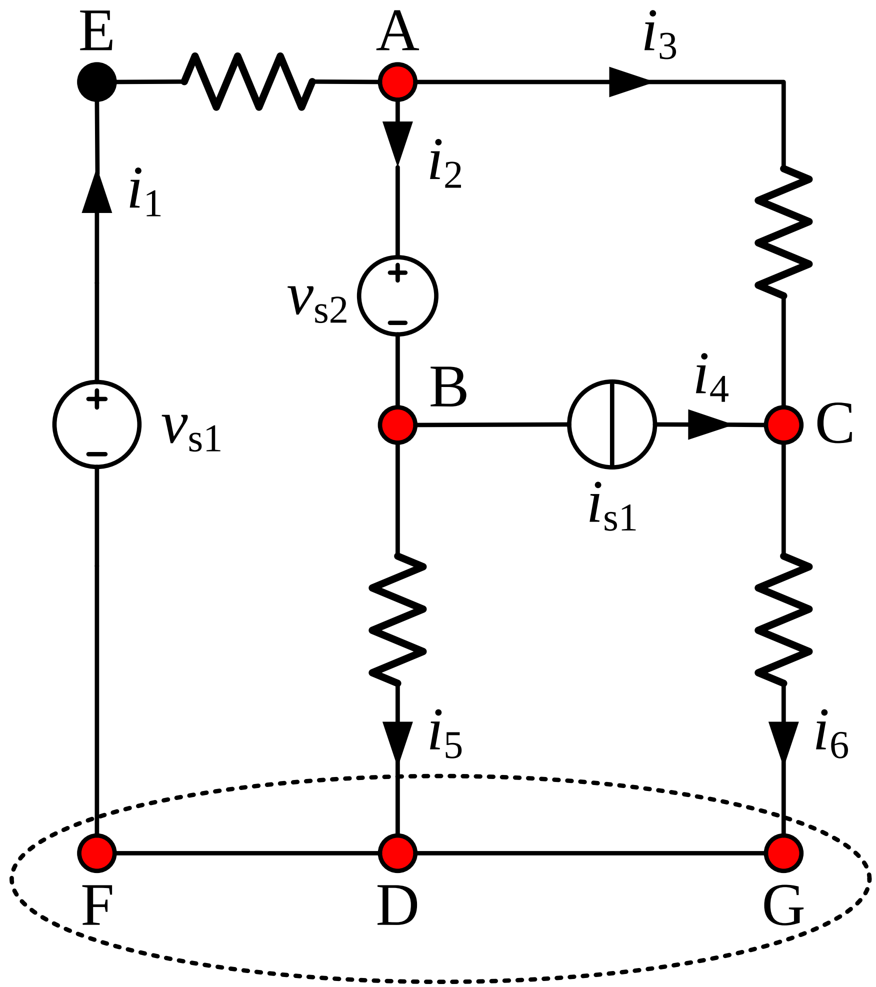
This is all one NODE.



Node (2)

- **Essential NODE:**

  A node where three or more elements join.



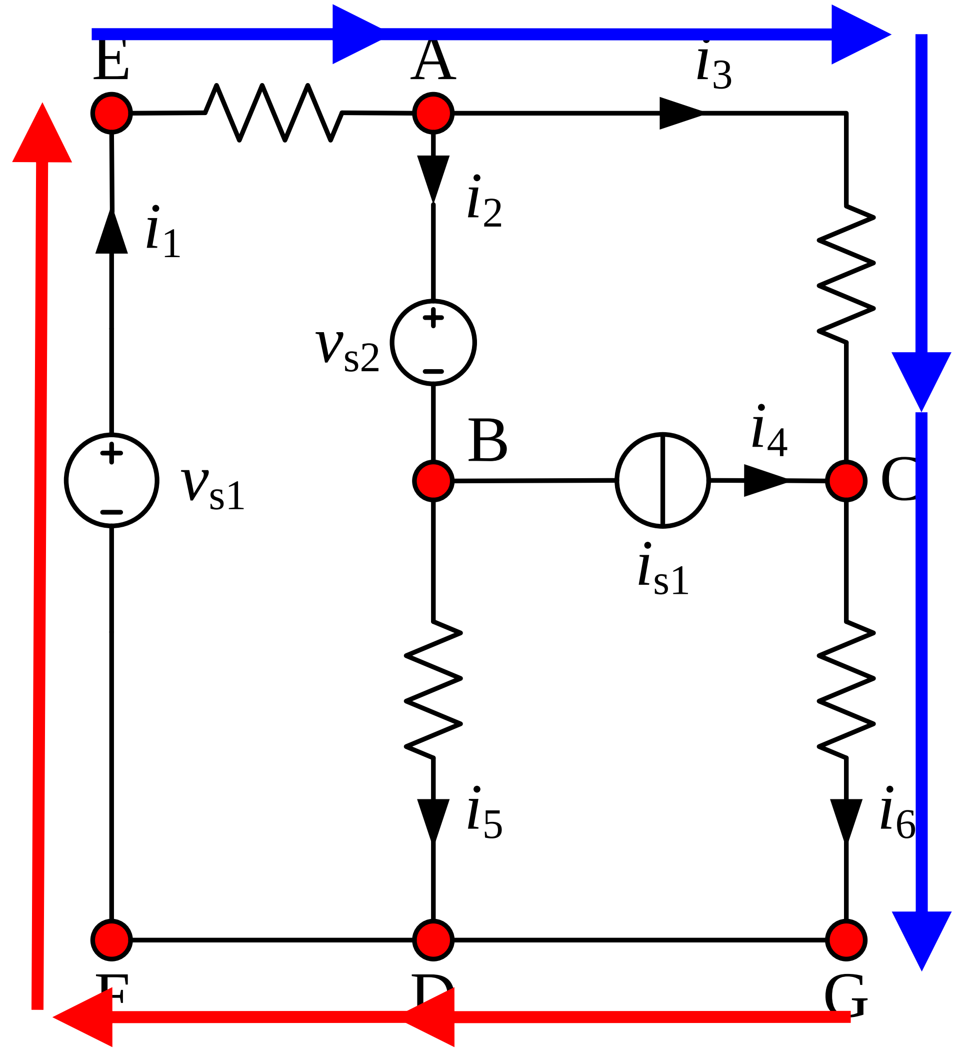
Node (3)

Notes:

- A NODE is a point where two or more circuit elements meet;
- Consider all of the perfect conducting wires as part of a NODE;
- Every element has a NODE at each of its terminals.

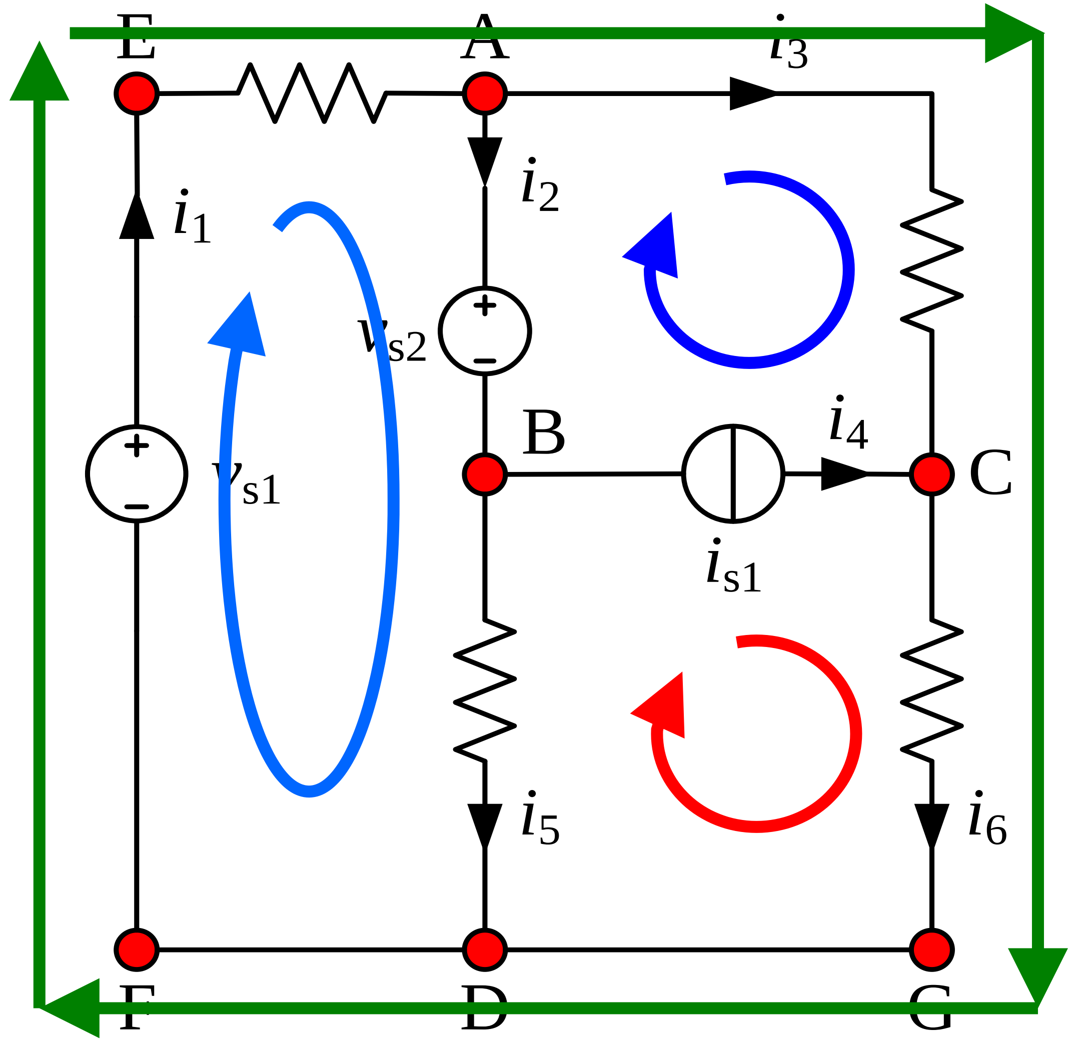
Path

- A **PATH** is a trace of adjoining basic elements with no intermediate nodes included more than once.



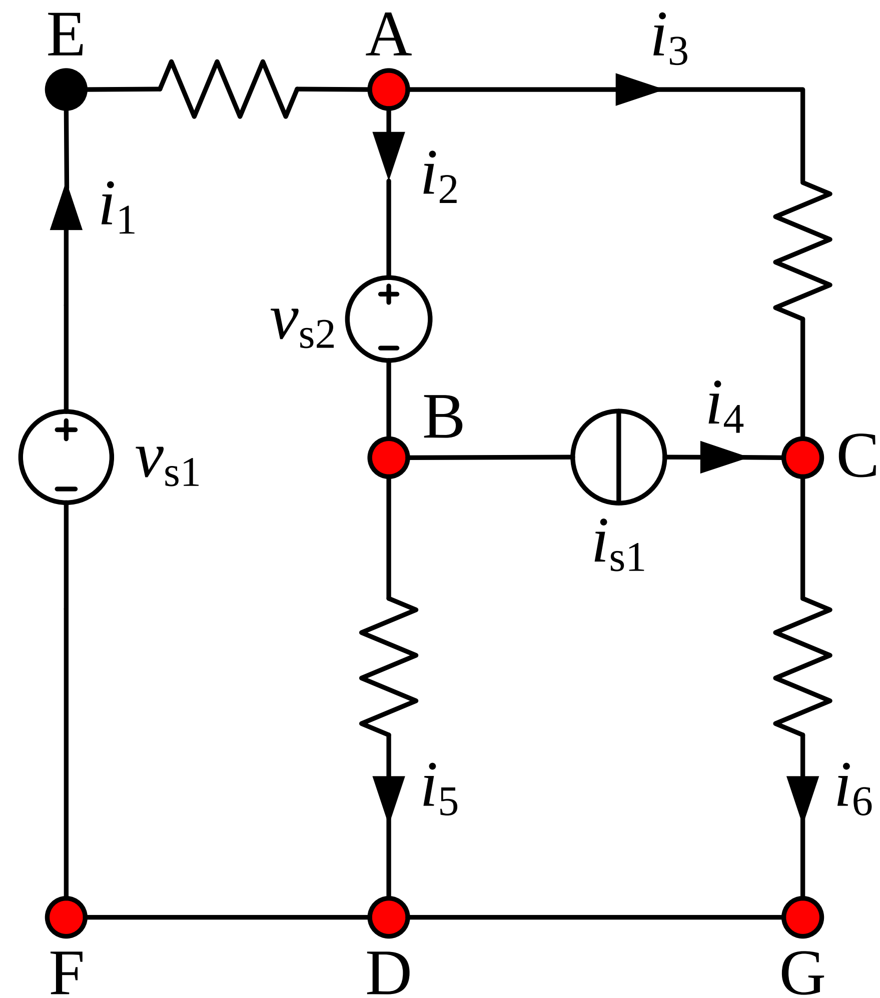
Loop

- A **LOOP** is a path whose last node is the same as the starting node, or a closed path.



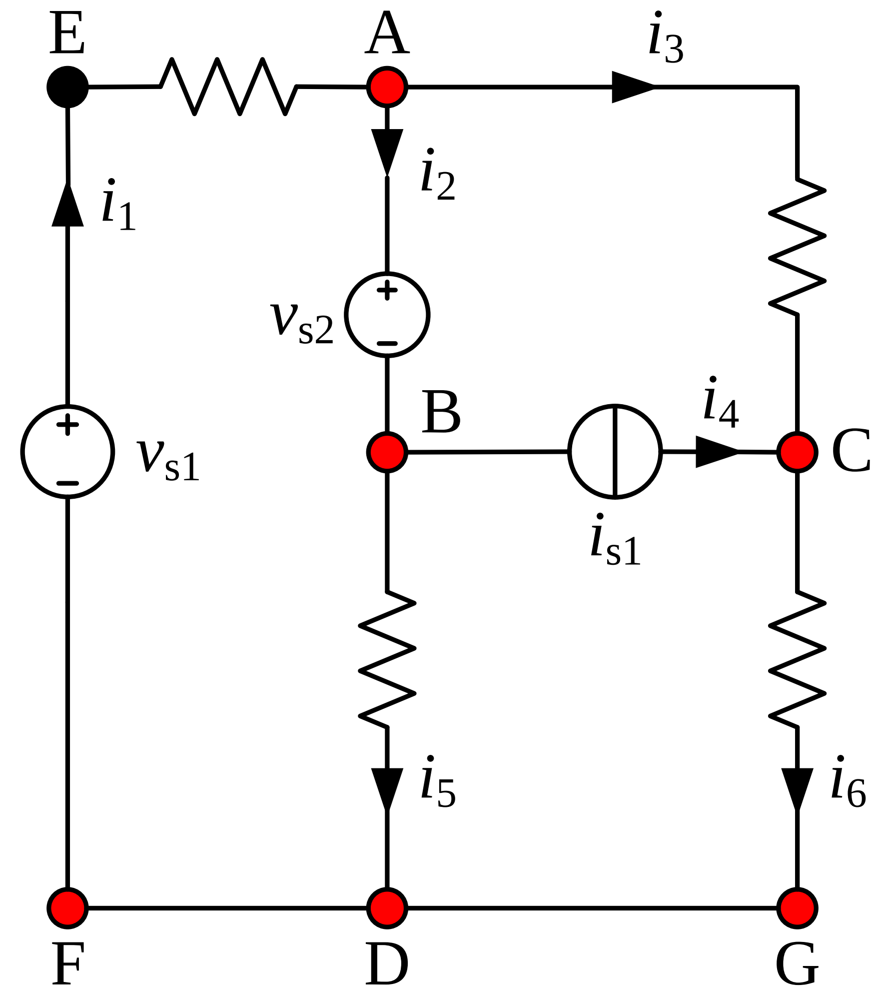
Branch (1)

- A **BRANCH** is defined as a path that connects two adjoining nodes.



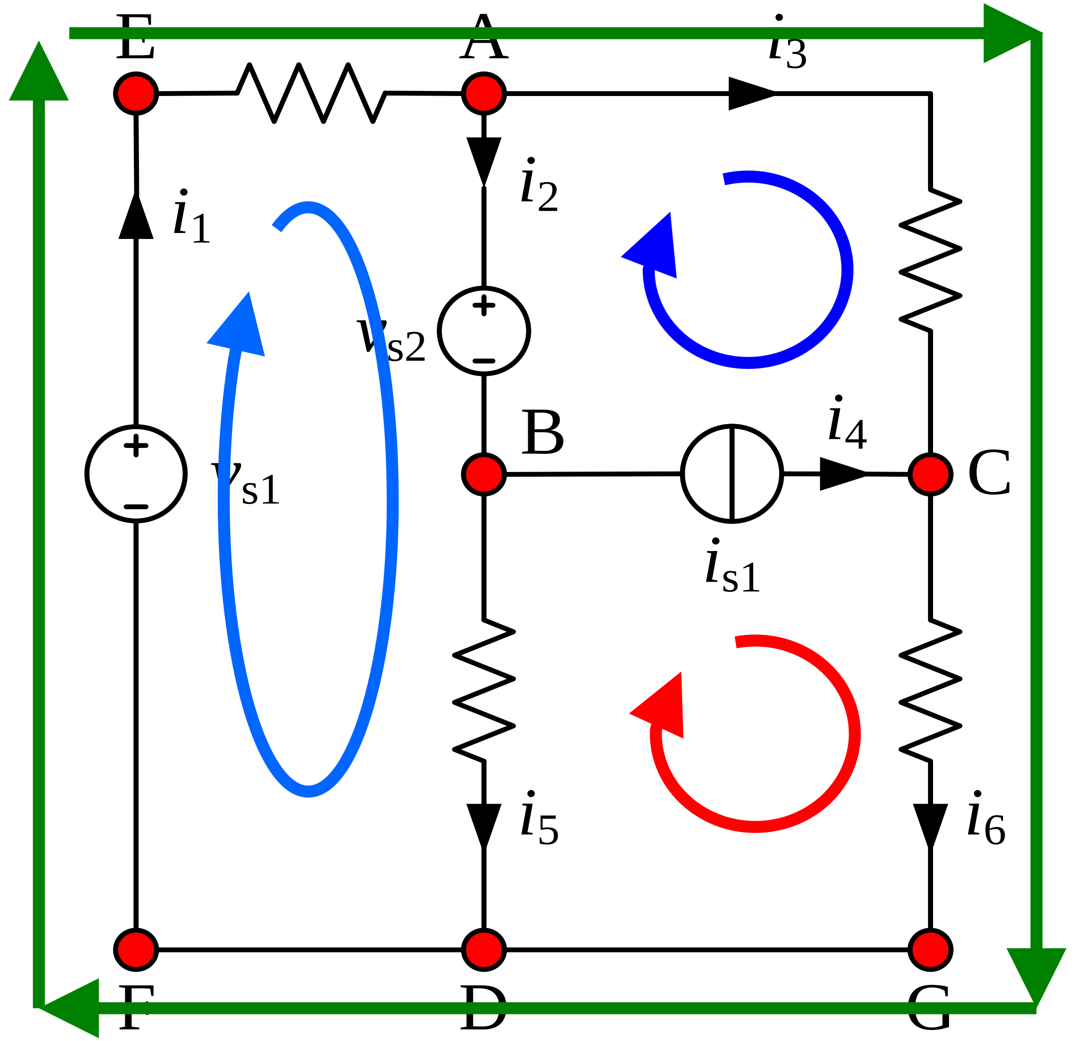
Branch (2)

- **Essential branch**
  - Connects two essential nodes without passing through any essential node.

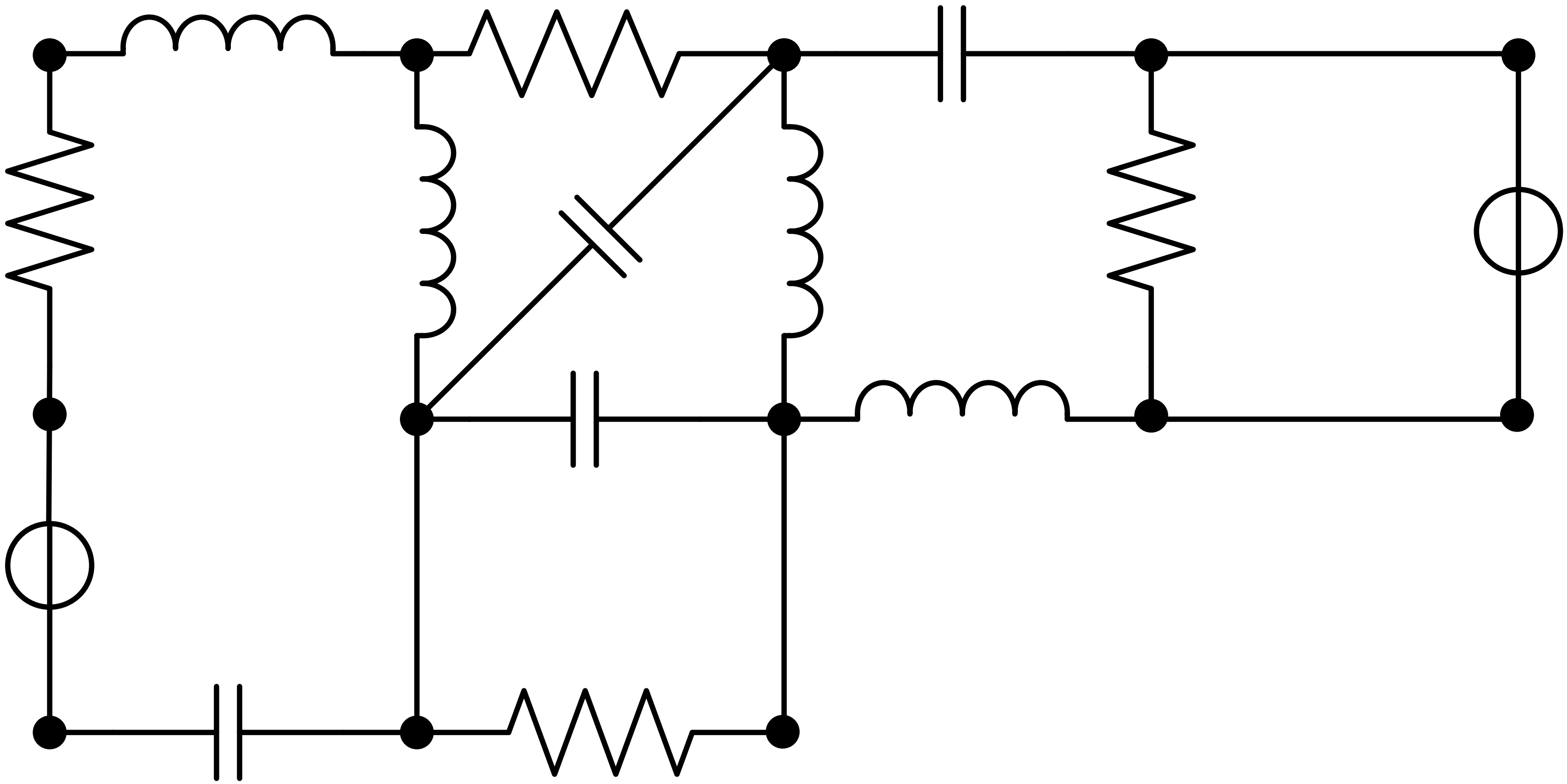


Mesh (1)

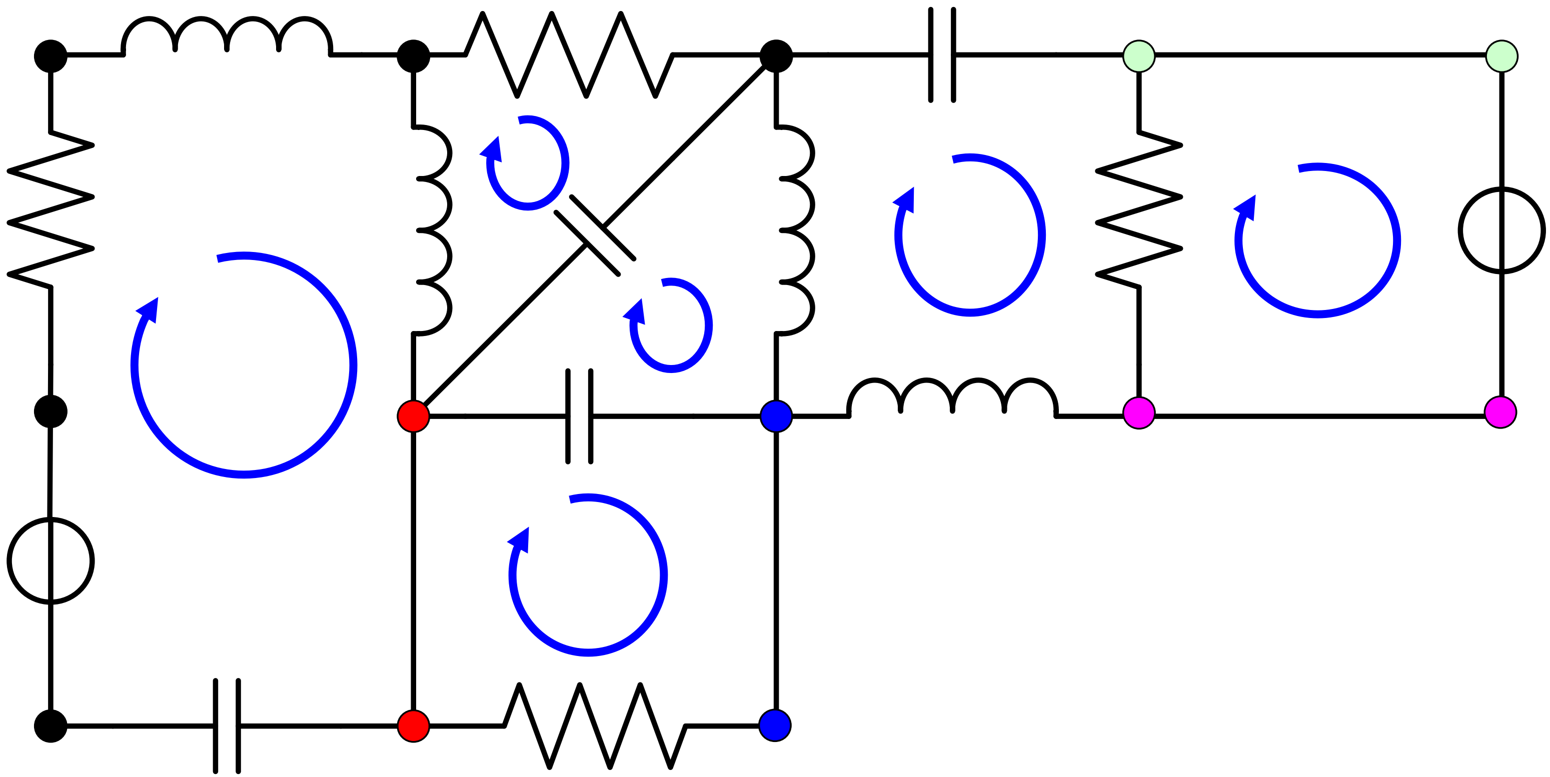
- A **MESH** is: defined as a loop that does not contain any other loops within it.
- Mesh does not enclose any branches.



How many branches, nodes, meshes?



How many branches, nodes, meshes?



ANS: 14 branches; 9 nodes; 6 meshes

Kirchhoff's Laws

Topology Constraint + **Element Constraint** = **Circuit Behavior**

Topology Constraint → **KCL, KVL**

Element Constraint → **Ohm's Law*** / **IVS, ICS, …**

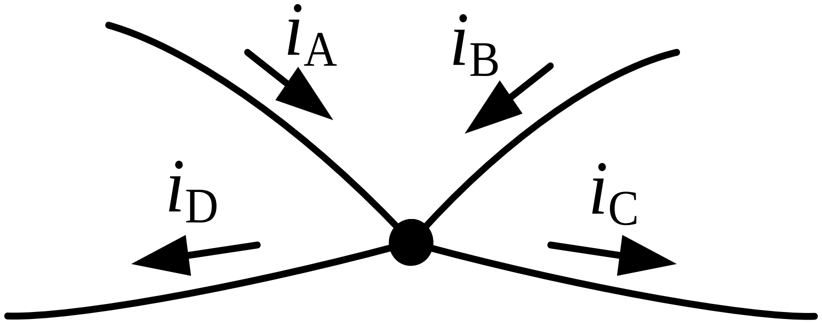
* For resistive elements

Kirchhoff's Current Law (KCL)

KCL: The algebraic sum of all the currents entering any node in a circuit is zero.

$$\sum_{n=1}^{N} i_n(t) = 0$$

Kirchhoff's Current Law (KCL)



$$i_A + i_B + (-i_C) + (-i_D) = 0$$

Or:

$$(-i_A) + (-i_B) + i_C + i_D = 0$$

Or:

$$i_A + i_B = i_C + i_D$$

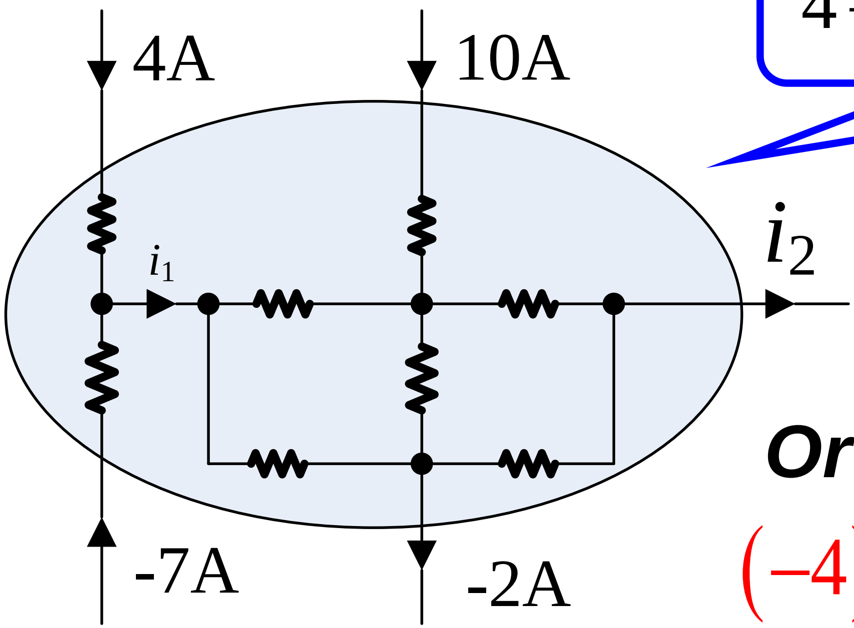
Reference direction of current is critical for KCL.

Generalization of KCL

The algebraic sum of all the currents entering any **closed surface** is zero.

$$\sum_{n=1}^{N} i_n(t) = 0$$

Generalization of KCL



$$4+(-7)+10+[-(-2)]+(-i_2)=0$$

Or:

$$(-4)+(-(-7))+(-10)+(-2)+i_2=0$$

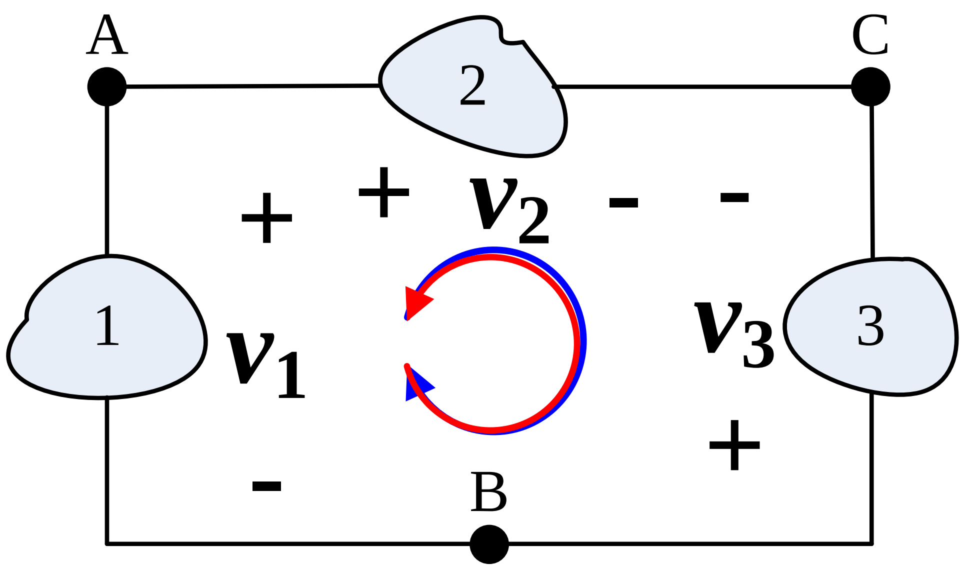
Or: $$4+(-7)+10=(-2)+i_2$$

Kirchhoff's Voltage Law (KVL)

KVL: **The algebraic sum of all the voltages around any loop in a circuit is ZERO.**

$$\sum_{n=1}^{N} v_n(t) = 0$$

Kirchhoff's Voltage Law (KVL)



$$-v_1 + v_2 - v_3 = 0$$

Or:

$$v_1 + v_3 - v_2 = 0$$

Or: $v_1 = v_2 - v_3$

Guiding direction (clockwise or anti-clockwise) is critical for KVL.

Comments on KCL

Conservation of Charge ⇨ KCL

- **A node cannot store, destroy, or generate charge**
- **Electrical charges cannot be accumulated at a node**
- **Continuity of current:**

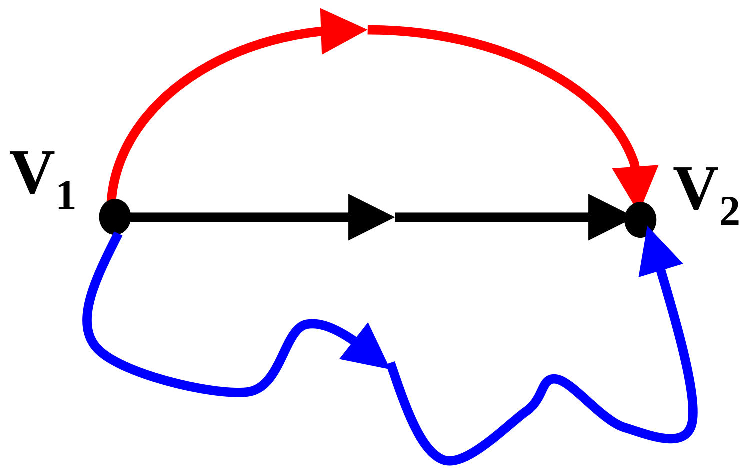
$$\oint \vec{\sigma} \cdot d\vec{s} = \frac{dq_{total}}{dt} = \sum_{n=1}^{N} i_n(t) = 0$$

Comments on KVL

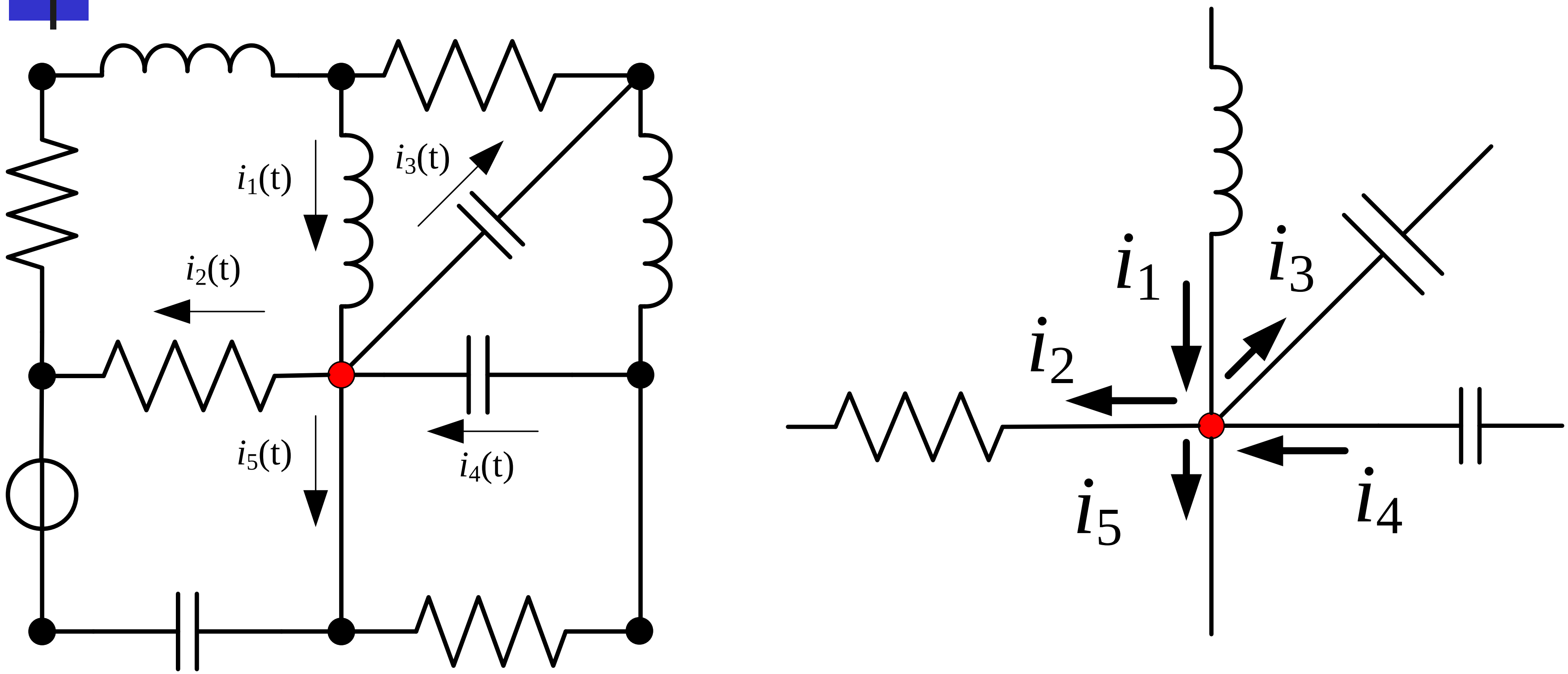
Conservation of Energy $\Rightarrow$ KVL

- **Potential difference (The energy/work required to move a unit charge) from point A to B is independent of the path taken from A to B;**

$$\oint \vec{E} \cdot d\vec{l} = \sum_{n=1}^{N} v_n(t) = 0$$

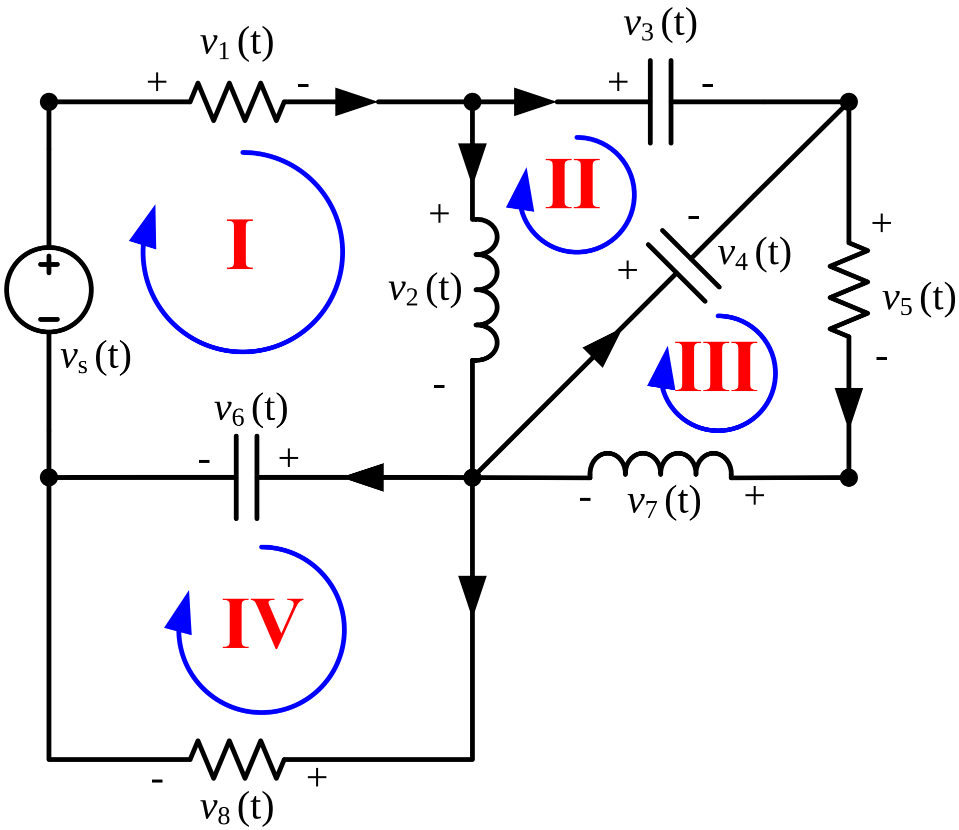


Apply KCL to a More Complex Circuit



KCL ⇨ $i_1 + (-\, i_2) + (-\, i_3) + i_4 + (-\, i_5) = 0$

Apply KVL to a More Complex Circuit



Loop I :

$$v_1 + v_2 + v_6 - v_s = 0$$

Loop II :

$$v_3 - v_4 - v_2 = 0$$

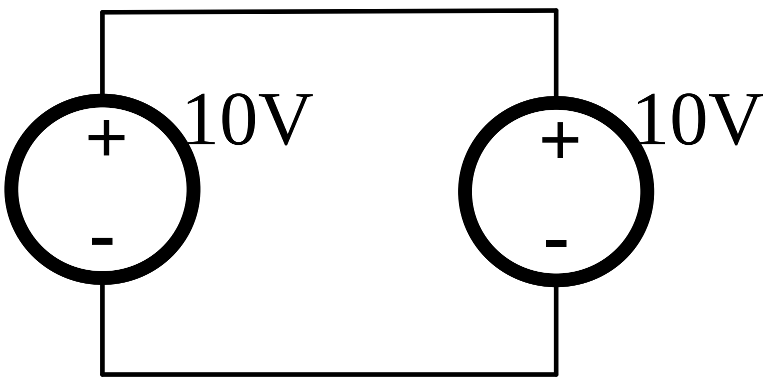
Loop III :

$$v_4 + v_5 + v_7 = 0$$

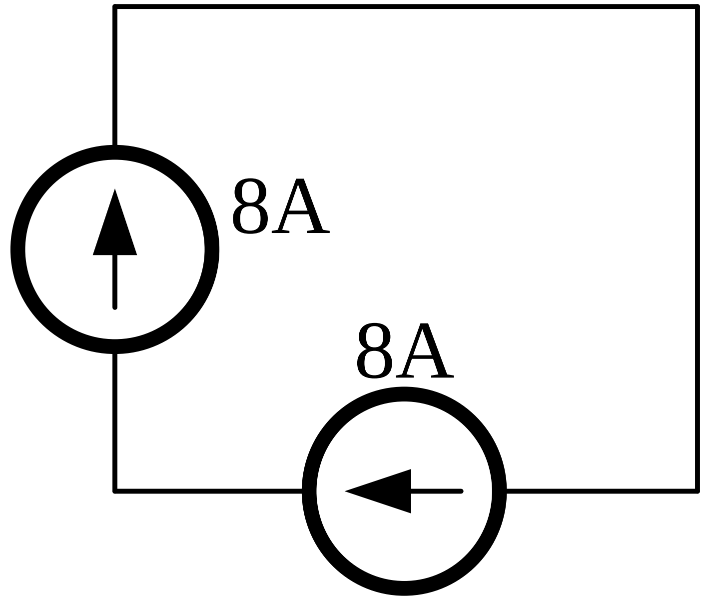
Loop IV :

$$-v_6 + v_8 = 0$$

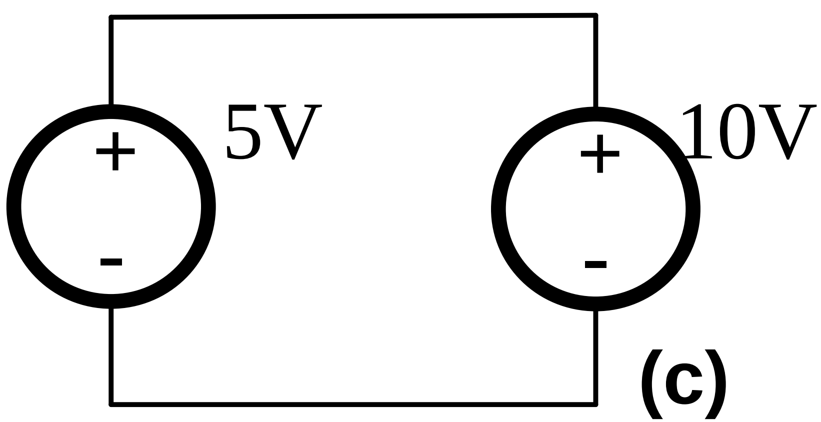
Interconnections are valid?



(a)

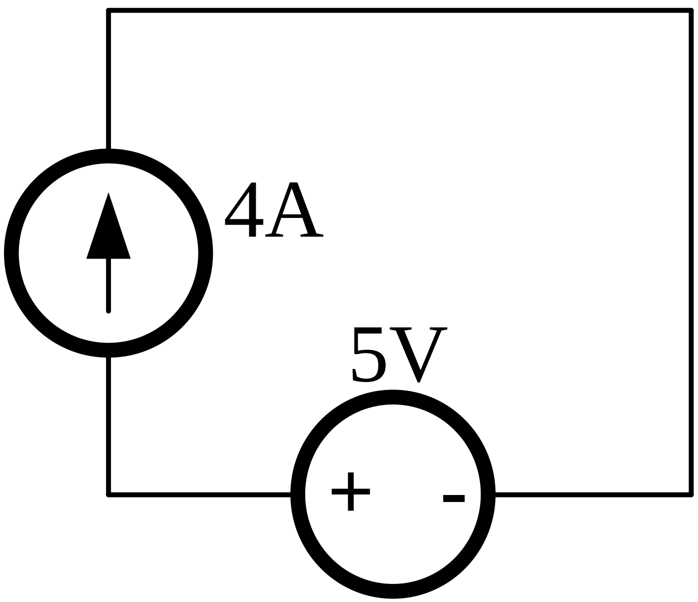


(b)

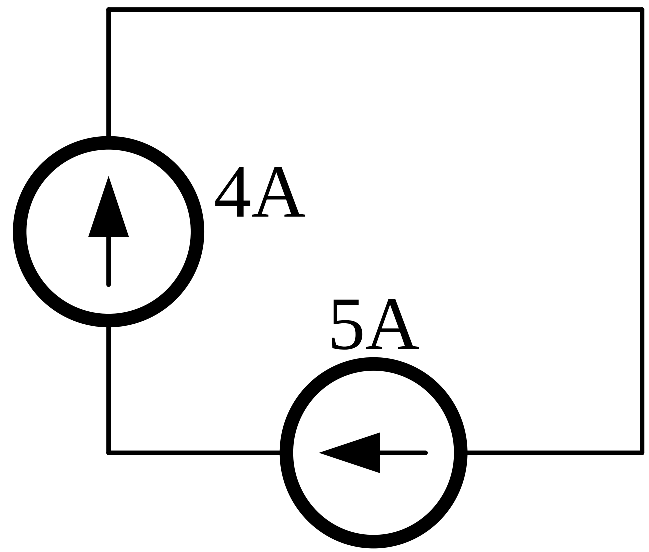


(c)

Interconnections are valid?

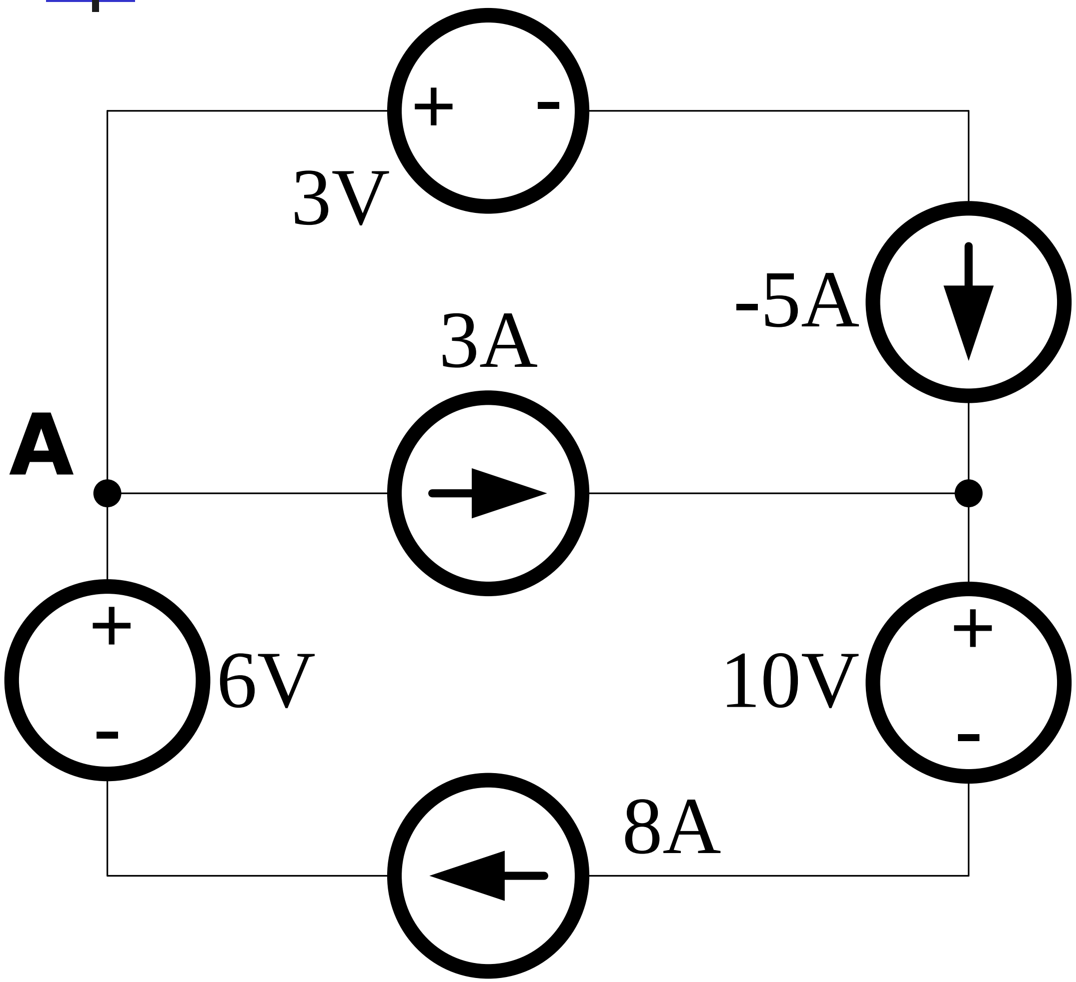


(d)



(e)

Is the interconnection valid?

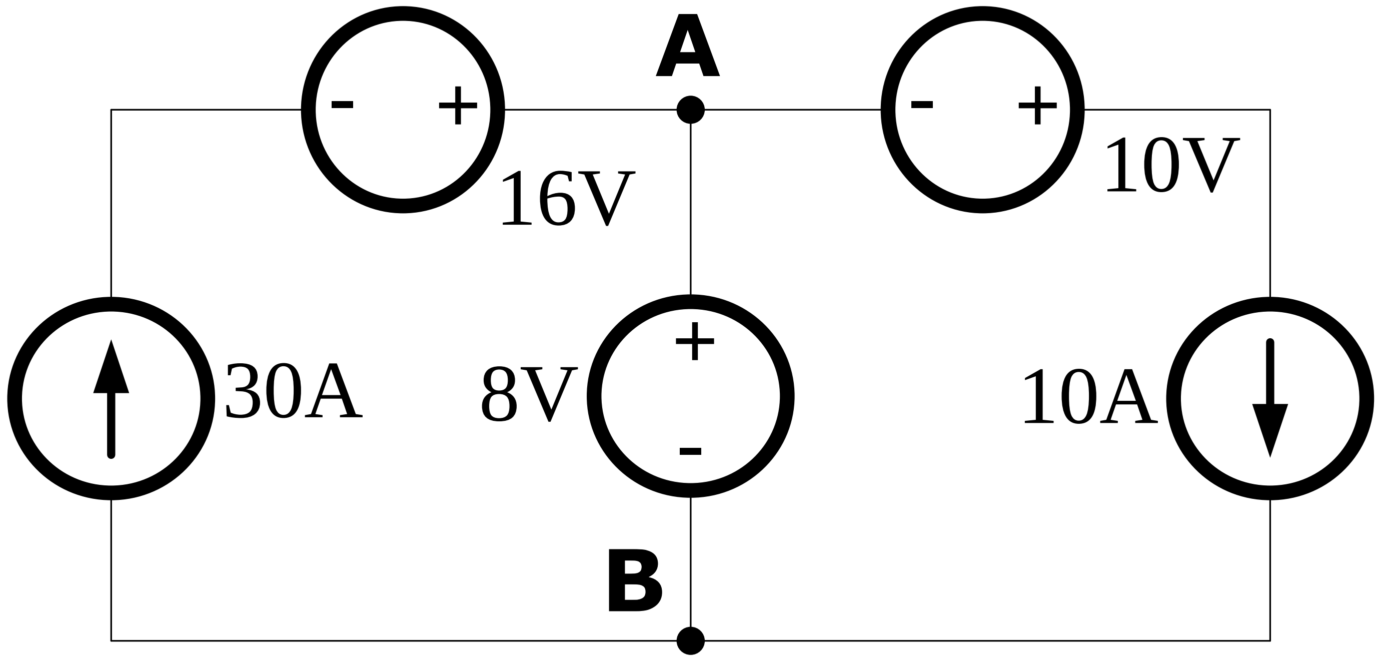


- Apply KCL for node A:

$$8 - (-5) - 3 \neq 0$$

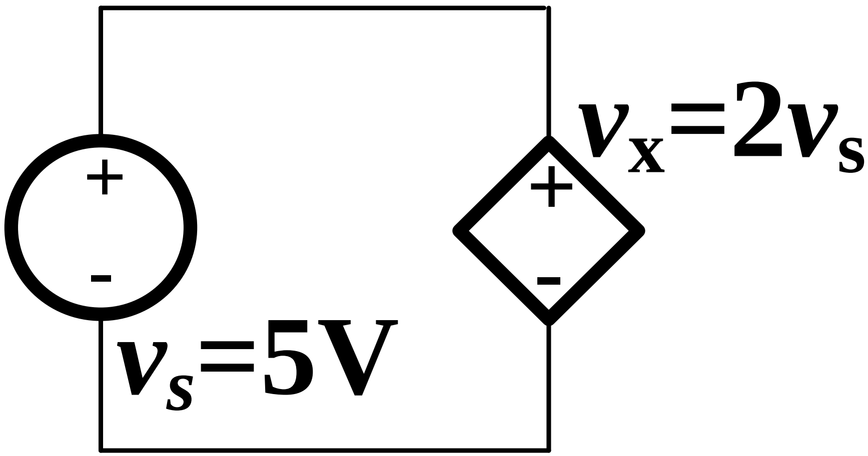
The connection is not permissible.

Is the interconnection valid?

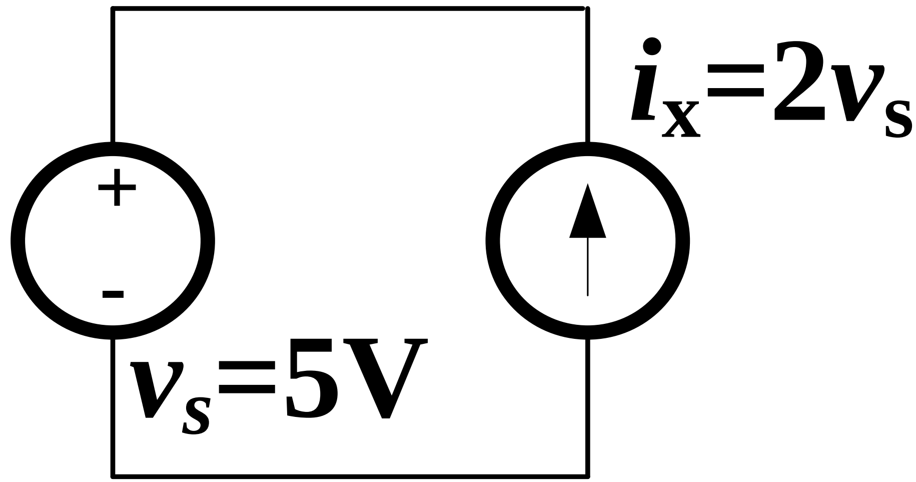


By KCL and KVL, this connection is valid.

Is the interconnection valid?

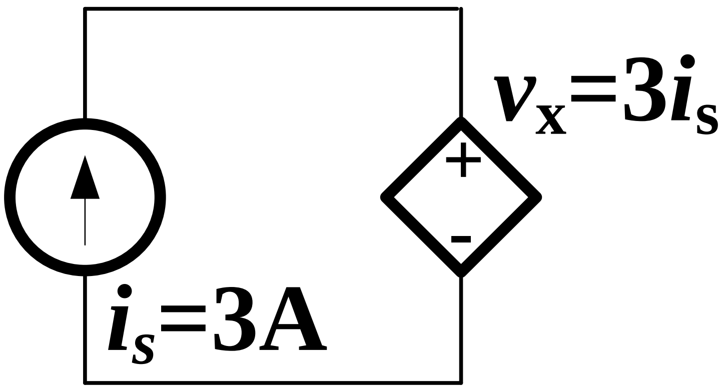


(a)

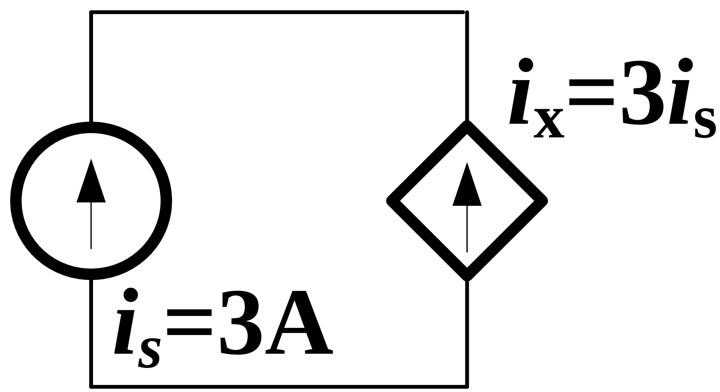


(b)

Is the interconnection valid?

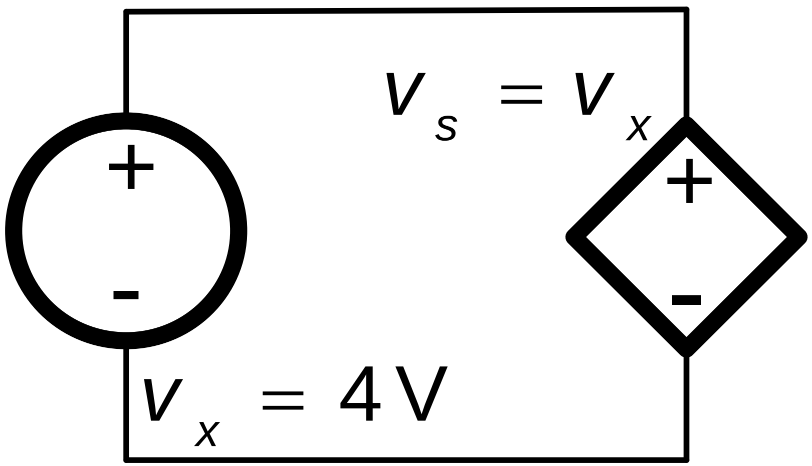


(c)

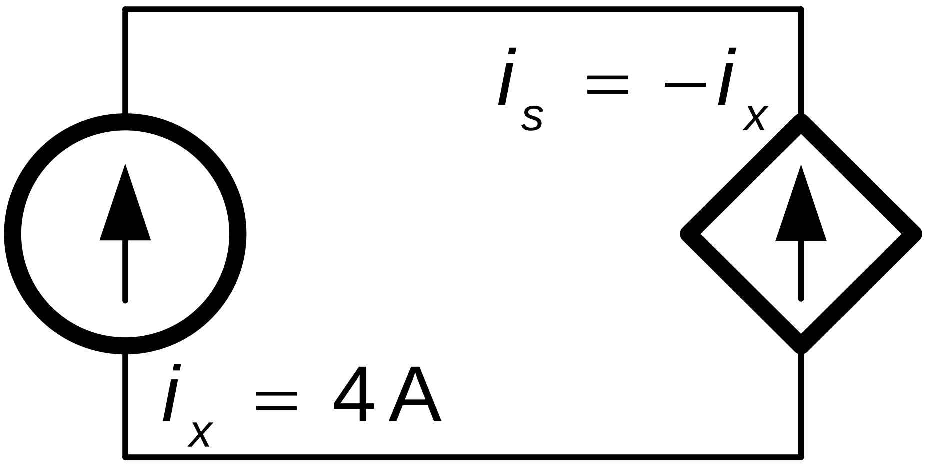


(d)

Interconnections are valid?



(e)



(f)

Topology Constraint + **Element Constraint** = **Circuit Behavior**

Topology Constraint → **KCL, KVL**

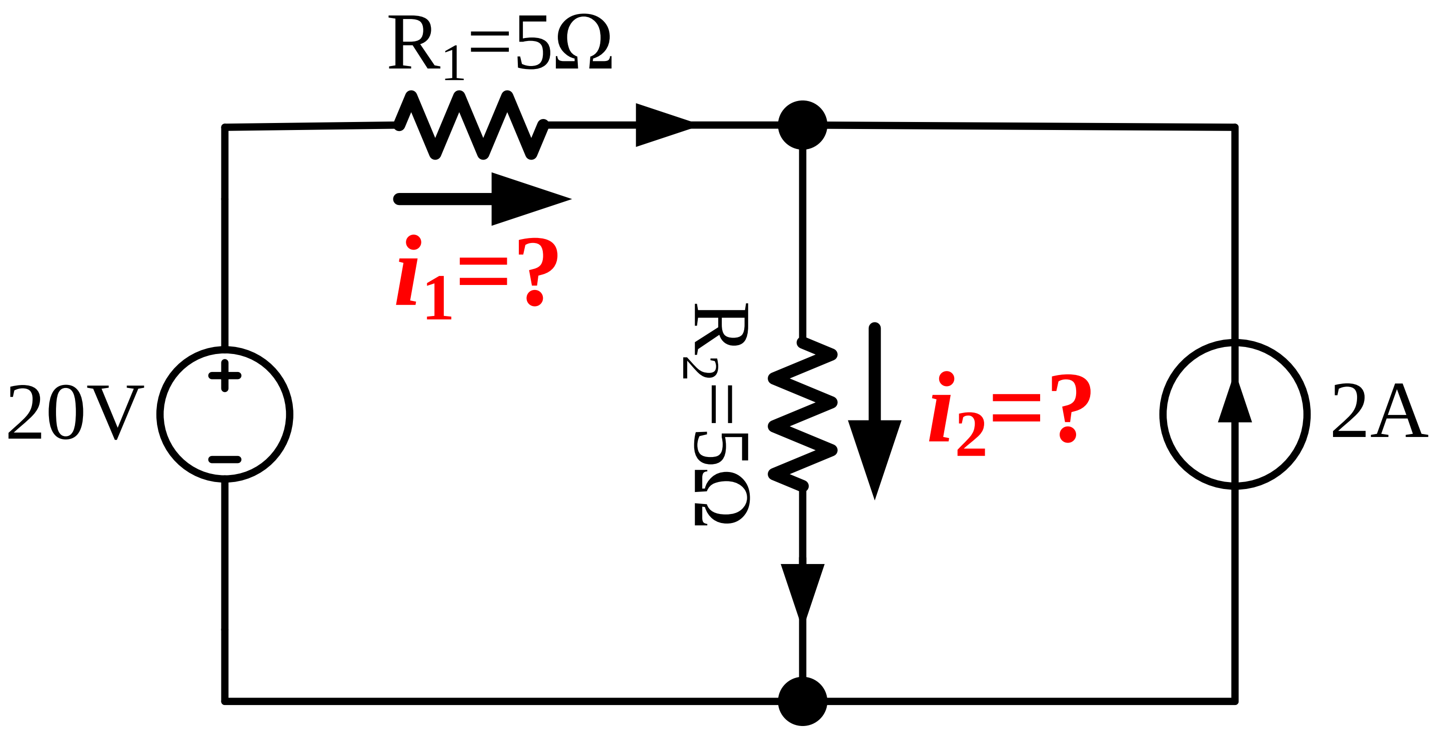
Element Constraint → **Ohm's Law*, IVS, ICS, ...**

* **For resistive elements**

Behavior of resistive circuits can be determined now by using:

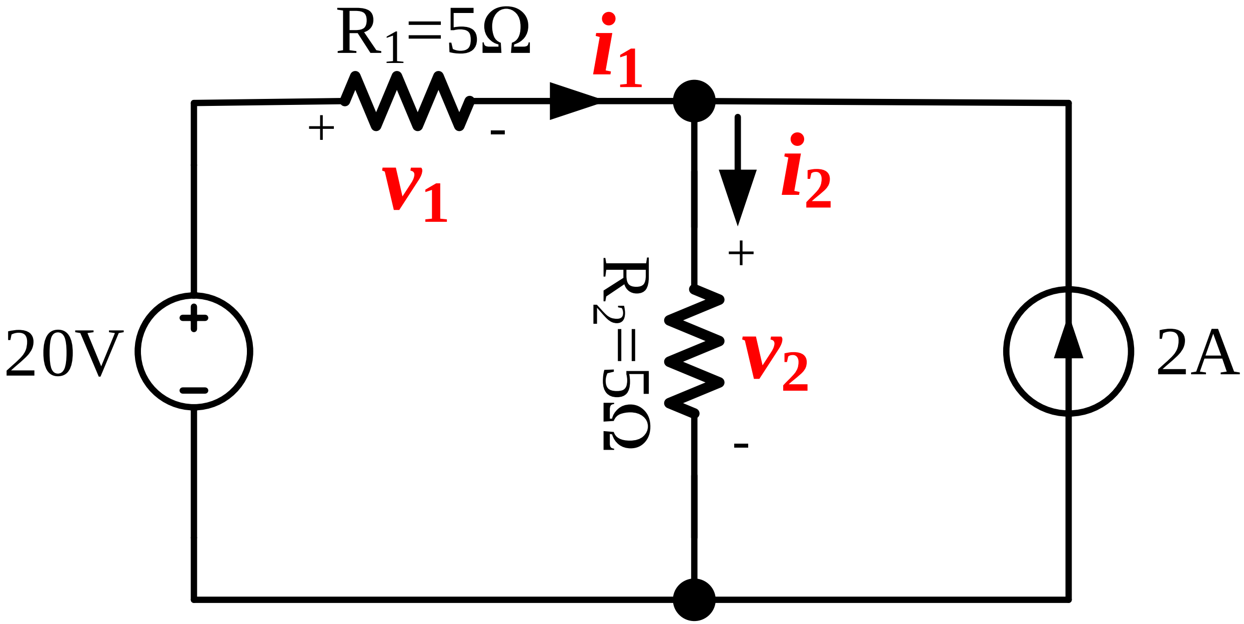
- **Element constraint --VCR for sources and resistors (Ohm's Law);**
- **Topology constraint --KCL and KVL!**

Example:

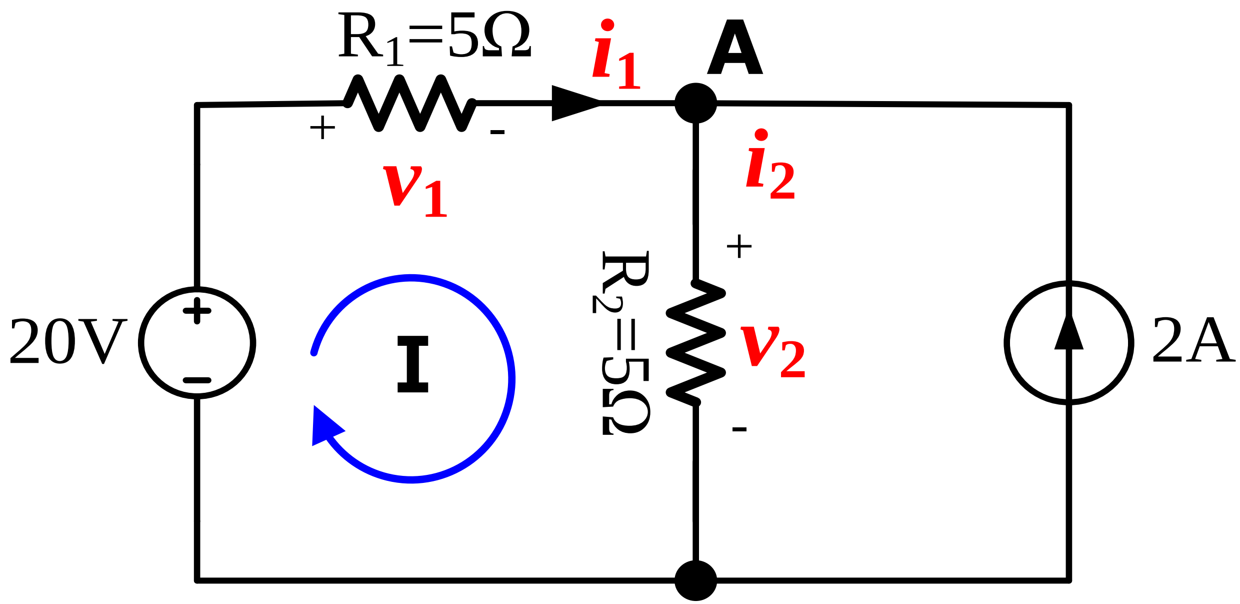


Find the value of current i_1 and i_2.

Solution:



By Ohm's law:
$$\begin{cases} v_1 = 5i_1 \\ v_2 = 5i_2 \end{cases}$$



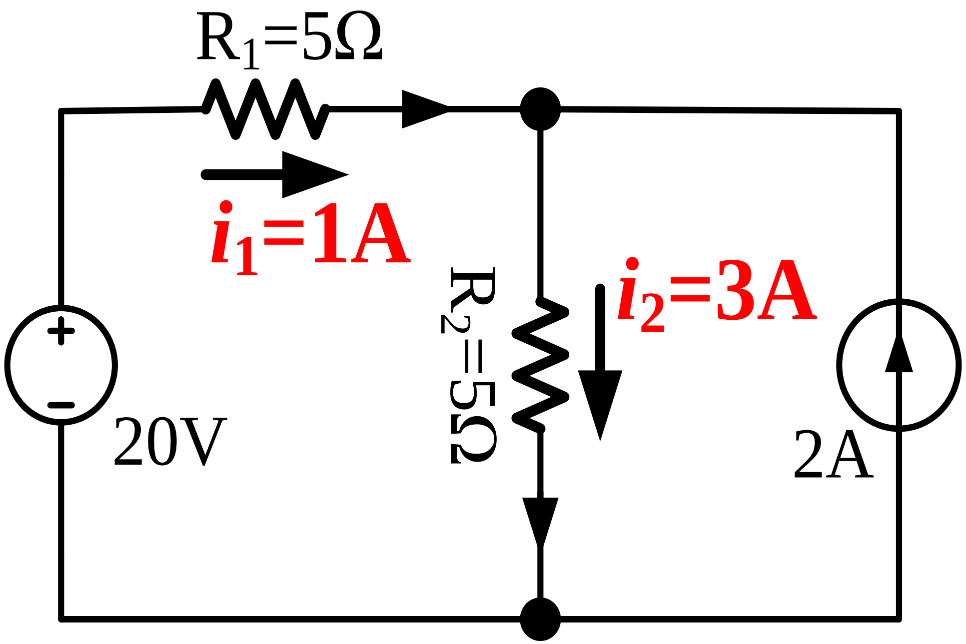
Apply KVL to loop I : $v_1 + v_2 - 20 = 0$

Apply KCL to node A: $i_1 - i_2 + 2 = 0$

Then, build a set of equations:

$$\begin{cases} v_1 = 5i_1 \\ v_2 = 5i_2 \\ i_1 - i_2 + 2 = 0 \\ v_1 + v_2 - 20 = 0 \end{cases} \Rightarrow \begin{cases} i_1 = 1\text{A} \\ i_2 = 3\text{A} \end{cases}$$

Check the answer by power balance:



$$\begin{cases} P_1 = 1^2 \times 5 = 5\text{W} \\ P_2 = 3^2 \times 5 = 45\text{W} \\ P_3 = -20 \times 1 = -20\text{W} \\ P_4 = -15 \times 2 = -30\text{W} \end{cases}$$

Check the answer by power balance:

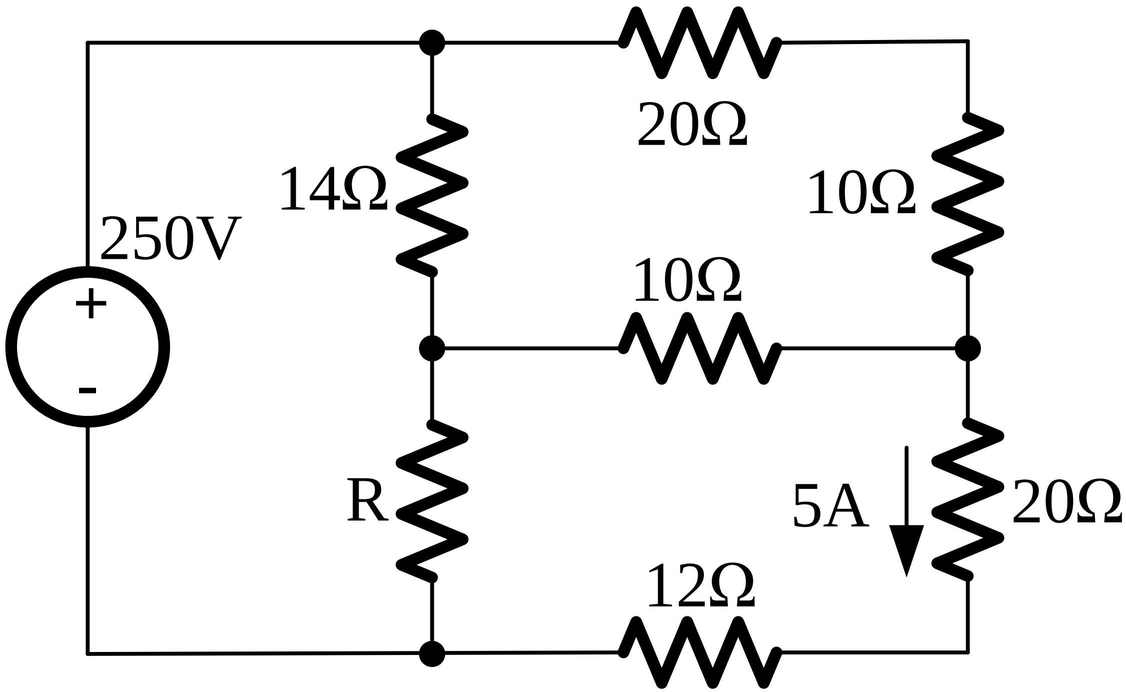
$$P_{dissipated} = P_1 + P_2 = 5 + 45 = 50\text{W}$$

$$P_{developed} = -\left(P_3 + P_4\right) = 20 + 30 = 50\text{W}$$

$$P_{dissipated} = P_{developed}$$

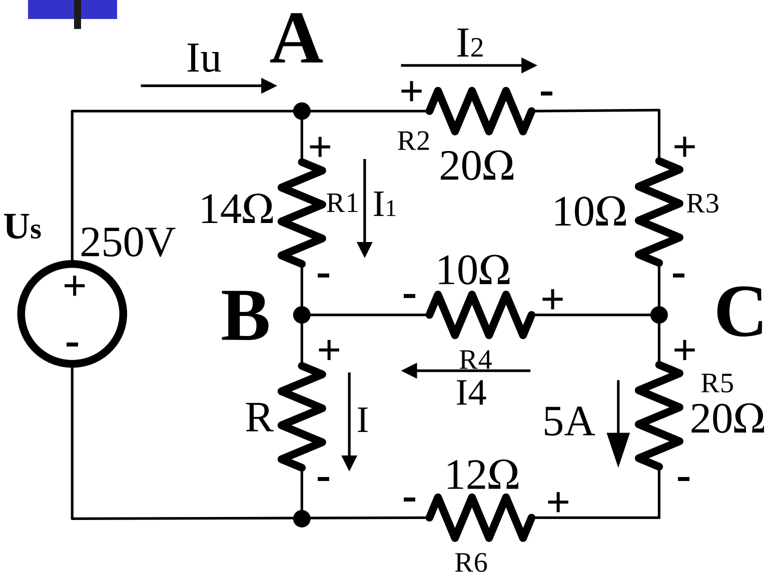
Power is balanced, and the answer is reasonable!

Example:



Find the value of R and the power supplied by the 250V voltage source.

ANS: R = 60Ω



取顺时针为绕行方向,对四个回路列写KVL方程,对节点A，B，C列写KCL方程:

$$\begin{cases} -250+14I_1+IR=0 \\ -14I_1+30I_2+10I_4=0 \\ -IR-10I_4+160=0 \\ -250+30I_2+160=0 \end{cases} \qquad \begin{cases} I_U-I_2-I_1=0 \\ I_1+I_4-I=0 \\ I_2-I_4-5=0 \end{cases}$$

解得

$I_U=8A$; $I_1=5A$; $I_2=3A$;

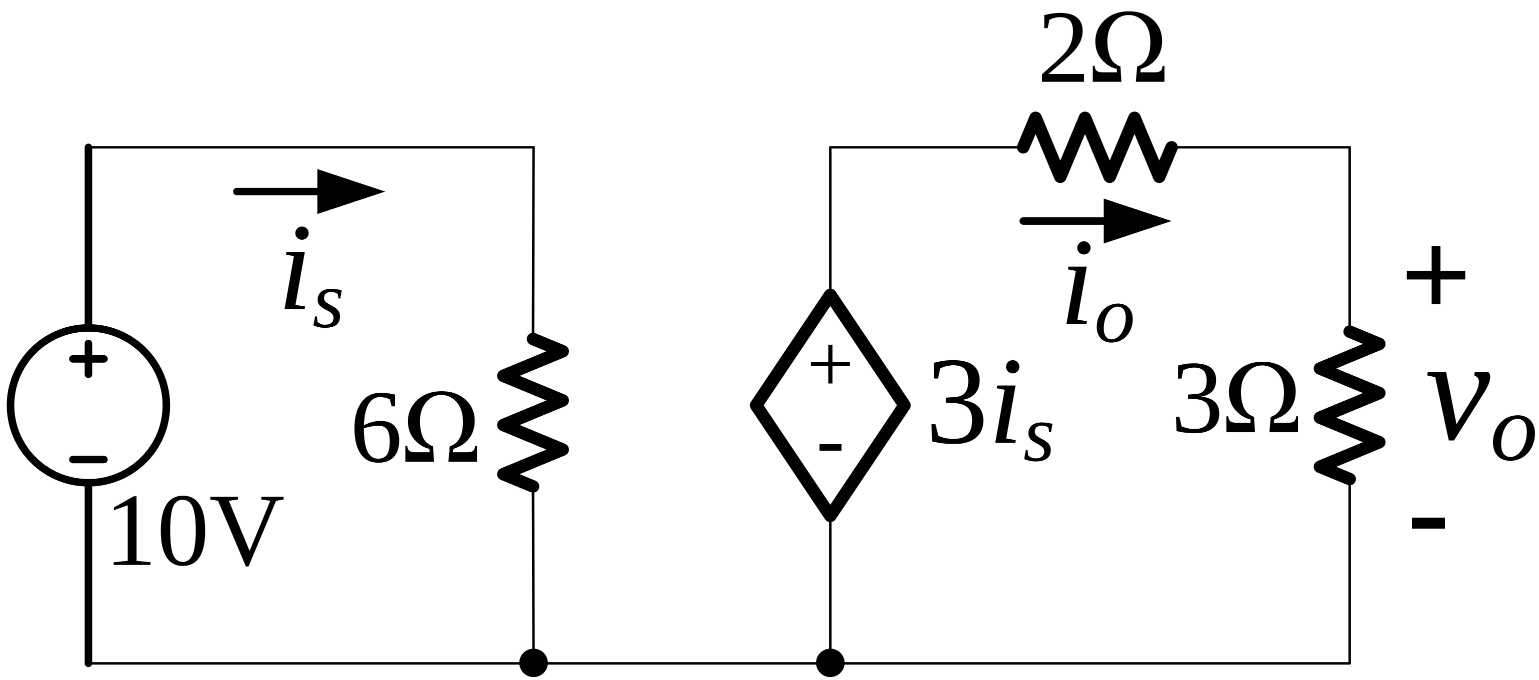
$I_4=-2A$;$I=3A$;$R=60\Omega$;

$P_u=U_s \cdot I_U=250V\times 8A=2000W$

注：R2，R3可以看做一个30Ω电阻；R5，R6可看做一个32Ω电阻以简化分析

2-2 Analysis of Simple Circuit Containing Controlled Sources

Example:



Find the value of voltage v_0 .

Solution:

By KVL, we have: $\begin{cases} 10 = 6i_s \\ 3i_s = 2i_o + 3i_o \end{cases}$

$$\Rightarrow \begin{cases} i_s = \dfrac{5}{3}\text{A} \\ i_o = 1\text{A} \end{cases} \Rightarrow v_o = 3i_o = 3\text{V}$$

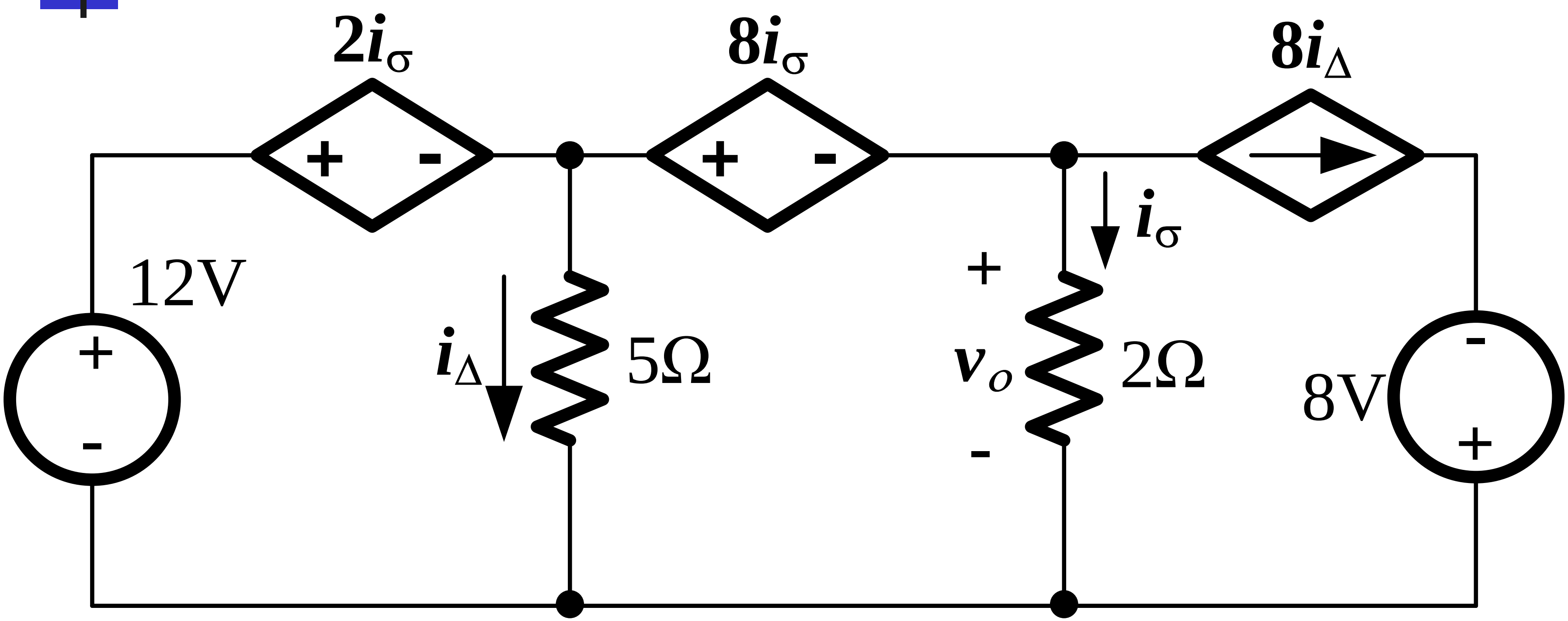
Finally, check the answer by power balance.

Check the answer by power balance:

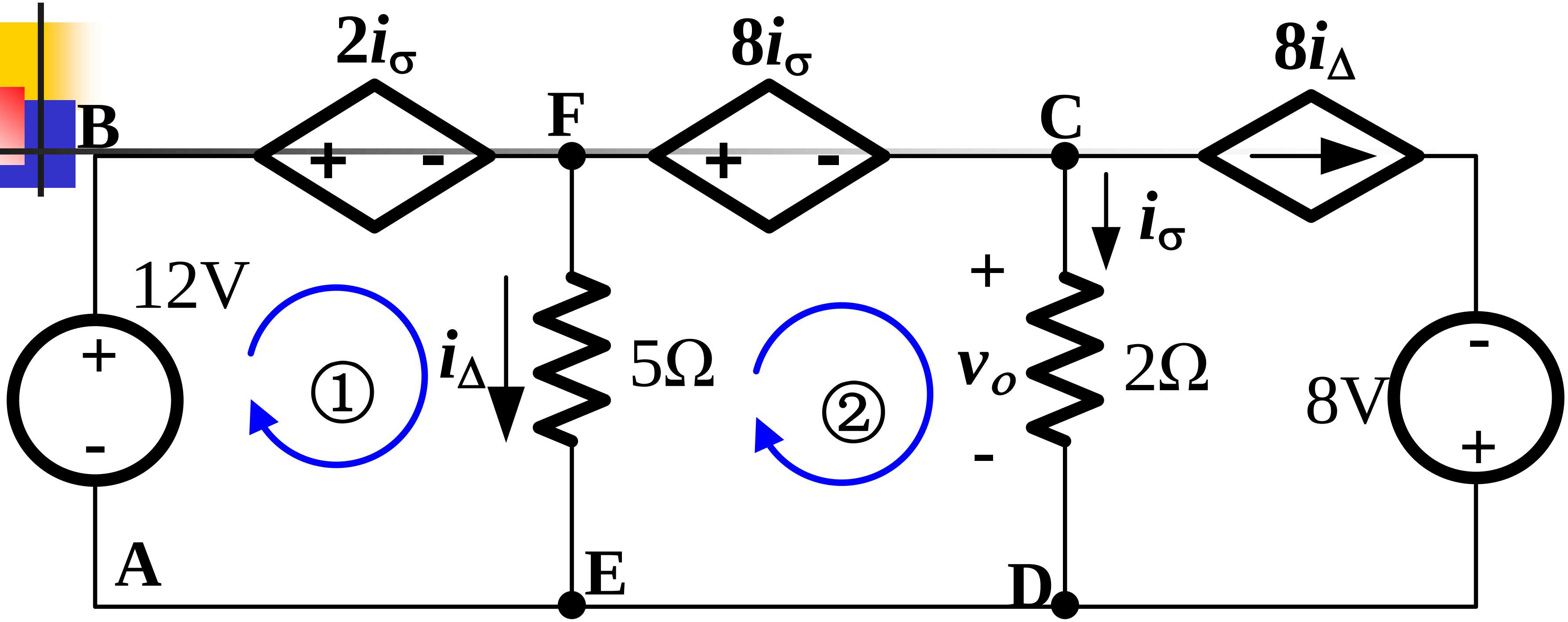
$$P_{dissipated} = P_{developed} ???$$

Example:

ANS: $i_\Delta = 2A$; $v_o = 2V$



Find the current i_Δ and voltage v_o; and show that the power developed equals the power absorbed.



对①②使用KVL方程

$$\begin{cases} 12 - 2i_\sigma - 5i_\Delta = 0 \\ 8i_\sigma + 2i_\sigma - 5i_\Delta = 0 \end{cases}$$

解得 $\begin{cases} i_\sigma = 1A \\ i_\Delta = 2A \end{cases}$ 所以 $v_0 = 2i_\sigma$=2V

总电流为: $i_\Delta + i_\sigma + 8i_\Delta = 19A$,则电压源 $p_{12V} = 19A \times 12V = 228W$,

$p_{8V} = 8i_\Delta \times 8V = 8 \times 2 \times 8 = 128W$,则电压源放出总功率356W.

其余元件吸收功率分别为:

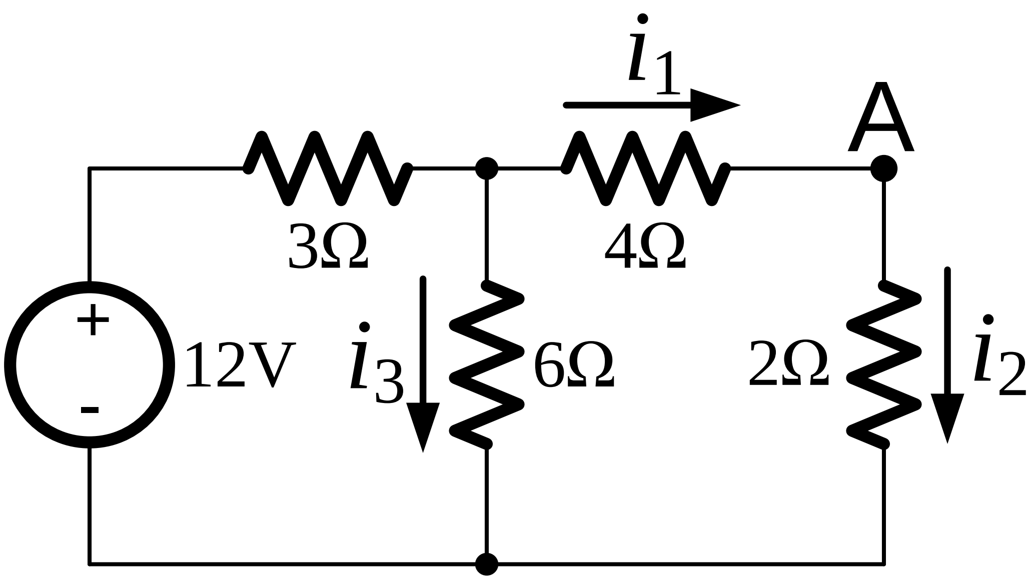
$2 \times 19 + 5 \times 2^2 + 8 \times (8 \times 2 + 1) + 2 \times 1 + 8 \times 2 \times (8 + 2)$ =356W

2-3 Resistors in Series and Parallel

- Resistors in Series
- Resistors in parallel
- Voltage and current division

Resistors in Series

In a circuit, all elements carry the **SAME** current are said to be connected in **series**.



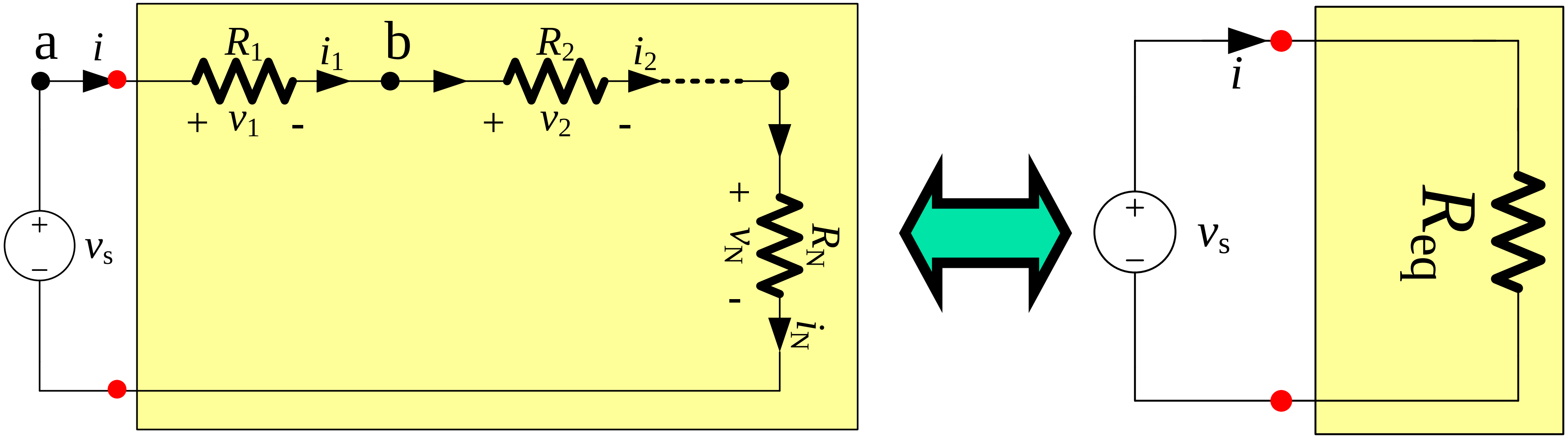
For node A, by KCL:

$$i_1 - i_2 = 0$$

Not only equal!

$$i_1 = i_2$$

Resistors in Series

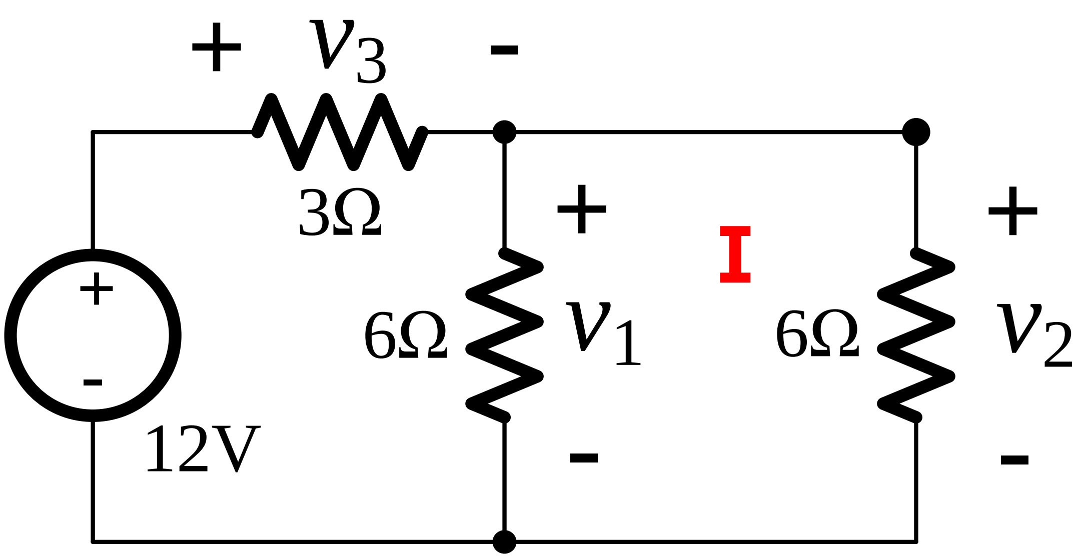


$$R_{eq} = \sum_{k=1}^{N} R_k$$

(Prove it by using KCL and KVL)

Resistors in Parallel

In a circuit, all elements have the **SAME** voltage across them are said to be connected in **parallel**.



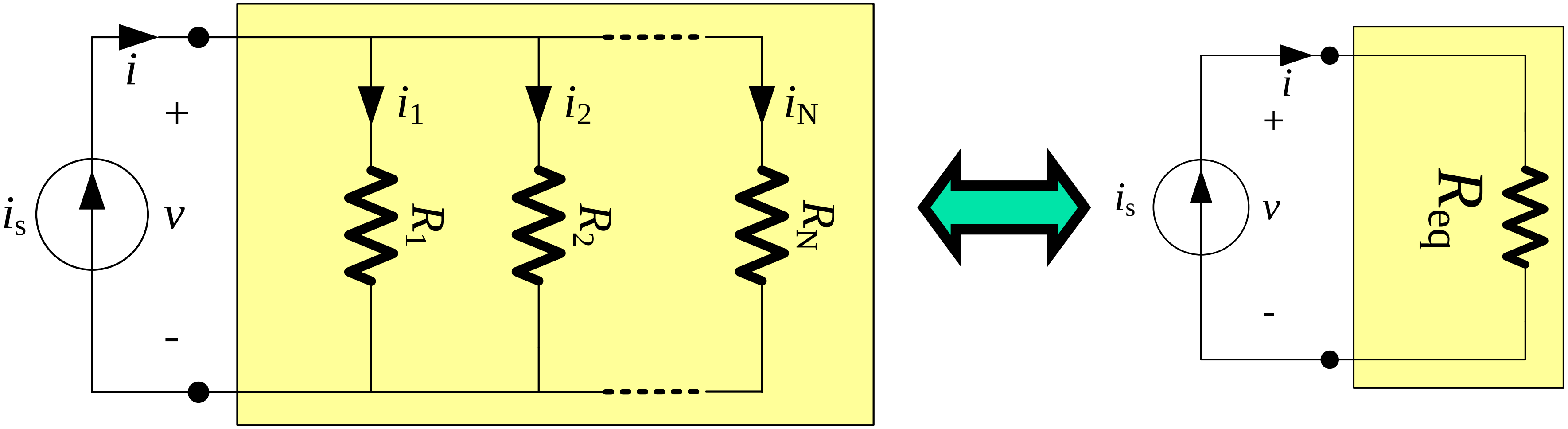
For Loop **I**, by KVL:

$-v_1 + v$

Not only equal!

$$v_1 = v_2$$

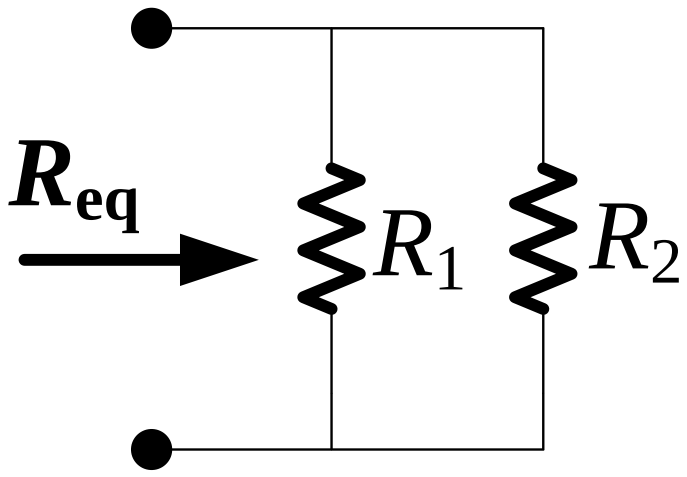
Resistors in Parallel



$$\therefore \quad \frac{1}{R_{eq}} = \sum_{k=1}^{N} \frac{1}{R_k}$$

(Prove it by using KCL and KVL)

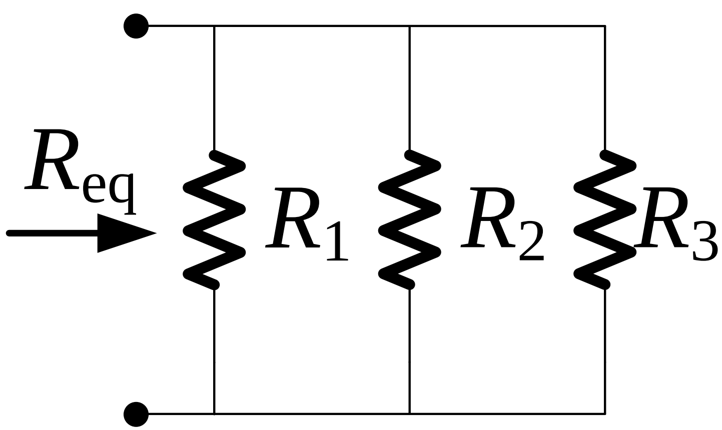
A special case:



$$R_{eq} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

A popular mistake:

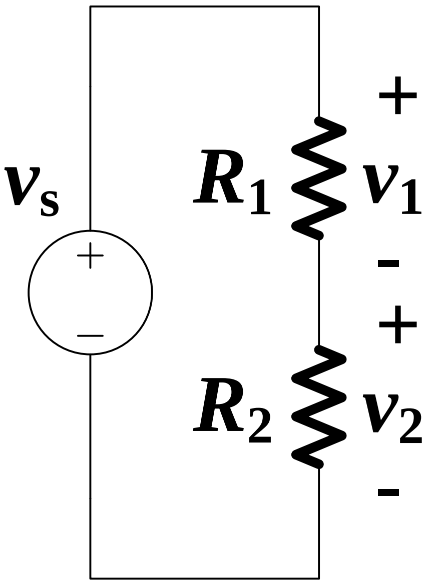
$$R_{eq} = R_1 \parallel R_2 \parallel R_3 = \cancel{\frac{R_1 R_2 R_3}{R_1 + R_2 + R_3}}$$



$$R_{eq} = R_1 \parallel R_2 \parallel R_3$$

$$= \frac{R_1 R_2 R_3}{R_1 R_2 + R_1 R_2 + R_2 R_3}$$

Voltage Division

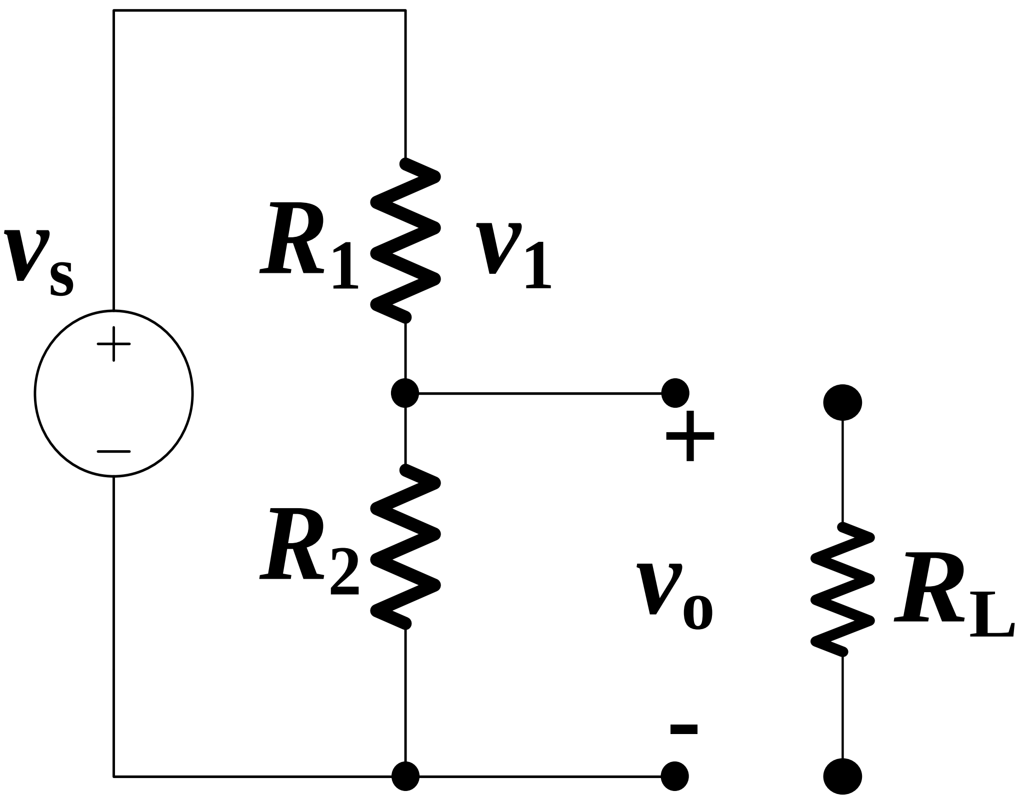


$$
\begin{cases}
v_1 = \dfrac{R_1}{R_1 + R_2} v_s \\[2ex]
v_2 = \dfrac{R_2}{R_1 + R_2} v_s
\end{cases}
$$

Generally, for *N* resistors in series:

$$v_k = \frac{R_k}{\sum_{n=1}^{N} R_n} v_s$$

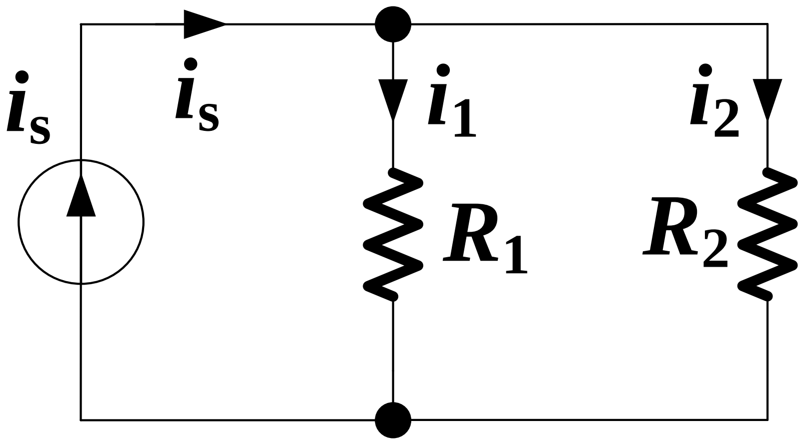
Example:



$$v_o = \frac{R_{eq}}{R_1 + R_{eq}} v_s$$

$$\left(R_{eq} = \frac{R_2 R_L}{R_2 + R_L} \right)$$

Current Division



$$\begin{cases} i_1 = \dfrac{R_2}{R_1 + R_2} i_s = \dfrac{G_1}{G_1 + G_2} i_s \\ i_2 = \dfrac{R_1}{R_1 + R_2} i_s = \dfrac{G_2}{G_1 + G_2} i_s \end{cases}$$

Generally, for *N* resistors in parallel:

$$i_k = \frac{G_k}{\sum_{n=1}^{N} G_n} i_s$$

Summary of Chapter 2

- Ohm's Law with and w/o PSC
- Node, Loop, Mesh, ……
- **KCL and KVL**
- Simple circuits analysis containing CS
- Resistors in Series and in Parallel

Primary Goals of Chapter 2

In this chapter, we seek to develop our:

- **Ability to implement Ohm's Law;**
- **Ability to use Kirchhoff's Laws (KCL & KVL);**
- **Skills in analyzing simple circuits containing dependent sources.**