When modeling, you need to be asking yourself some fundamental questions:

1. Why are you modeling?

1. To determine the feasibility of a new architecture (interconnect)?
2. To understand timing issues?
3. To create a golden standard against which to RTL development?
4. To allow firmware development to start early?
5. To share with an external customer?
6. To use synthesis tools?

2. What is the focus of the model?

1. A single component
2. An entire system
3. Interoperability with another system
4. Post silicon validation

3. Who is your customer, and what do they need?

1. Architect
2. Verification team
3. Firmware team
4. Validation team

4. How "configurable" will the model be?

1. Limited
2. Allow different timing models/mixes
3. Support different teams
4. Support different connectivities

5. Are there simulation performance goals?

1. The more details you add, the slower the simulation
2. With fewer details, accuracy may be impacted
3. What is reasonable it required?

6. How much development time do you have for the model?

1. How much validation is needed?
2. How does it impact others' schedules?
3. How long do you expect this model to be used?
4. How much time do you have?
5. Can you acquire parts of the model from the teams or externally?
6. Can you purchase parts of the model?

Answers to the above questions will drive your decisions.

TLM的b\_transport和nb\_tranport传输方法带的sc\_time参数都只是时间标注，不会做实际的delay，实际的delay需要在绑定的回调函数里面调用wait(delay\_time)、peq管道等延时方法