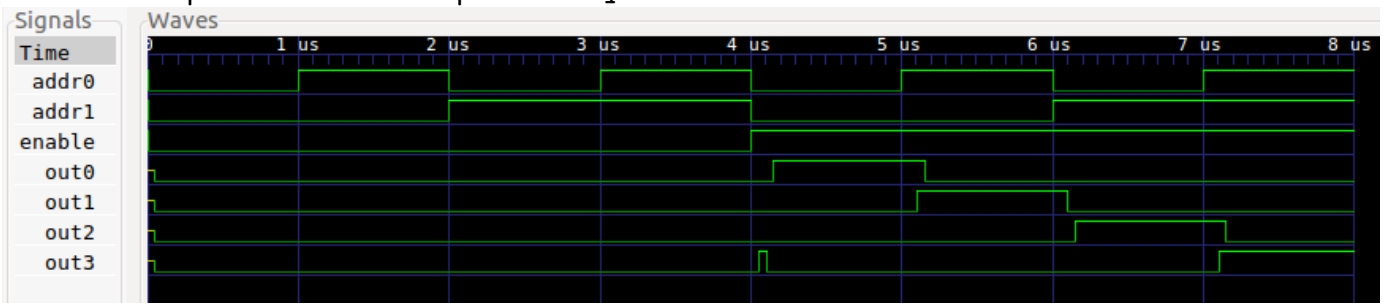
Taylor Sheneman
Computer Architecture - HW2

## Decoder

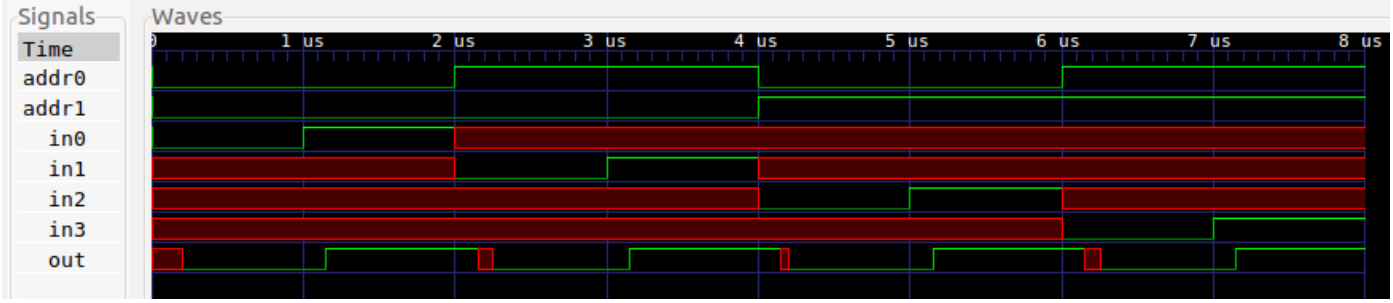
| En | A0 | A1 | O0 | O1 | O2 | O3 | Expected Output |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | All false |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | All false |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | All false |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | All false |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | O0 Only |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | O1 Only |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | O2 Only |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | O3 Only |




As expected, the only output trace set high in each test is the number encoded in the binary input address bits.

## Multiplexer

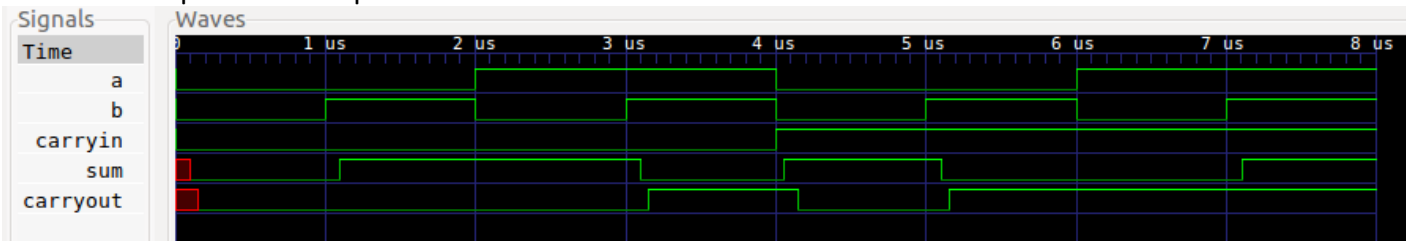
| i0 | i1 | i2 | i3 | A0 | A1 | out | Expected Output |
|---|---|---|---|---|---|---|---|
| 0 | x | x | x | 0 | 0 | 0 | False |
| 1 | x | x | x | 0 | 0 | 1 | True |
| x | 0 | x | x | 1 | 0 | 0 | False |
| x | 1 | x | x | 1 | 0 | 1 | True |
| x | x | 0 | x | 0 | 1 | 0 | False |
| x | x | 1 | x | 0 | 1 | 1 | True |
| x | x | x | 0 | 1 | 1 | 0 | False |
| x | x | x | 1 | 1 | 1 | 1 | True |




Only the input whose address is encoded in the address bits is passed through to the output; all other inputs are undefined, with no effect on the steady state of the output trace.

# 1-Bit Full Adder

| Ci | A | B | sum | Co | Expected Output | |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |




A single high input results in sum=1, carryout=0
Two high inputs result in sum=0, carryout=1
The single case of three inputs results in sum=1, carryout=1