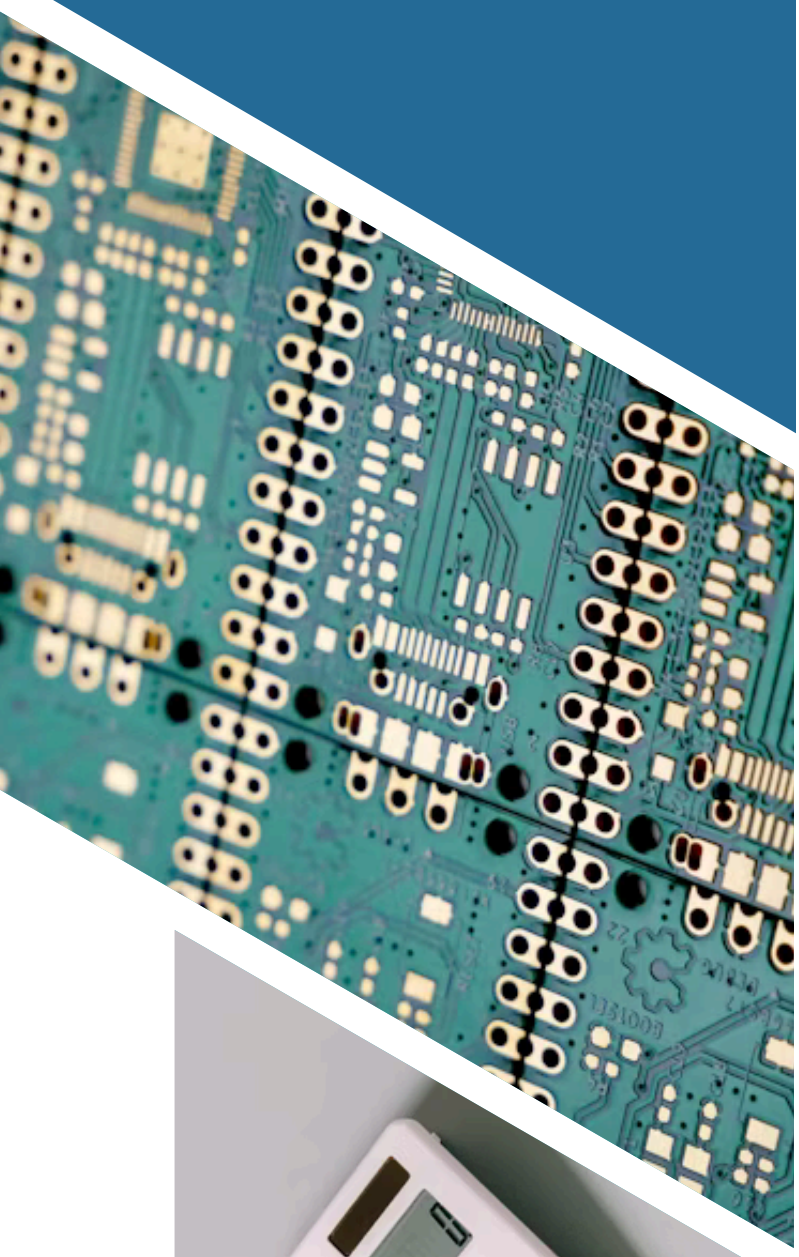
LOGIC DESIGN



4-BIT CALCULATOR

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HAMDI EMAD HAMDI

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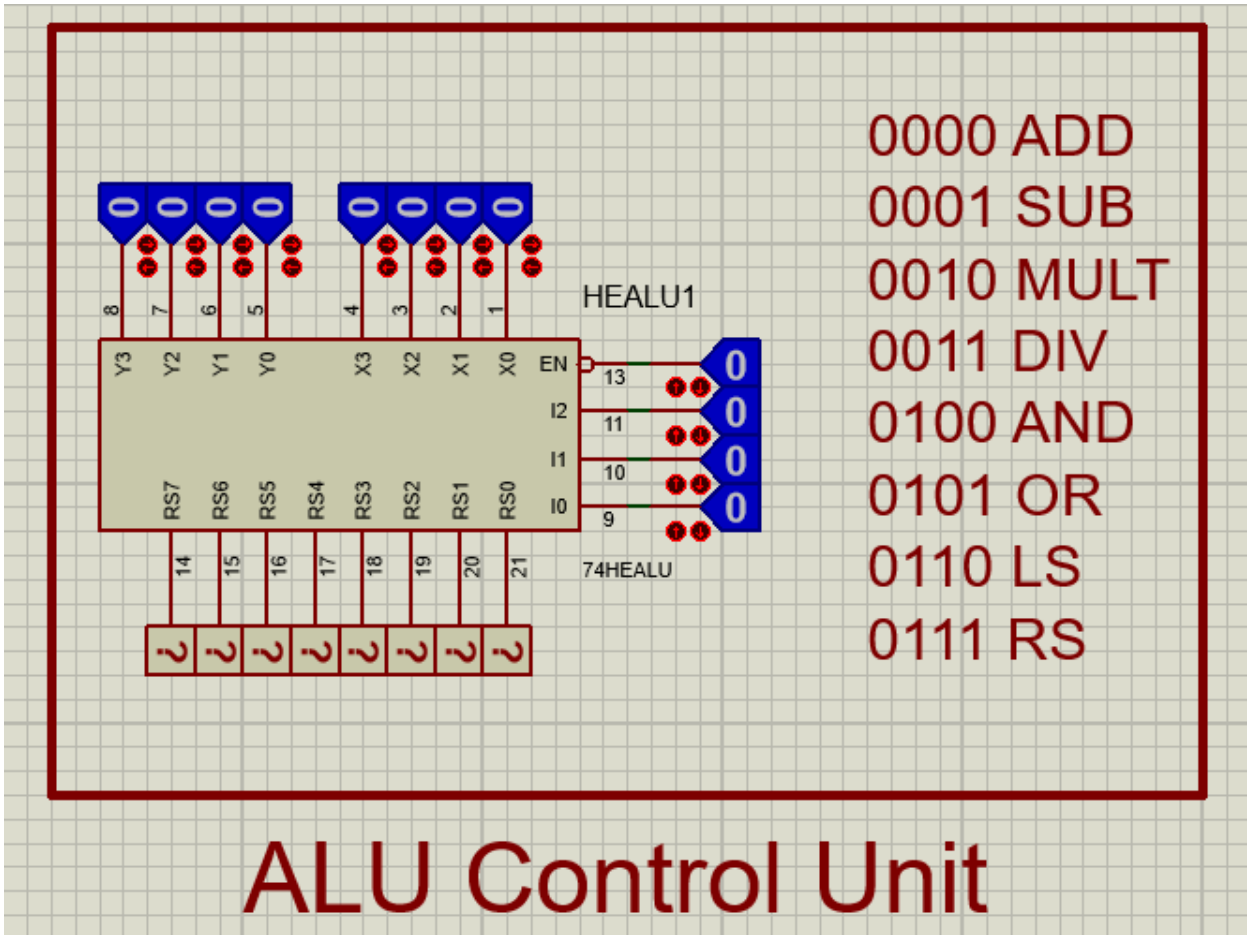
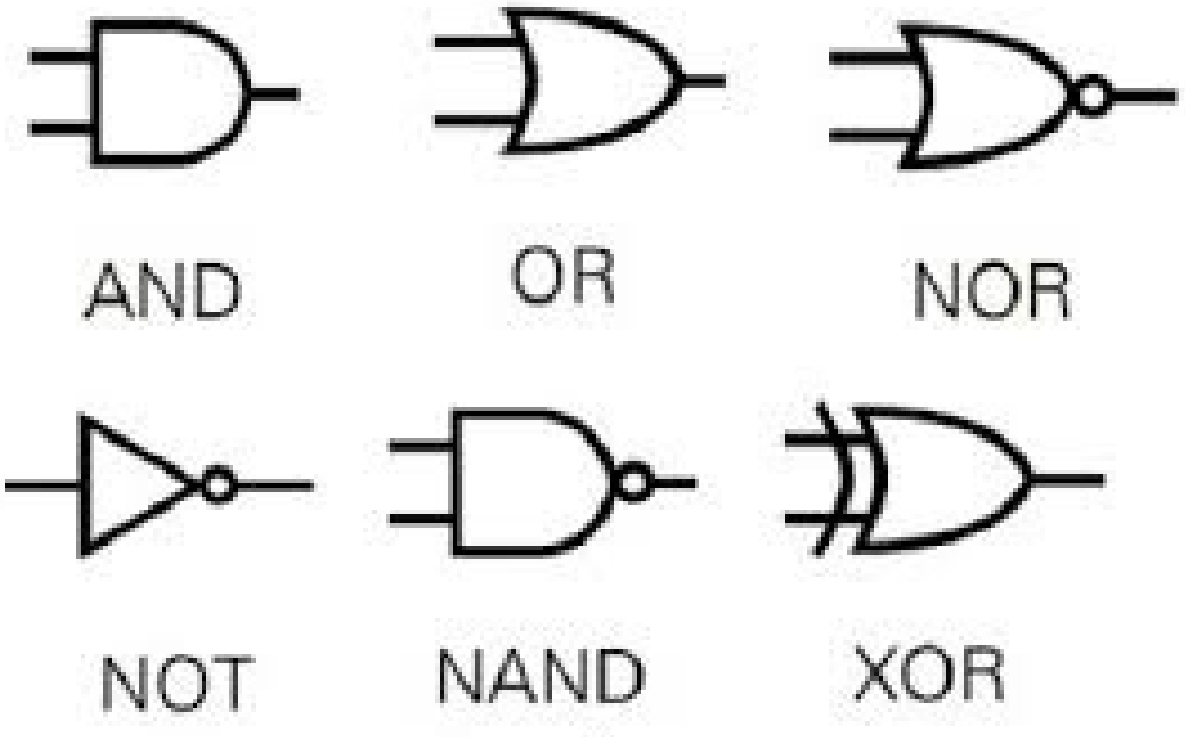
Introduction

This report outlines the development of a 4-bit calculator using fundamental logic gates, including AND, OR, NOT, XOR, NAND, and NOR. The system performs eight arithmetic and logic operations on 4-bit binary numbers. This project emphasizes understanding combinational logic, truth tables, and circuit-level design without using any hardware description language.



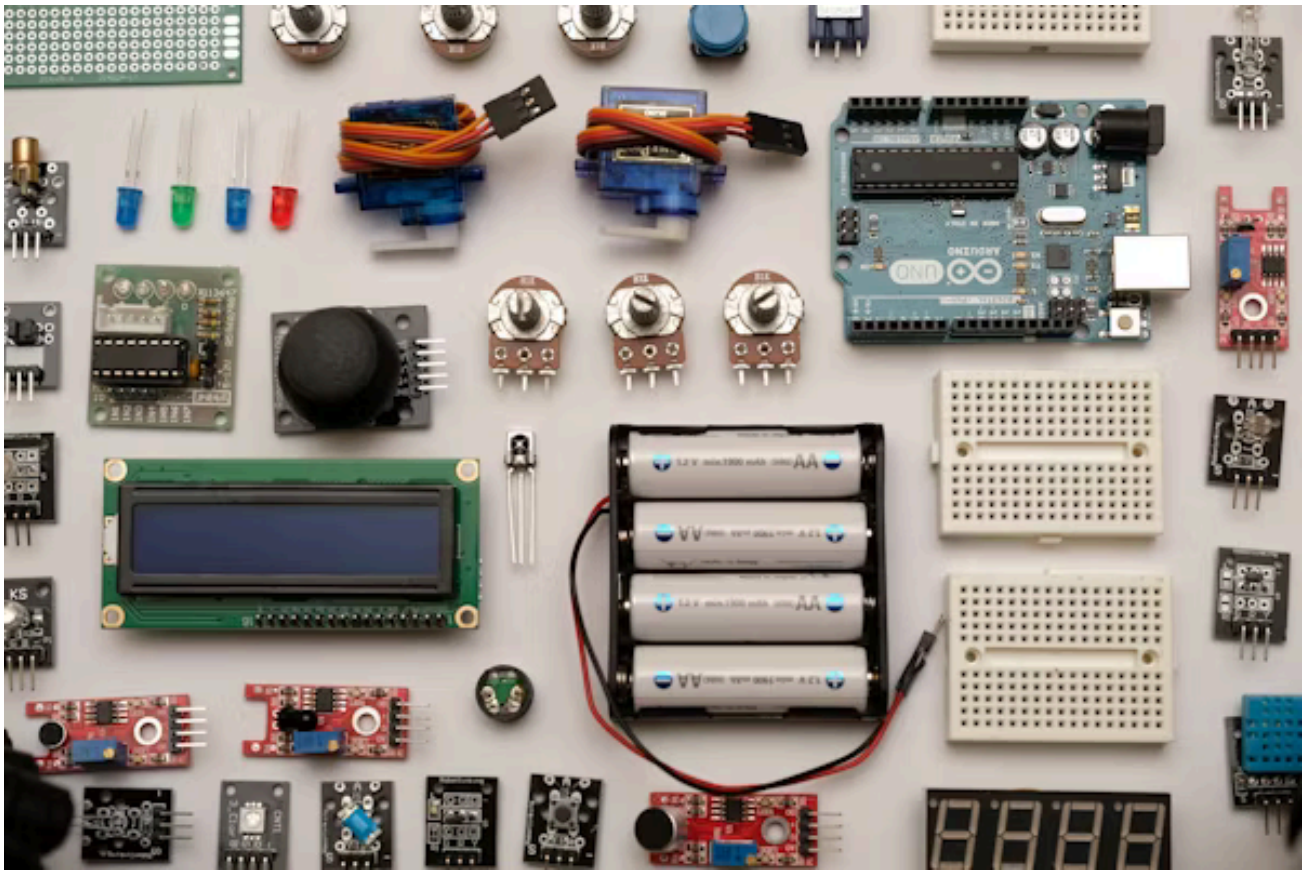
Project Objectives

- **To implement a 4-bit ALU from scratch using logic gates.**
- **To realize 8 operations: ADD, SUB, MULT, DIV, AND, OR, LS, and RS.**
- **To assemble a physical calculator circuit using ICs or on a breadboard.**
- **To develop a modular and reusable digital design.**
- **To enhance practical skills in digital electronics.**



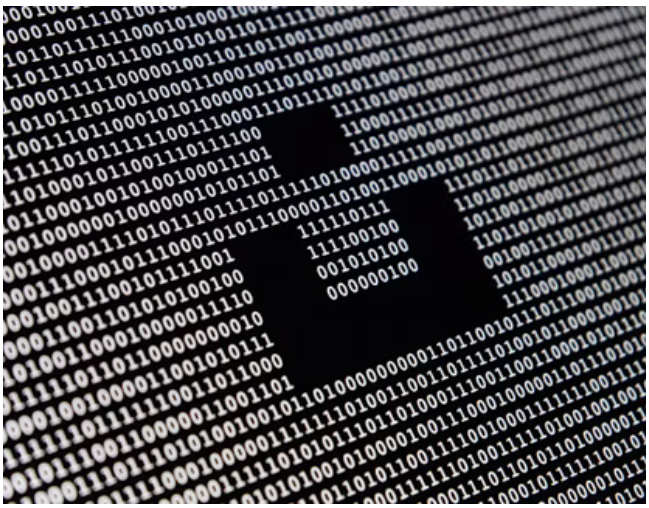
Tools and Materials Used

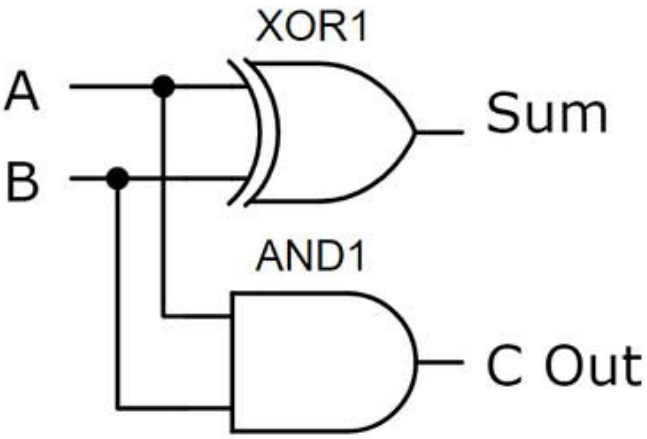
- Logic ICs (e.g., 74125, 7408, 7432, 7486, 74238)
- Breadboard
- Connecting wires and resistors
- Power supply (5V regulated)
- Toggle switches for inputs
- LEDs or 7-segment display for outputs
- Multimeter and logic probe for testing



Theoretical Background

- Boolean algebra and logic gate operations
- Binary number system and arithmetic
- Half adder and full adder logic
- Bit-wise logic operations
- Control signal decoding via combinational logic

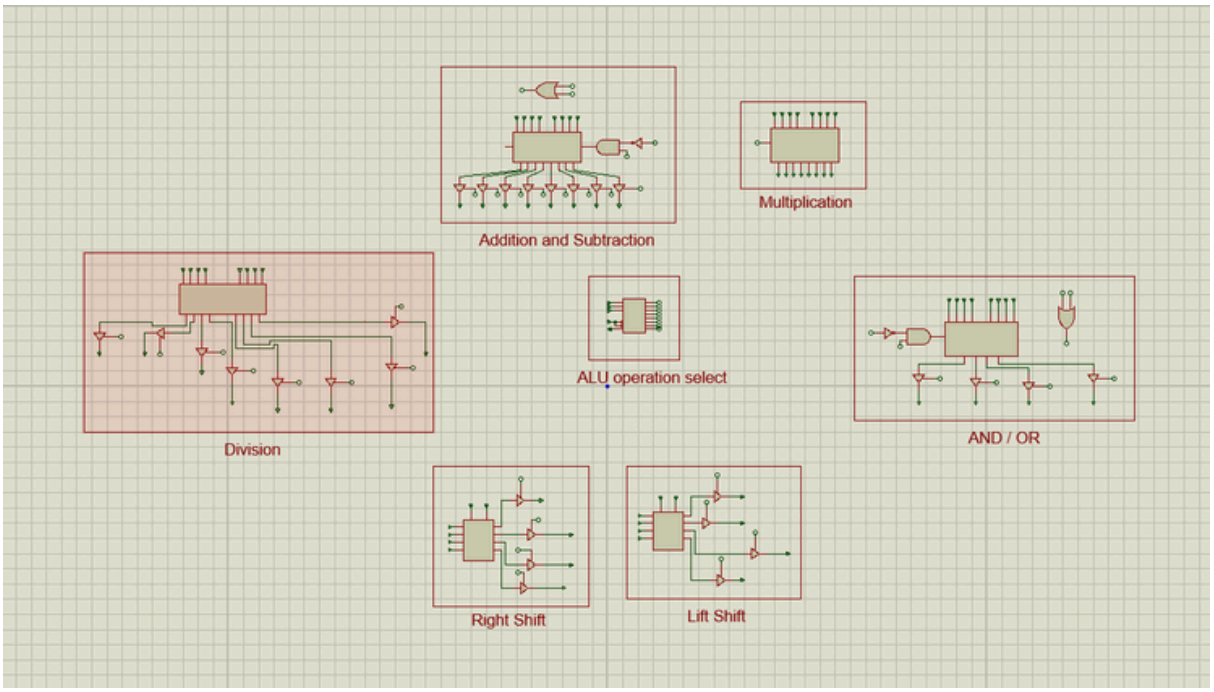




System Truth table

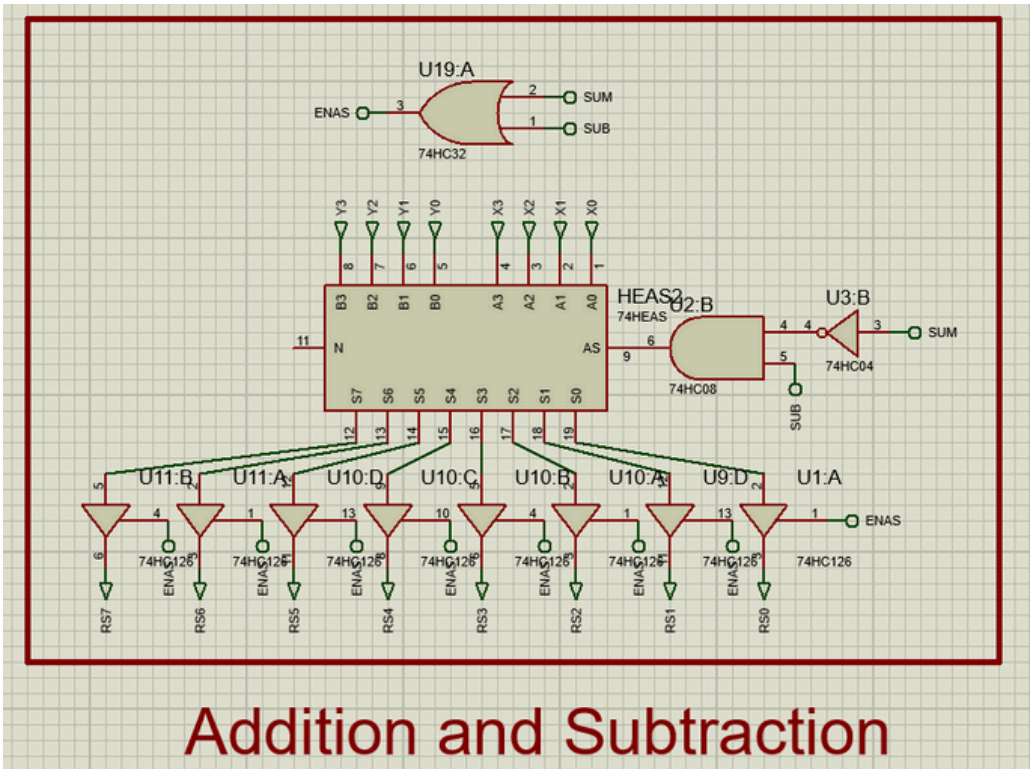
Opcode	Operation	Function	Description
0000	ADD	A + B	Addition of inputs A and B
0001	SUB	A - B	Subtraction (A minus B)
0010	MULT	A × B	Multiplication of A and B
0011	DIV	A ÷ B	Division (A divided by B)
0100	AND	A & B	Bitwise AND operation
0101	OR	A | B	Bitwise OR operation
0110	LS	A << n	Left Shift operation
0111	RS	A >> n	Right Shift operation

Circuit Schematics



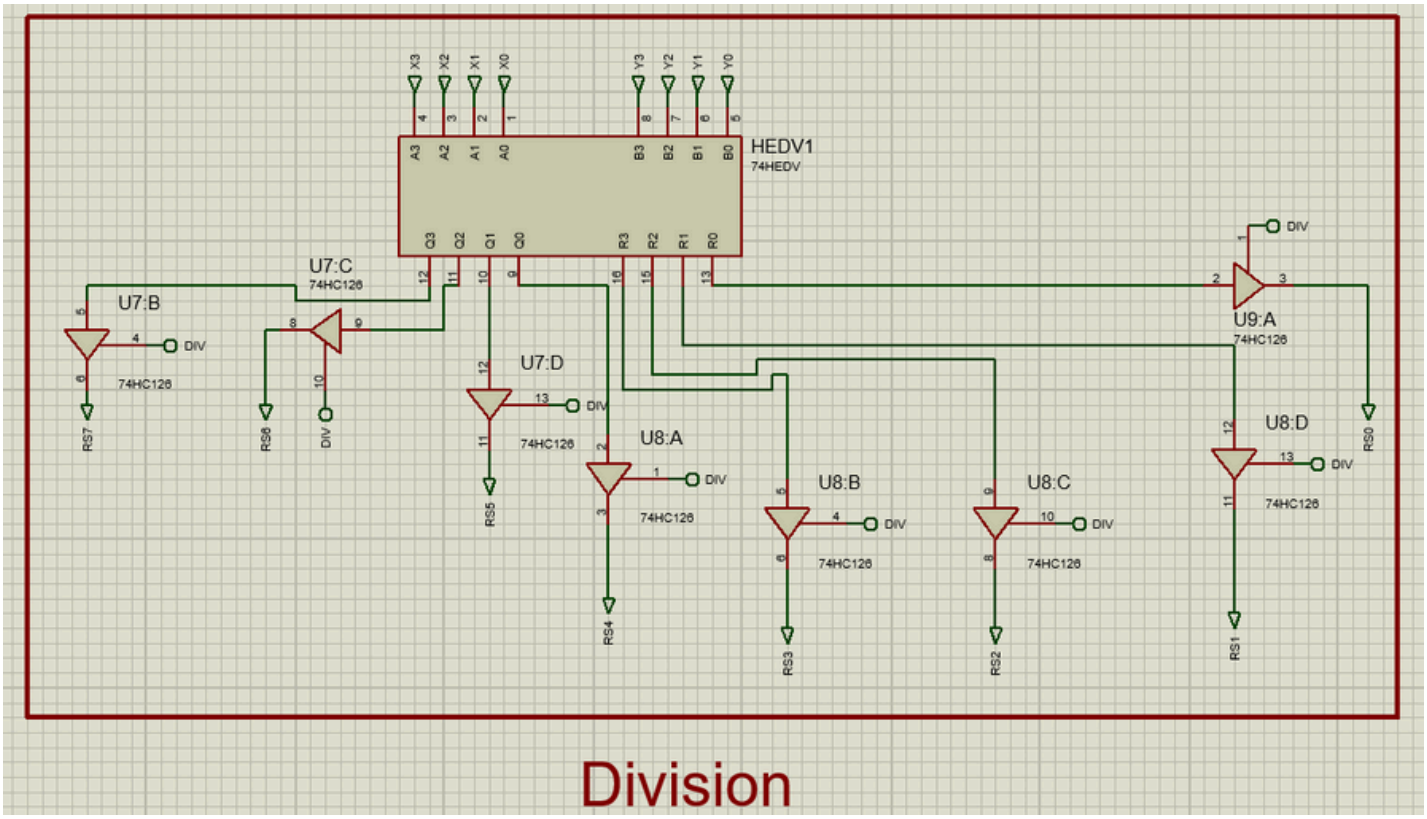
Truth Tables and Logic Diagrams

1- Addition & Subtraction



ENAS	SUB	SUM	Operation	Function	Output Enable
0	X	X	Disabled	High-Z	Disabled
1	0	1	Addition	A + B	Enabled
1	1	0	Subtraction	A - B	Enabled

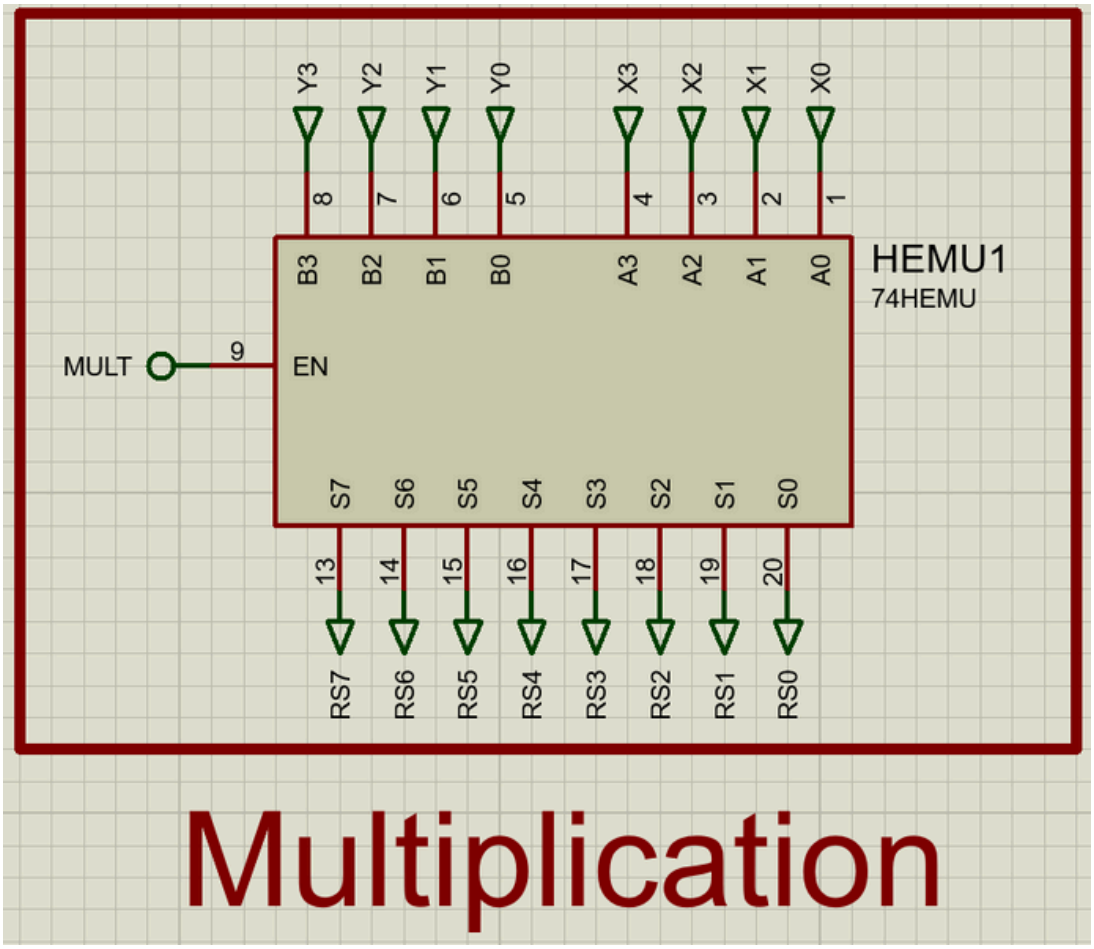
2- Division



Division

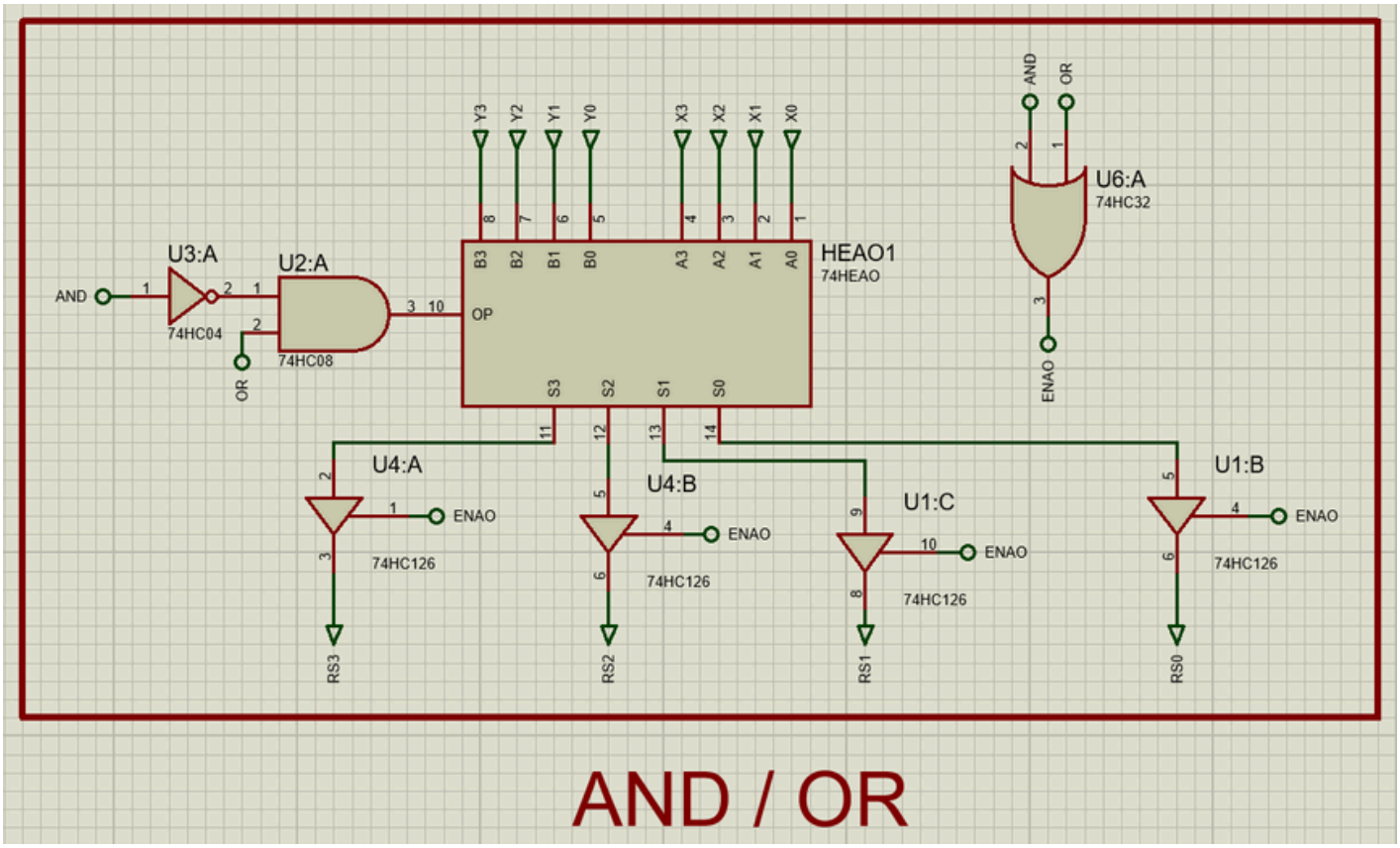
Signal Group	Pins	Function	Description
X3-X0	4-bit	Dividend	The number to be divided
Y3-Y0	4-bit	Divisor	The number to divide by
RS3-RS0	4-bit	Control	Register select/enable signals
DIV	1-bit	Enable	Division operation enable

3- Multiplication



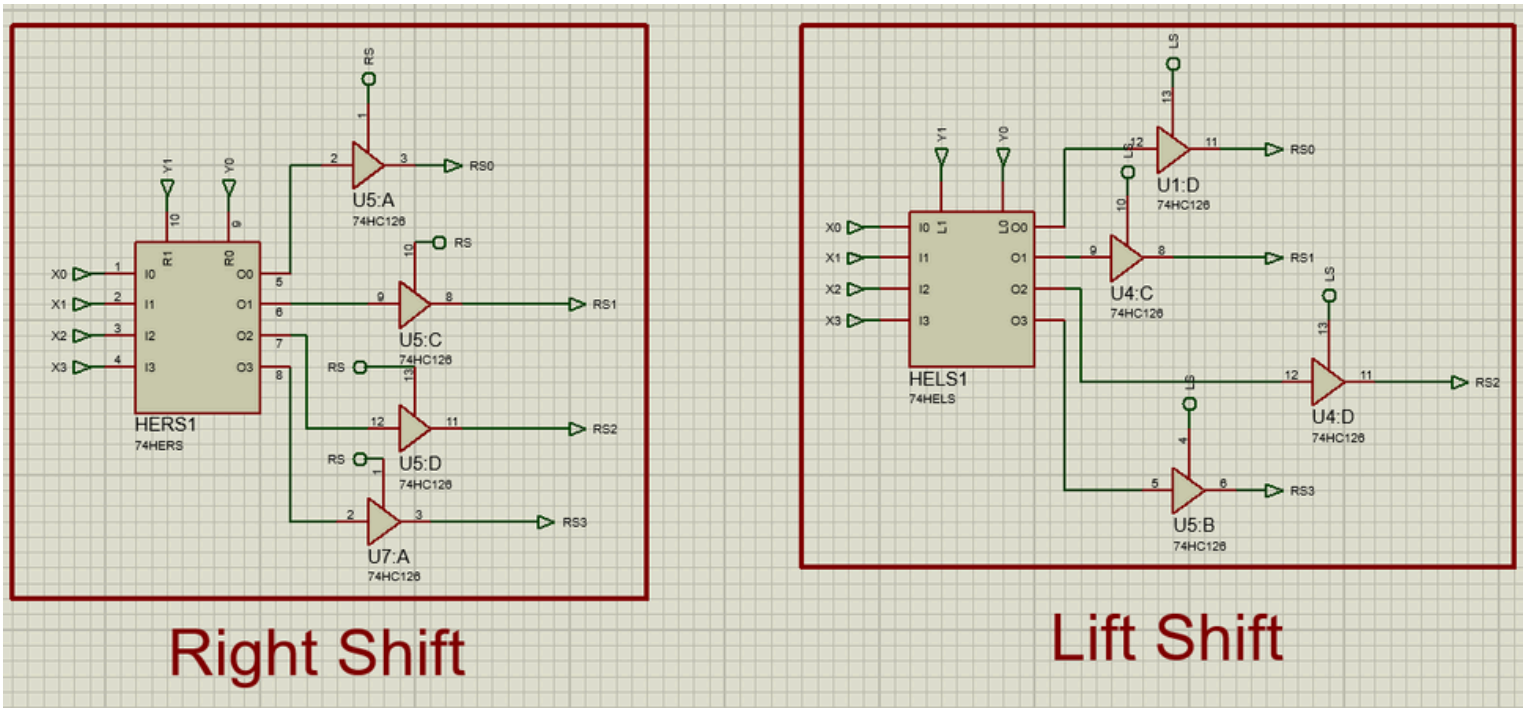
MULT (EN)	Operation	Output State
0	Disabled	High-Z or 0
1	Multiply	A × B

4- AND / OR



AND	OR	U3:A Output (NOT OR)	U2:A Output (AND • NOT OR)	U6:A Output (OR Control)	Operation	Output Enable
0	0	1	0	0	Disabled	High-Z
0	1	0	0	1	OR	Enabled
1	0	1	1	0	AND	Enabled

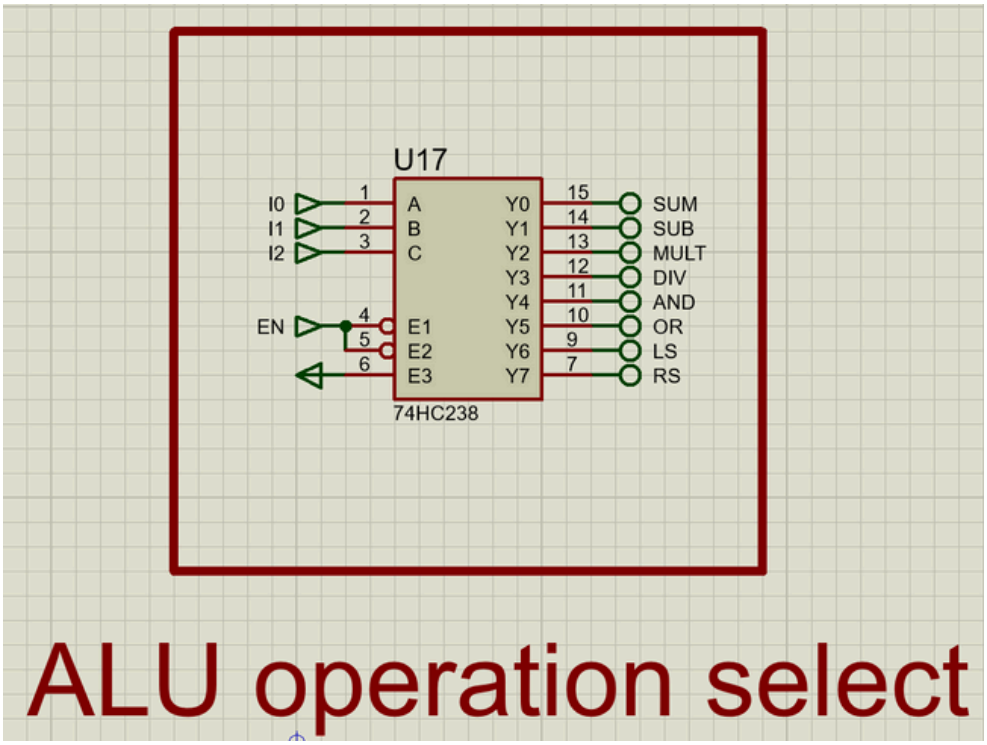
5- Lift Shift & Right Shift



RS	Operation	Output State
0	Disabled	High-Z
1	Right Shift	X >> 1

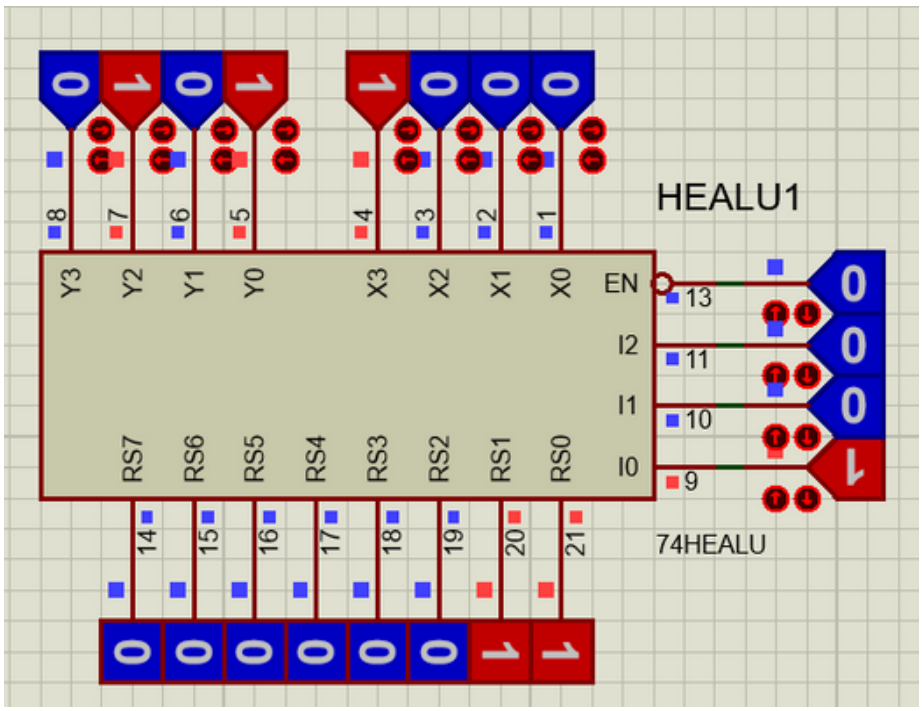
LS	Operation	Output State
0	Disabled	High-Z
1	Left Shift	X << 1

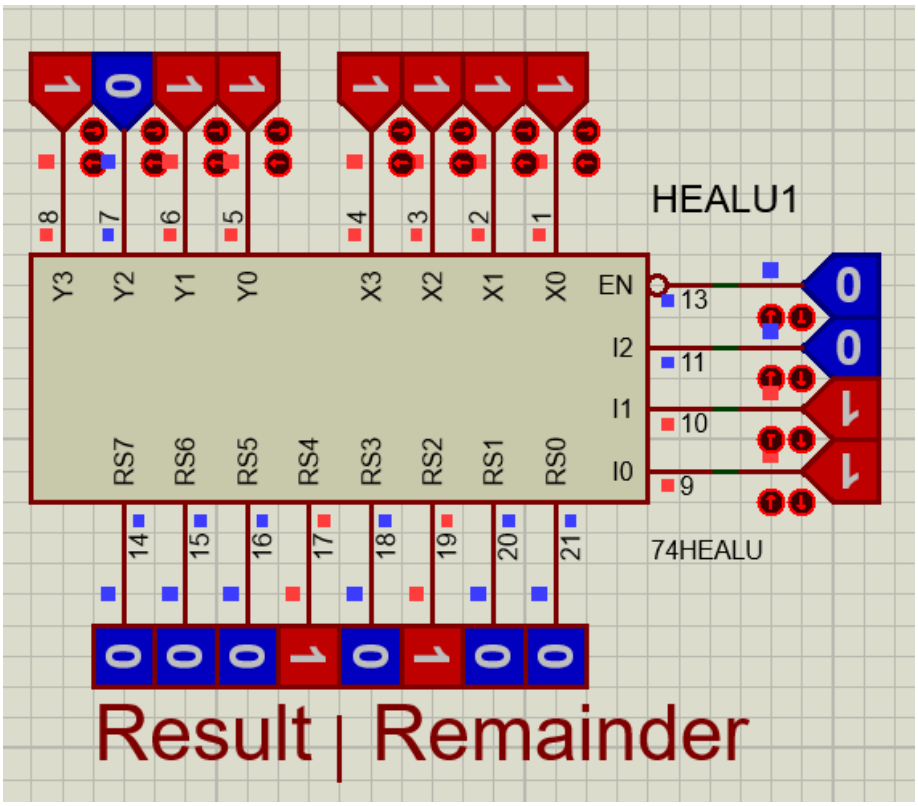
Input and Output Interface

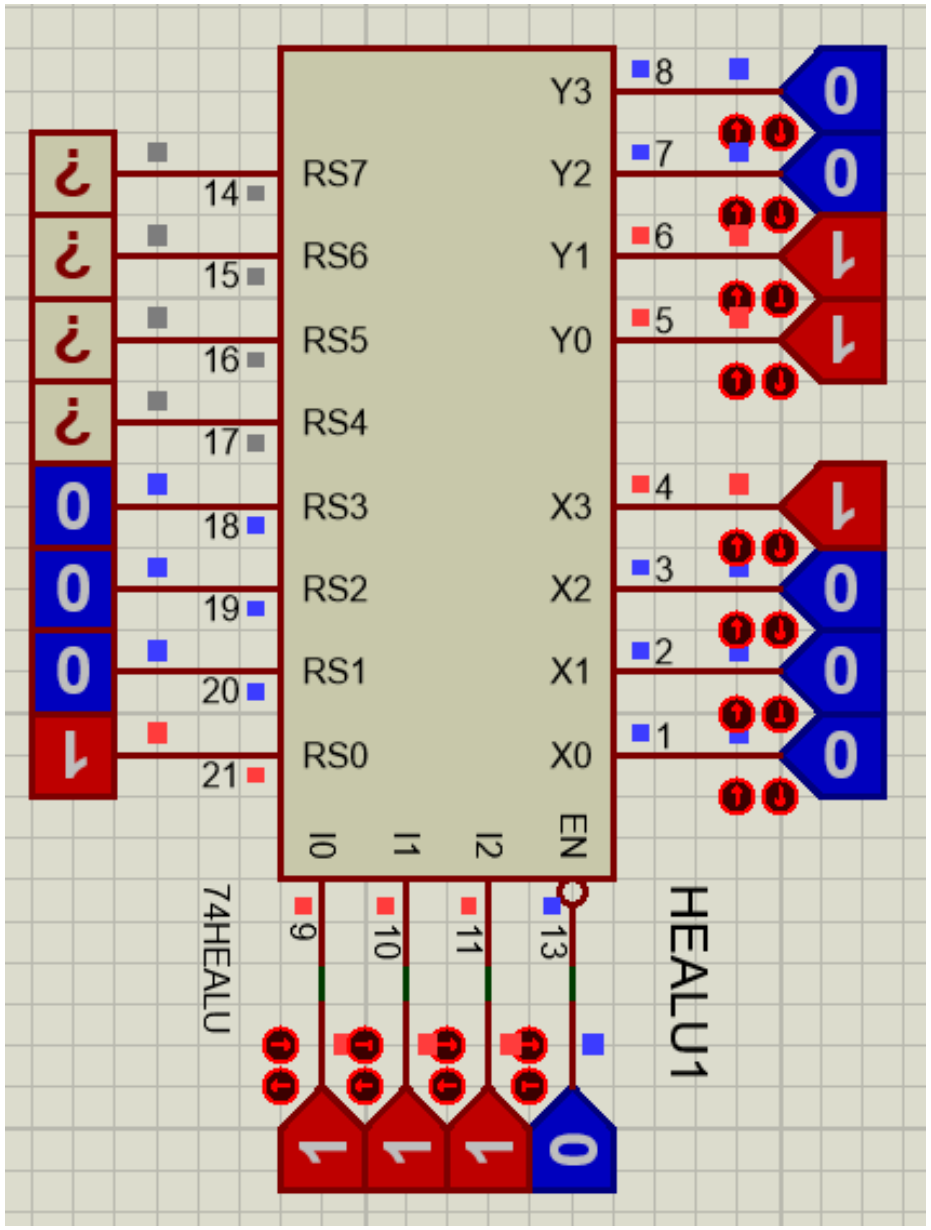


EN	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Selected Operation
0	X	X	X	1	1	1	1	1	1	1	1	None (Disabled)
1	0	0	0	0	1	1	1	1	1	1	1	SUM
1	0	0	1	1	0	1	1	1	1	1	1	SUB
1	0	1	0	1	1	0	1	1	1	1	1	MULT
1	0	1	1	1	1	1	0	1	1	1	1	DIV
1	1	0	0	1	1	1	1	0	1	1	1	AND
1	1	0	1	1	1	1	1	1	0	1	1	OR
1	1	1	0	1	1	1	1	1	1	0	1	LS (Left Shift)
1	1	1	1	1	1	1	1	1	1	1	0	RS (Right Shift)

Testing and Troubleshooting






RS7
RS6
RS5
RS4
RS3
RS2
RS1
RS0
Y3
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X3
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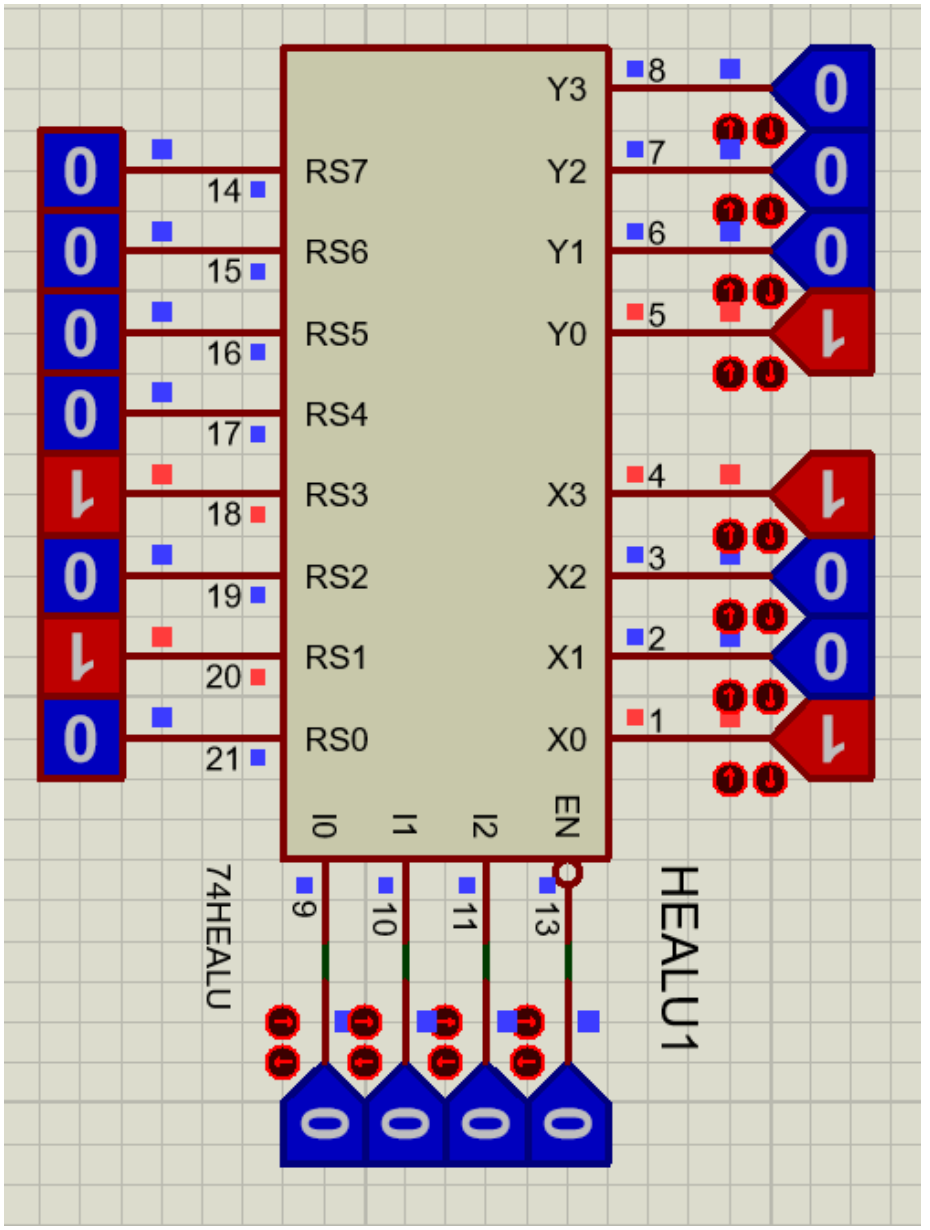
I0
I1
I2
EN
74HEALU
HEALU1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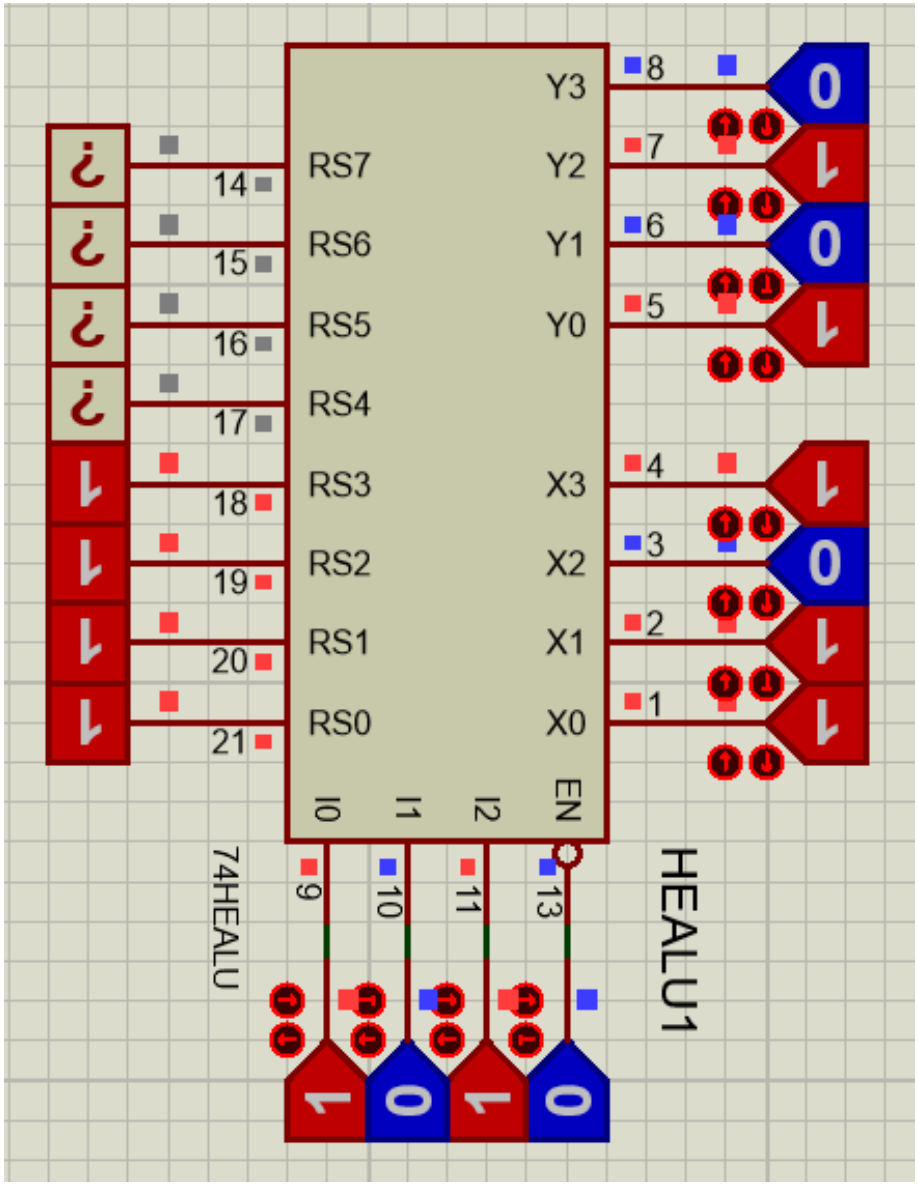
I0
I1
I2
EN
74HEALU
HEALU1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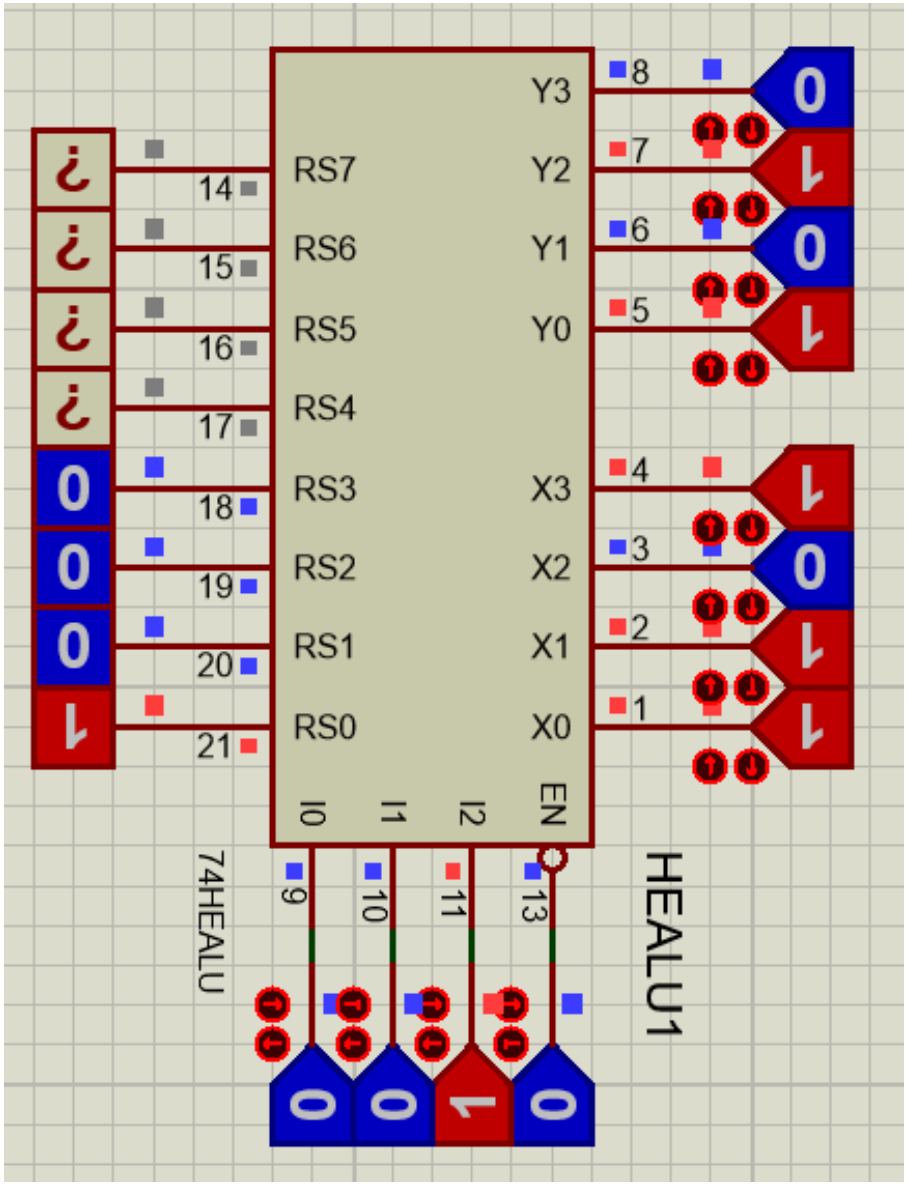
I1
I2
EN
74HEALU
HEALU1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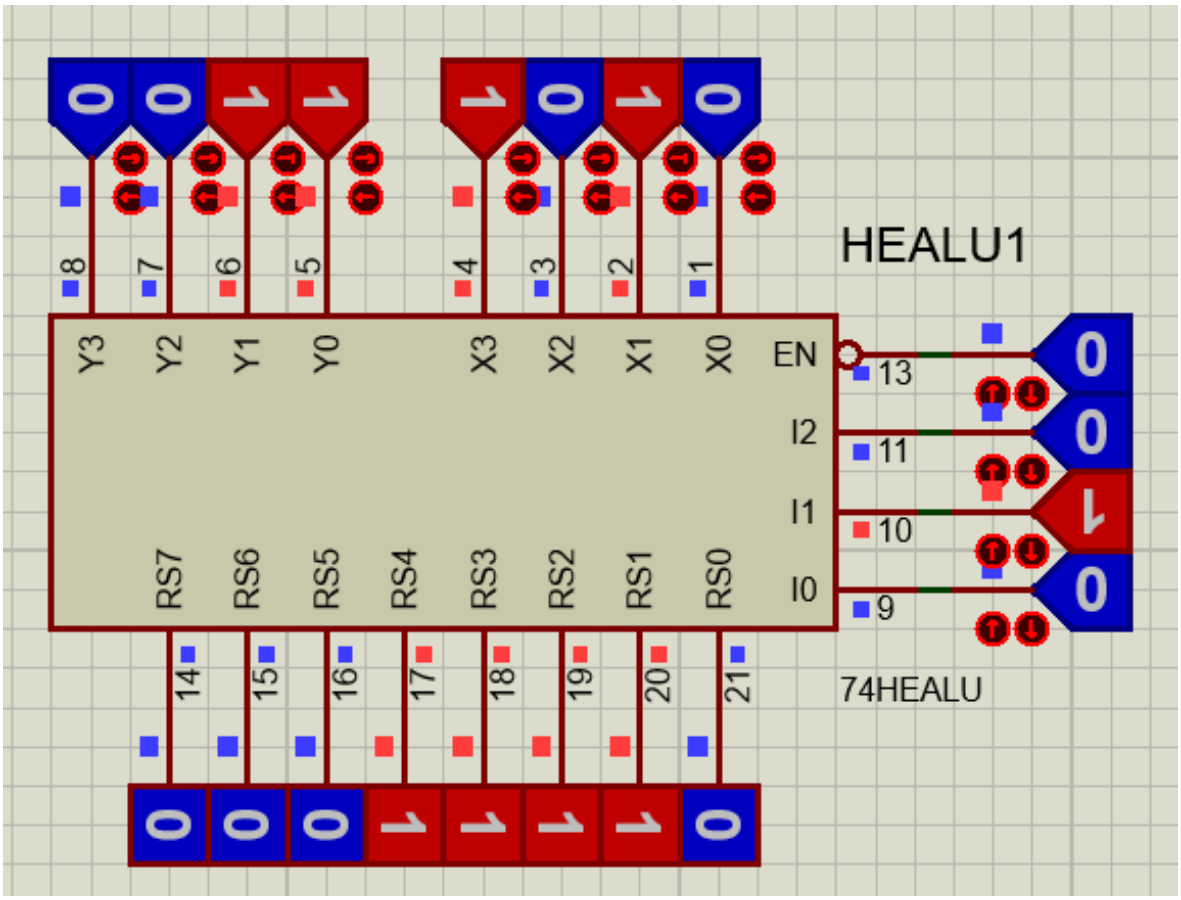
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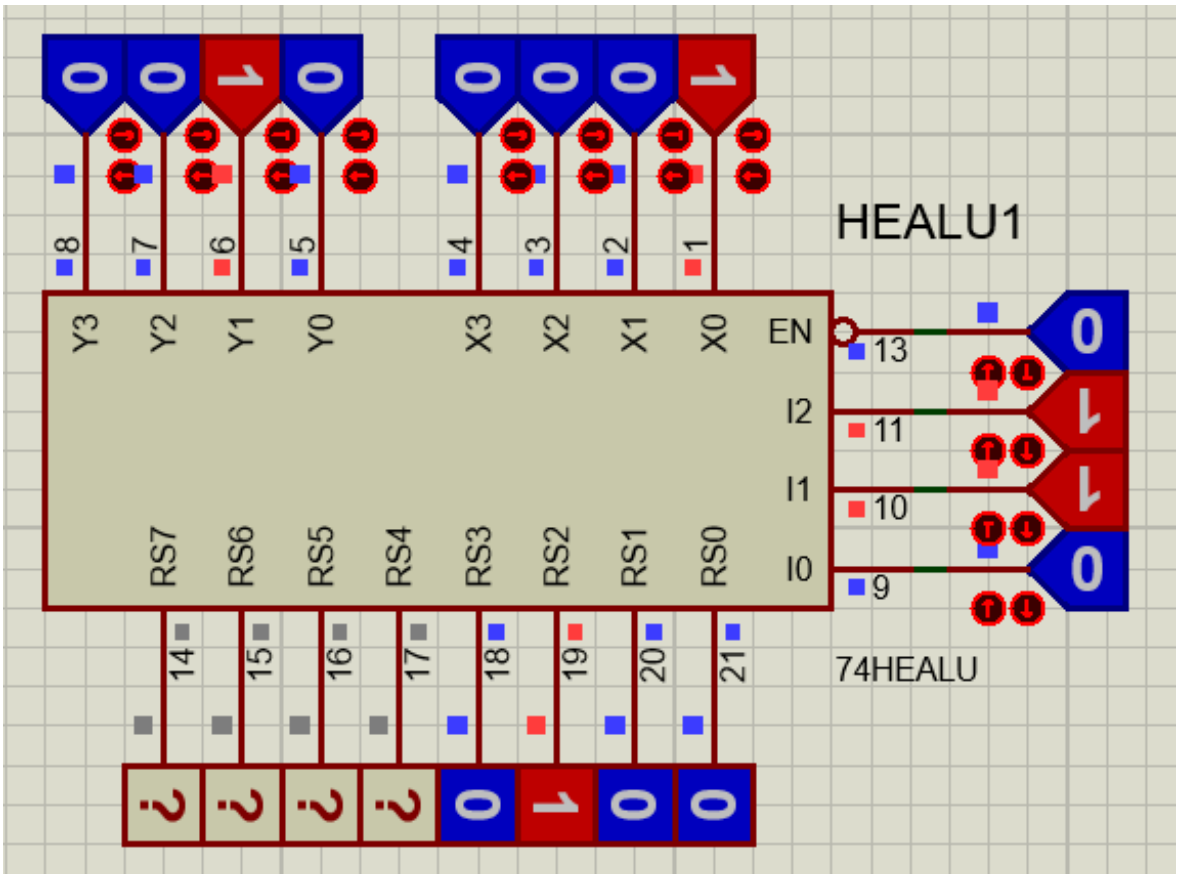
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RS7
RS6
RS5
RS4
RS3
RS2
RS1
RS0
74HEALU

Conclusion

The 4-bit calculator using logic gates was successfully designed and implemented. This hands-on project enhanced understanding of digital circuit design, binary arithmetic, and combinational logic without relying on software tools. It provides a strong foundational experience in hardware-level digital electronics.

Future Enhancements

- **Expand to 8-bit or 16-bit calculator.**
- **Add flags: zero, carry, overflow detection.**
- **Introduce signed number support.**
- **Use ICs like 74181 for compact ALU implementation.**
- **Add display controller (LCD or 7-segment).**
- **Integrate memory or ROM to store multiple results.**