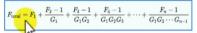
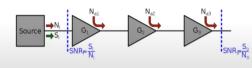
LNA Theory & Fundamentals - Quick Review

Friis's formula is used to calculate the total noise factor of a cascade of stages, each with its own noise factor and power gain (assuming that the impedances are matched at each stage). The total noise factor can then be used to calculate the total noise figure.

The total noise factor is given as:



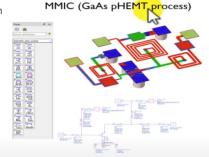
where F_i and G_i are the noise factor and available power gain, respectively, of the i-th stage, and n is the number of stages. Both magnitudes are expressed as ratios, not in decibels.



$$\mbox{Noise Figure} \quad \mbox{NF} = 10 \log_{10}(F) = 10 \log_{10} \left(\frac{\mbox{SNR}_i}{\mbox{SNR}_o} \right) = \mbox{SNR}_{i, \ dB} - \mbox{SNR}_{o, \ dB}$$

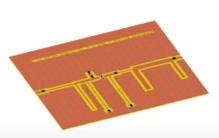
https://en.wikipedia.org/wiki/Friis formulas for noise

LNA Design Process - Options



Proc & Cone

- 1. Good performance & Mass Production friendly
- . Less Size (few microns)
- 3. Can be designed up to very high frequencies (>30 GHz)
- 4. Octave bandwidth possible
- 5. Cost is prohibitive if large quantities are not needed
- 6. Performance tuning not possible after fabrication



Good performance & Low cost

Easy tuning after fabrication

2. Decent performance up to Ku-band (~18 GHz)

5. Large Physical Size (compared to MMIC/RFIC)

4. Octave bandwidth matching - very difficult

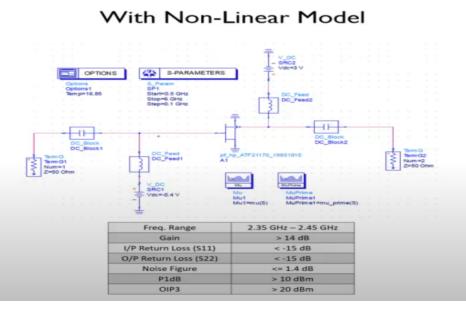
PCB / MIC / RF Board

RFIC (Silicon / CMOS)

Proc & Con

- 1. Decent performance & Mass Production friendly
- Less Size (few microns) and can be integrated into SoCs
- Usually limited to sub 6 GHz applications
- 4. Inferior Noise Figure compared to GaAs due to Silicon
- 5. Cost is prohibitive if large quantities are not needed
- 6. Performance tuning nor possible after fabrication

Transistor Models for LNA Designs



Freq. Range	2.35 GHz - 2.45 GHz
Gain	> 14 dB
I/P Return Loss (S11)	< -15 dB
O/P Return Loss (S22)	< -15 dB
Noise Figure	<= 1.4 dB
- P1dR	> 10 dRm
OIP3	> 20 d0m

