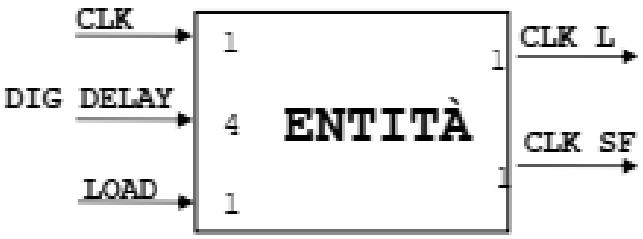
ELECTRONICS PROGRAMMABLE SYSTEMS (9 CFU) **Prof. C.G. GIACONIA**

NOTE:

(Produce synthesis and physical simulation using a Spartan3, XC3S200; Package:VQ100; Speed grade: -4 FPGA, as target. Check maximum available frequency and occupied area of your entity)

LAB07.A

Student will design a VHDL entity, synchronous to a clock signal (**CLK**), able to generate two outputs: the first (**CLK_L**) provides a clock signal with a frequency equal to 1/16 of **CLK**, the second (**CLK_SF**) is a copy of the first one with the only difference of being out of phase with the latter of a programmable amount of time via a 4-bit input (**DIG_DELAY**), whose dynamics covers the 360 degrees of possible phase shift between the two outputs.
The entity will upload a new offset value only in correspondence to a load signal (**LOAD**) which will allow the input of the new value of DIG_DELAY. In any other case, the outputs will remain indefinitely out of phase by an amount equal to the last loaded phase shift value.



LAB07.B

Student will design a VHDL entity synchronous to a clock signal (**CLK**) which is able to generate three outputs: the first (**SLOW**) provides a square wave with a period equal to 32 CLK periods, the second (**FAST**) has instead a period equal to 3 clock periods; the third output (**SHIFT_OUT**) is finally a copy of **SLOW**, with a shift respect to it given by a number of **FAST** periods equal to value read at the 3-bit **DELAY** input.
The entity will upload a new **DELAY** value only if a positive loading pulse (**LOAD**) having a time interval going from 50nsec up to 200ns.
Otherwise, the outputs will remain indefinitely out of phase by a quantity equal to the last loaded phase shift value.