U N I V E R S I T À D I P A L E R M O
D I P A R T I M E N T O D I I N G E G N E R I A

MASTER DEGREE ON ELECTRONICS ENGINEERING

ELECTRONICS PROGRAMMABLE SYSTEMS (9 CFU) **Prof. C.G. GIACONIA**

LAB09

***Exam practice test to be completed within*: 100 minutes**

Candidato (scrivere a stampatello):		
Name:	Surname:	**Submitted: ___ (SI – NO)**
Corso di Laurea:	UNIPA ID N.:	PC:
Fill with personal data and return at the end of test		
(Proceed to the synthesis and physical simulation of the designed entities, reporting the maximum operating frequency of the circuit on FPGA Target Spartan3, XC3S200; Package: VQ100; Speed grade: -4)		

TEST FEATURES AND CONSTRAINTS:

The candidate creates a VHDL entity synchronous to a clock(**CLK**) that, starting from a **RESET** pulse, active low and lasting between 100 and 140 ns, analyze the two serial inputs (**DIN1** and **DIN2**). In the event that the first 16 bits arriving at the two inputs are mirror images of each other (e.g example: 0x00FF and 0xFF00) then the **BINGO** output, normally at 0, will emit a pulse equal to one clock cycle that warns of the start of the emission of a **DOUT16** output containing the word contained in **DIN2.**
The entity will also need to check whether the incoming 16 bits also have a condition of mirroring between the first and second byte of each of the inputs (for example DIN1: 01010101 and 10101010). In this circumstance the entity will have to issue a second pulse at the **BINGO** output, lasting 2 clock periods and, immediately after the output of **BINGO**, a further serial output (**DOUT_BYTE**) containing the eight bits of the first byte arriving from the **DIN1** input. In case the specularity conditions on the inputs are not verified, the **BINGO** output will continue to issue its pulses while the other two outputs will remain at high impedance.
Finally, design the entity so that it can sustain an output speed which, in the worst case, still remains above 1Mbit/sec; and a **DISABLE** signal which, when active, will bring all outputs to high impedance.

The candidate provides:
- the duly commented VHDL description of the aforementioned entity;
- one or more test benches which, in physical simulation,
show the correctness of the entity's functioning and compliance with the required specification times.

NOTES CONCERNING THE ARCHIVING OF THE TEST RESULTS

For correct archiving, the nest steps must be followed:
Test must be solved with the use of the ISE (Xilinx) installed on PCs of the computer room.
Indications for correct saving:

1. Create a folder named with your name and serial number in the directory c:\xilinx\projects (eg: c:\xilinx\projects\surname0123456);
2. At the end of the project execution, save the files and the project and use, from the drop-down menus, the ISE 9.2 project\archive function to archive the entire project in a single .zip file called with name and number of serial number (e.g. surname0123456.zip);
3. Copy the zip file thus formed from the folder c:\xilinx\projects\ to the Desktop of the assigned PC".

FAILURE TO FOLLOW THIS PROCEDURE WILL LEAD TO THE IMPOSSIBILITY, FOR THE TEACHER, TO READ THE TEST CONTENT AND THE CONSEQUENT

NEGATIVE RESULT