

*DDCO LAB ASSIGNMENT*  
*WEEK 2*

*Name: Gautam Vijay Hanchinal*

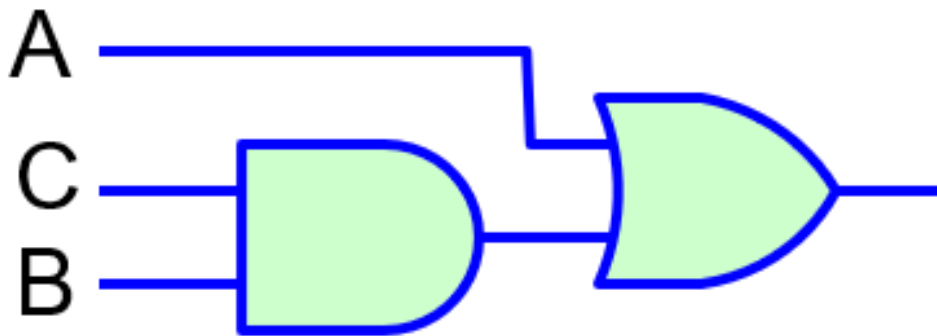
*SRN: PES1UG22CS215*

*Date: 20-08-23*

*Section D*

Circuit 1:

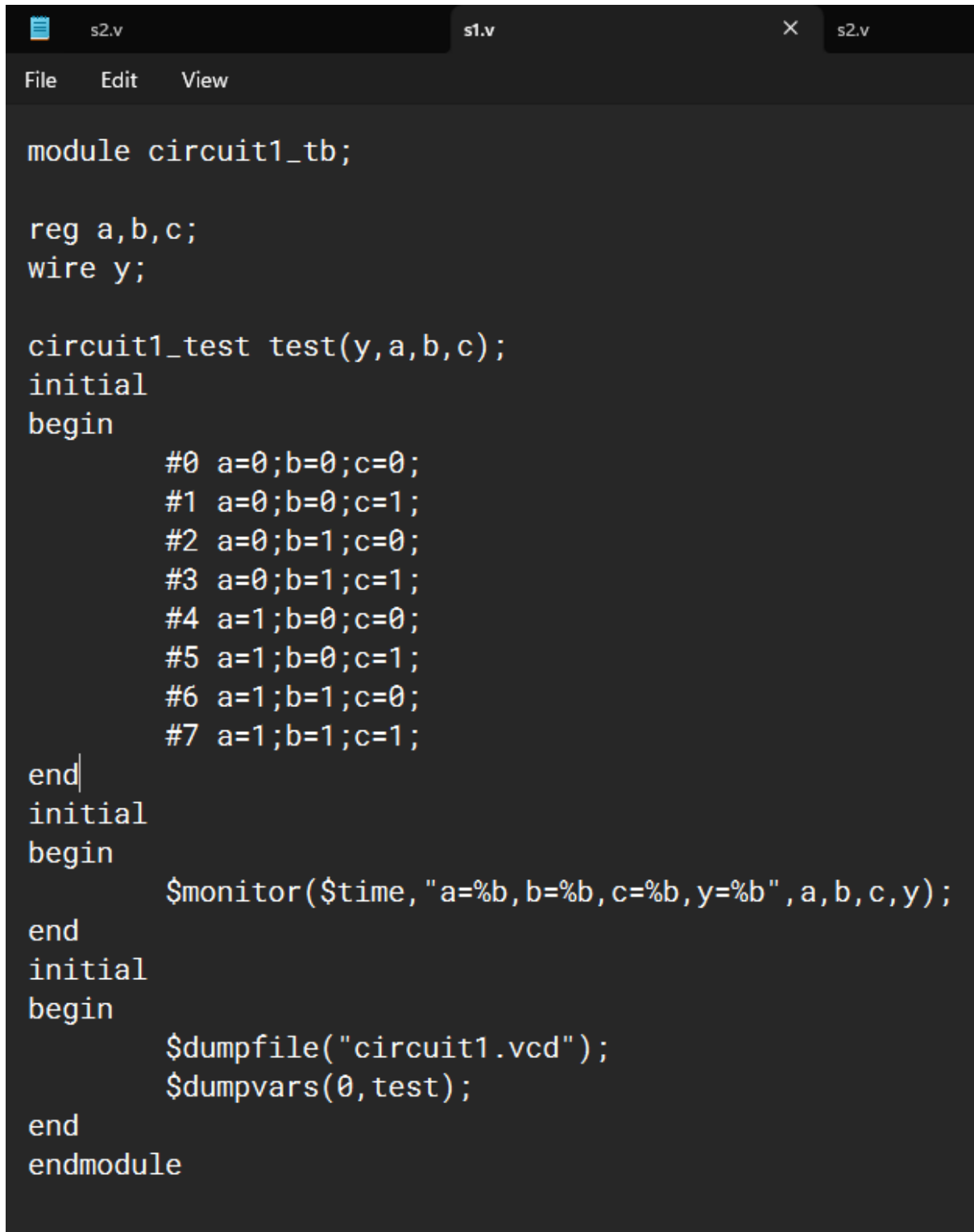
CIRCUIT 1



$$Y = (C \& B) \mid A$$

Code :

```
module circuit1_test(output y,input a,input b,input c);  
  assign y=(c&b)|a;  
endmodule
```



The image shows a screenshot of a Verilog code editor with a dark theme. The editor has a menu bar with 'File', 'Edit', and 'View'. There are two tabs at the top: 's1.v' (active) and 's2.v'. The code is a Verilog testbench for a circuit named 'circuit1'. It defines three registers 'a', 'b', and 'c', and a wire 'y'. It instantiates a test module 'circuit1\_test' with 'y', 'a', 'b', and 'c' as inputs. The testbench includes two 'initial' blocks. The first block contains a sequence of eight delay-based assignments for 'a', 'b', and 'c'. The second block calls '\$monitor' to print the values of 'a', 'b', 'c', and 'y' at every time step. A third 'initial' block calls '\$dumpfile' and '\$dumpvars' to save the simulation data to a file named 'circuit1.vcd'. The code ends with 'endmodule'.

```
module circuit1_tb;

reg a,b,c;
wire y;

circuit1_test test(y,a,b,c);
initial
begin
    #0 a=0;b=0;c=0;
    #1 a=0;b=0;c=1;
    #2 a=0;b=1;c=0;
    #3 a=0;b=1;c=1;
    #4 a=1;b=0;c=0;
    #5 a=1;b=0;c=1;
    #6 a=1;b=1;c=0;
    #7 a=1;b=1;c=1;
end
initial
begin
    $monitor($time,"a=%b,b=%b,c=%b,y=%b",a,b,c,y);
end
initial
begin
    $dumpfile("circuit1.vcd");
    $dumpvars(0,test);
end
endmodule
```

## VVP output:

```
C:\Users\aimem\OneDrive\Desktop\T>iverilog -o test1 s2.v.txt s1.v.txt

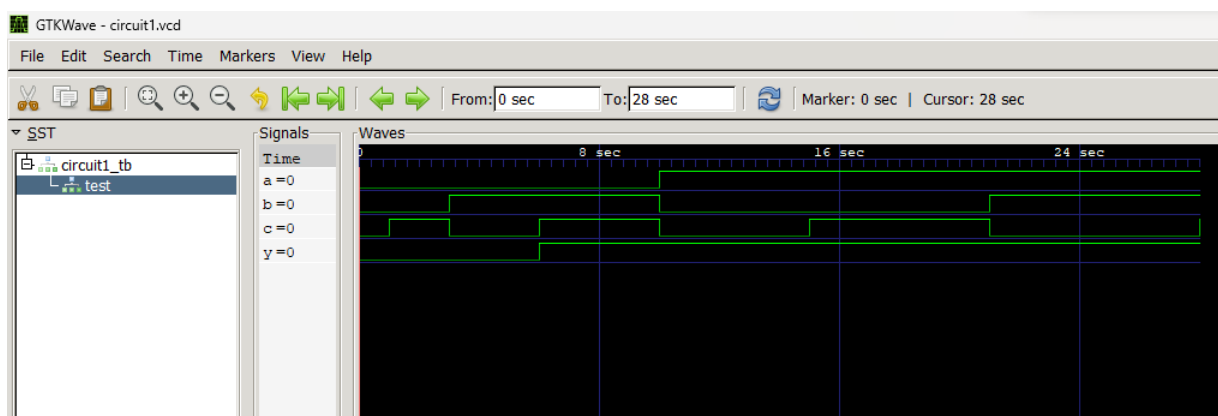
C:\Users\aimem\OneDrive\Desktop\T>vvp test1
VCD info: dumpfile circuit1.vcd opened for output.
      0a=0,b=0,c=0,y=0
      1a=0,b=0,c=1,y=0
      3a=0,b=1,c=0,y=0
      6a=0,b=1,c=1,y=1
     10a=1,b=0,c=0,y=1
     15a=1,b=0,c=1,y=1
     21a=1,b=1,c=0,y=1
     28a=1,b=1,c=1,y=1

C:\Users\aimem\OneDrive\Desktop\T>gtkwave circuit1.vcd

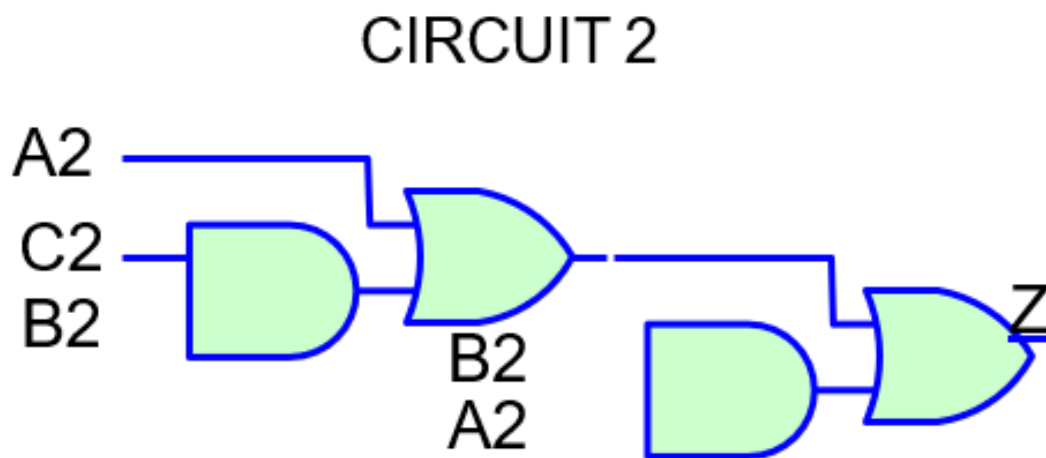
GTKWave Analyzer v3.3.48 (w)1999-2013 BSI

[0] start time.
[28] end time.
```

## GTKwave Output:



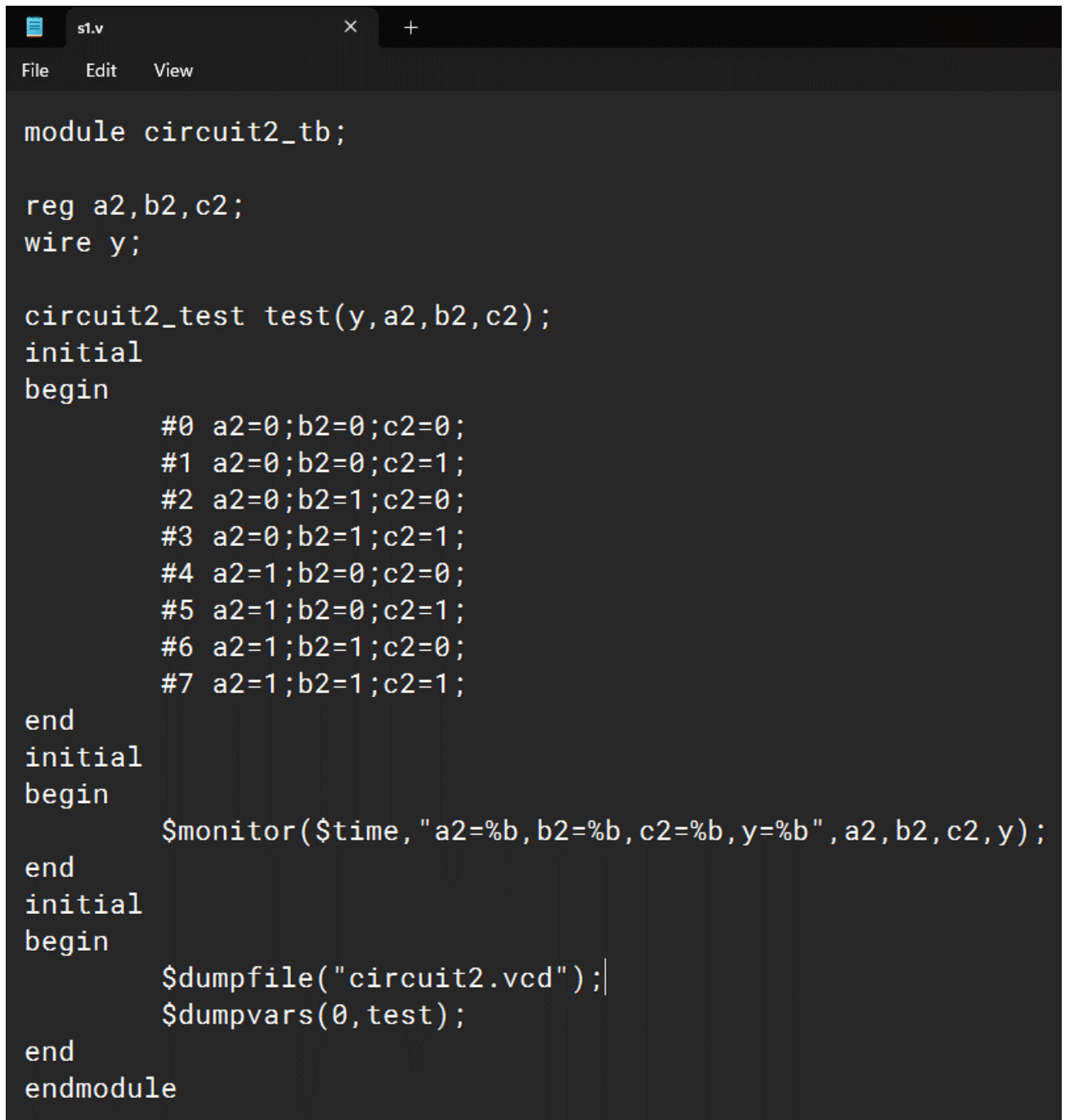
Circuit 2:



$$Y = (A2 \mid (B2 \& C2)) \mid (B2 \& A2)$$

Code :

```
s2.v
File Edit View
module circuit2_test(output y,input a2,input b2,input c2);
assign y=(a2|(c2&b2))|(b2&a2);
endmodule
```



```
module circuit2_tb;

reg a2,b2,c2;
wire y;

circuit2_test test(y,a2,b2,c2);
initial
begin
    #0 a2=0;b2=0;c2=0;
    #1 a2=0;b2=0;c2=1;
    #2 a2=0;b2=1;c2=0;
    #3 a2=0;b2=1;c2=1;
    #4 a2=1;b2=0;c2=0;
    #5 a2=1;b2=0;c2=1;
    #6 a2=1;b2=1;c2=0;
    #7 a2=1;b2=1;c2=1;
end
initial
begin
    $monitor($time,"a2=%b,b2=%b,c2=%b,y=%b",a2,b2,c2,y);
end
initial
begin
    $dumpfile("circuit2.vcd");
    $dumpvars(0,test);
end
endmodule
```

## VVP Output:

```
C:\Users\aimem\OneDrive\Desktop\T>iverilog -o test2 s2.v.txt s1.v.txt

C:\Users\aimem\OneDrive\Desktop\T>vvp test2
VCD info: dumpfile circuit2.vcd opened for output.
      0a2=0,b2=0,c2=0,y=0
      1a2=0,b2=0,c2=1,y=0
      3a2=0,b2=1,c2=0,y=0
      6a2=0,b2=1,c2=1,y=1
     10a2=1,b2=0,c2=0,y=1
     15a2=1,b2=0,c2=1,y=1
     21a2=1,b2=1,c2=0,y=1
     28a2=1,b2=1,c2=1,y=1

C:\Users\aimem\OneDrive\Desktop\T>|
```

## GTKwave Output:

