DDCO ASSIGNMENT
MPROC

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Section D

CODES:

```
module ir (input wire clk, reset, load, input wire [15:0] din, output wire [15:0] dout);
  dfrl dfrl_0 (clk, reset, load, din['h0], dout['h0]);

dfrl dfrl_1 (clk, reset, load, din['h1], dout['h1]);

 dfrl dfrl_2 (clk, reset, load, din['h2], dout['h2]);

dfrl dfrl_3 (clk, reset, load, din['h3], dout['h3]);

dfrl dfrl_4 (clk, reset, load, din['h4], dout['h4]);

dfrl dfrl_5 (clk, reset, load, din['h5], dout['h5]);

dfrl dfrl_6 (clk, reset, load, din['h6], dout['h6]);

dfrl dfrl_7 (clk, reset, load, din['h7], dout['h7]);

dfrl dfrl_8 (clk, reset, load, din['h8], dout['h8]);

dfrl dfrl_9 (clk, reset, load, din['h9], dout['h9]);

dfrl dfrl_a (clk, reset, load, din['ha], dout['ha]);

dfrl dfrl_b (clk, reset, load, din['hb], dout['hb]);

dfrl dfrl_c (clk, reset, load, din['hc], dout['hc]);

 dfrl dfrl_d (clk, reset, load, din['hd], dout['hd]);

dfrl dfrl_e (clk, reset, load, din['he], dout['he]);

 dfrl dfrl_f (clk, reset, load, din['hf], dout['hf]);

endmodule
```

```
module nor5 (input wire [0:4] i, output wire o);

wire t;

 or3 or3_0 (i[0], i[1], i[2], t);

 nor3 nor3_0 (t, i[3], i[4], o);
endmodule


module control_logic (input wire clk, reset, input wire [15:0] cur_ins, output wire [2:0] rd_addr_a, rd_addr_b, wr_addr, output wire [1:0] op, output wire pc_inc, load_ir, wr_reg);

wire t, alu_ins;

 dfsl fetch (clk, reset, 1'b1, wr_reg, pc_inc);

assign load_ir=pc_inc;

dfrl dec_exec (clk, reset, 1'b1, load_ir, t);

nor5 nor5_0 (cur_ins[15:11], alu_ins);

and2 and2_0 (t, alu_ins, wr_reg);

assign rd_addr_a = cur_ins[2:0];

assign rd_addr_b = cur_ins[5:3];

assign wr_addr = cur_ins[8:6];

assign op = cur_ins[10:9];

endmodule
```

```
module ram_128_16 (input wire clk, reset, wr, input wire [6:0] addr, input wire [15:0] din, output wire [15:0] dout);
  reg [0:127] ram [15:0];

  initial begin
    ram[0]=16'o000100;
    ram[1]=16'o001201;
    ram[2]=16'o002321;
    ram[3]=16'o003432;
  end
  always @(wr) ram[addr]=din;
  assign dout=ram[addr];
endmodule

module mproc_mem (input wire clk, reset);
  wire [15:0] addr; wire [15:0] ins;

  ram_128_16 ram_128_16_0 (clk, reset, 1'b0, addr[6:0], 16'b0, ins);
  mproc mproc_0 (clk, reset, ins, addr);
endmodule
```

```
`timescale 1 ns / 100 ps

`define TESTVECS 4


module tb;

 reg clk, reset;

 integer i;

  initial begin
$dumpfile("tb_mproc_mem.vcd");
$dumpvars(0,tb);
end

 initial
begin
reset = 1'b1;
#12.5 reset = 1'b0;
 end

 initial clk = 1'b0;
 always #5 clk =~ clk;

mproc_mem mproc_mem_0 (clk, reset);

initial begin

#6 for(i=0;i<`TESTVECS;i=i+1)

   begin #10; end

 #100 $finish;

 end
endmodule
```

GTK WAVE OUTPUT: