DDCO LAB ASSIGNMENT

WEEK 2

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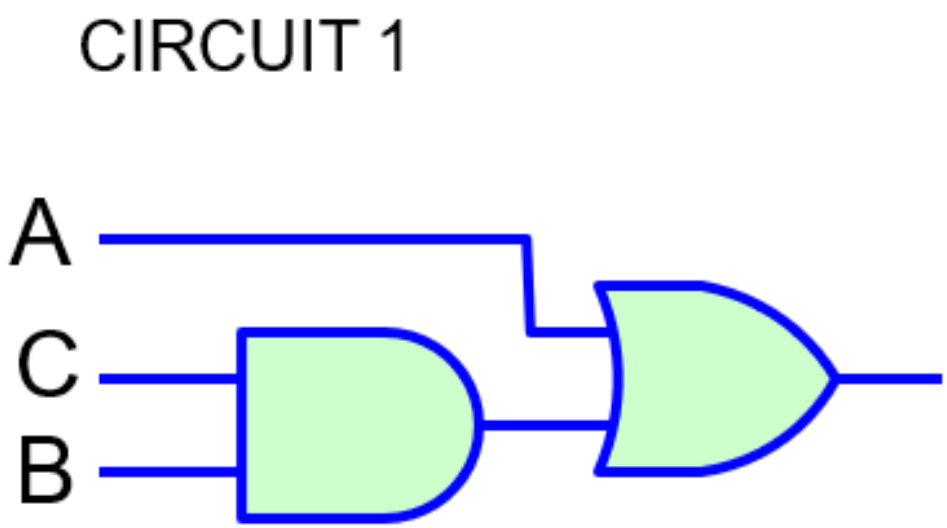
Section D

Circuit 1:



$$Y = (C\&B) \mid A$$

Code:

s2.v s1.v s2.v

File Edit View

```
module circuit1_test(output y,input a,input b,input c);
assign y=(c&b)|a;
endmodule
```

s2.v | s1.v | s2.v

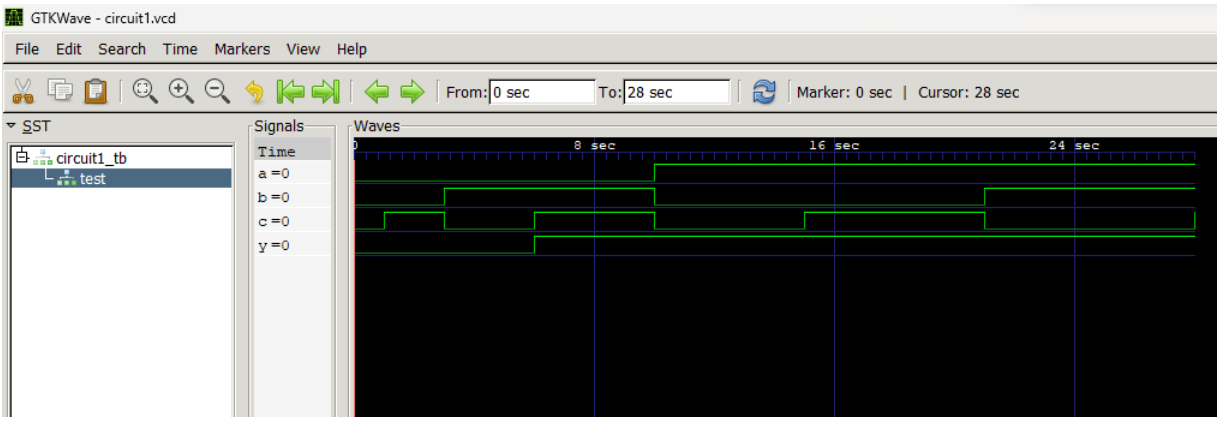
File Edit View

```
module circuit1_tb;

reg a,b,c;
wire y;

circuit1_test test(y,a,b,c);
initial
begin
        #0 a=0;b=0;c=0;
        #1 a=0;b=0;c=1;
        #2 a=0;b=1;c=0;
        #3 a=0;b=1;c=1;
        #4 a=1;b=0;c=0;
        #5 a=1;b=0;c=1;
        #6 a=1;b=1;c=0;
        #7 a=1;b=1;c=1;
end
initial
begin
        $monitor($time,"a=%b,b=%b,c=%b,y=%b",a,b,c,y);
end
initial
begin
        $dumpfile("circuit1.vcd");
        $dumpvars(0,test);
end
endmodule
```

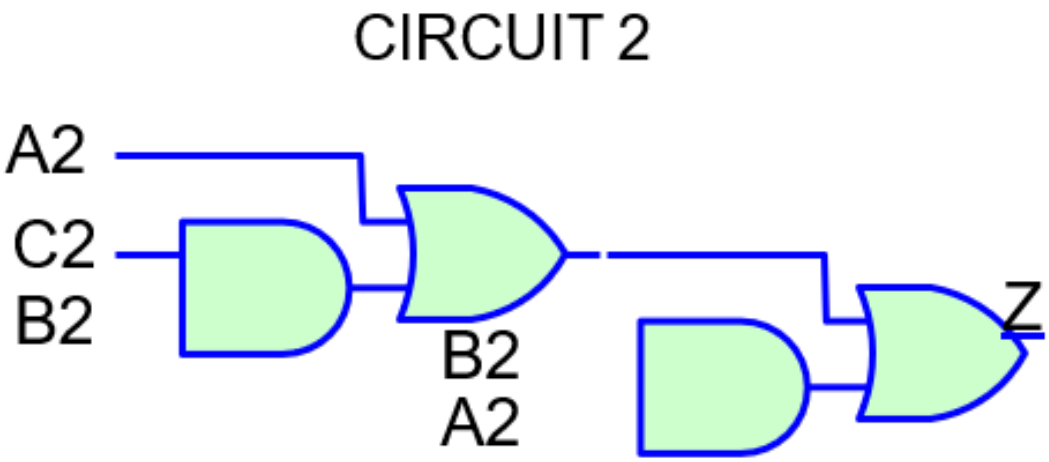
VVP output:

```
C:\Users\aimem\OneDrive\Desktop\T>iverilog -o test1 s2.v.txt s1.v.txt

C:\Users\aimem\OneDrive\Desktop\T>vvp test1
VCD info: dumpfile circuit1.vcd opened for output.
                   0a=0,b=0,c=0,y=0
                   1a=0,b=0,c=1,y=0
                   3a=0,b=1,c=0,y=0
                   6a=0,b=1,c=1,y=1
                  10a=1,b=0,c=0,y=1
                  15a=1,b=0,c=1,y=1
                  21a=1,b=1,c=0,y=1
                  28a=1,b=1,c=1,y=1

C:\Users\aimem\OneDrive\Desktop\T>gtkwave circuit1.vcd

GTKWave Analyzer v3.3.48 (w)1999-2013 BSI

[0] start time.
[28] end time.
```

GTKwave Output:



Circuit 2:



$$Y = (A2|(B2\&C2))|(B2\&A2)$$

Code:

s2.v

File Edit View

```
module circuit2_test(output y,input a2,input b2,input c2);
assign y=(a2|(c2&b2))|(b2&a2);
endmodule
```

s1.v

File Edit View

```
module circuit2_tb;

reg a2,b2,c2;
wire y;

circuit2_test test(y,a2,b2,c2);
initial
begin
        #0 a2=0;b2=0;c2=0;
        #1 a2=0;b2=0;c2=1;
        #2 a2=0;b2=1;c2=0;
        #3 a2=0;b2=1;c2=1;
        #4 a2=1;b2=0;c2=0;
        #5 a2=1;b2=0;c2=1;
        #6 a2=1;b2=1;c2=0;
        #7 a2=1;b2=1;c2=1;
end
initial
begin
        $monitor($time,"a2=%b,b2=%b,c2=%b,y=%b",a2,b2,c2,y);
end
initial
begin
        $dumpfile("circuit2.vcd");
        $dumpvars(0,test);
end
endmodule
```

VVP Output:

```
C:\Users\aimem\OneDrive\Desktop\T>iverilog -o test2 s2.v.txt s1.v.txt

C:\Users\aimem\OneDrive\Desktop\T>vvp test2
VCD info: dumpfile circuit2.vcd opened for output.
                   0a2=0,b2=0,c2=0,y=0
                   1a2=0,b2=0,c2=1,y=0
                   3a2=0,b2=1,c2=0,y=0
                   6a2=0,b2=1,c2=1,y=1
                  10a2=1,b2=0,c2=0,y=1
                  15a2=1,b2=0,c2=1,y=1
                  21a2=1,b2=1,c2=0,y=1
                  28a2=1,b2=1,c2=1,y=1

C:\Users\aimem\OneDrive\Desktop\T>
```

GTKwave Output: