Aror University of Art, Architecture, Design & Heritage Sukkur.

BS (Multimedia Gaming)
Spring-2024
Digital Logic Design

Course Title:	Digital Logic Design
Course Code:	CS103
Credit Hours:	(2+1)
Course Instructor:	Dr. Santosh Kumar Banbhrani
Electronic mail:	santosh.faculty@aror.edu.pk
Office location:	Faculty office, 2nd floor, Building 02
Consulting hours:	2:30PM to 4:30PM (Tuesday)

Description:

The aim of this course is to provide students with a good understanding of basic concepts, techniques, and principles of logic design in digital circuits.

COURSE LEARNING OUTCOMES

The students will be able:

CLO1: **Simplify** the Boolean Expressions using Boolean laws, rules, theorems and Karnaugh map

CLO2: **Interpret** the functionality of basic combinational and sequential logic circuits

CLO3: **Demonstrate** practical skills to build combinational and sequential digital logic circuits using fixed function Integrated Circuits (IC).

CLOs	Level of learning	Mapped OBE PLOs	Mapped ABET SOs	Teaching Methods	CLO attainment checked in
CLO1	**Cog-4**	**1**	1	Lectures, tutorials	First Term Exam,
CLO2	**Cog-2**	**1**		Lectures, tutorials	Second Term Exam, Quiz 2
CLO3	**Psych-4**	**5**		Lectures, Demonstrations	Lab Exams

Mapped OBE Program Learning Outcomes (PLOs):

PLO1 Engineering Knowledge: An ability to apply knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems.

PLO5 Modern Tool Usage: An ability to create, select and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modelling, to complex engineering activities, with an understanding of the limitations.

Mapped ABET Student Outcomes (SOs):

SO1: An ability to identify, formulate and solve complex engineering problems by applying principles of engineering science and mathematics

Performance Indicator for SO1 are:

a. Identification of specific facts of mathematics, science and engineering for a given situation.
b. Convert real world situation into an appropriate model
c. Ability to solve engineering problems using relevant facts of mathematics, science and engineering

Assessment: Theory

S. No	**Assessment Activities**	Percentage	Total Activities
1.	Sessional: Quizzes and Assignments	30%	10
2.	Mid Term Exam	30%	1
3.	Final Exam	40%	1

Assessment: Lab

S. No	**Assessment Activities**	Percentage	Total Activities
1.	Lab Handout Submissions	30%	10
2.	Mid Term Exam	30%	1
3.	Final Exam	40%	1

Recommended Books: (Textbook)

S.No	**Book Name**	**Author/s Name**	**Publisher Name & Edition**
1.	Digital Fundamentals (11th Ed)	Floyd Thomas	Prentice Hall, USA.

Reference Books:

1.	Digital Systems: Principles & Applications	R. C. Tocci	Prentice Hall, USA
2.	Digital Electronics: Principles & Applications	R. Tokheim	McGraw Hill.
3.	Introduction to Digital Electronics,	Crowe John and Hayes-Gill Barrie	Newnes Books, UK. ISBN = 0340645709,
4.	Digital Design	M. Moris Mano	Pearson, Prentice Hall.

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Course Outlines:

Weeks	LEC#	SUBTOPICS .	REFERENCE	Course% Covered
Week No: 01	Lec: 01	• Introduction to the Class & Subject • Introductory Analog and Digital Concepts • Binary digits	Sections 1.1-1.3	2.08%
	Lec: 02	• Logic levels • Digital waveform (periodic and non-periodic) • Basic Logic Operations.	Sections 1.1-1.3	4.16%
Week No: 02	Lec :03	• Number Systems and conversions (Binary, Decimal, Hexadecimal, Octal)	Sections 2.1-2.12	8.33%
	Lec: 04	• Signed Numbers, • Arithmetic Operations with Signed Numbers	Sections 2.1-2.12	10.41%
Week No: 03	Lec: 05	• Binary Arithmetic, • Digital Codes (Gray Code, Alphanumeric Codes, Unicode) • Error Codes (Parity Method for Error Detection and Cyclic Redundancy Check)	Sections 2.1-2.12	14.57%
	Lec: 06	• Logic Gates • Truth Table	Sections 2.1-2.12	16.65%
Week No: 04	Lec: 07	• Boolean Algebra, • Apply the basic laws and rules of Boolean Algebra to simplify Boolean expressions DE Morgan's theorems.	Sections 4.1-4.11	20.81%
	Lec: 08	• Sum-of-Product (SOP) and • the Product-of Sum (POS) expressions • converting a Boolean expression to a truth table and vice versa.	Sections 4.1-4.11	22.89%
Week No:05	Lec: 09	• The Karnaugh Map • simplification using Karnaugh Map • The Karnaugh Map Examples	Sections 4.1-4.11	27.05%

	Lec: 10	• Quine McCluskey Method	**Sections 4.1-4.11**	**31.21%**
Week No:06	**Lec: 11**	• Combinational Logic Analysis	**Sections 5.1 -5.5**	**33.29%**
	Lec: 12	• Basic Combinational Logic Circuits	**Sections 5.1 -5.5**	**35.37%**
Week No:07	**Lec: 13**	• Implementing Combinational Logic	**Sections 5.1 -5.5**	**39.53%**
	Lec: 14	• The Universal Property of NAND and NOR Gates	**Sections 5.1 -5.5**	**41.61%**
Week No: 08	**Lec: 15**	• Combinational Logic Using NAND and NOR Gates	**Sections 5.1 -5.5**	**44.71%**
	Lec: 16	• Pulse Waveform Operation.	**Sections 5.1 -5.5**	**50.00%**
Midterm exam				
Week No: 09	**Lec: 17**	• Functions of Combinational Logic • Half and Full Adders • Parallel Binary Adders	**Sections 6.1 – 6.10**	**52.00%**
	Lec: 18	• Ripple Carry and Look-Ahead Carry Adders • Comparators	**Sections 6.1 – 6.10**	**54.09%**
Week No: 10	**Lec: 19**	• Decoders • Encoders • Code Converters	**Sections 6.1 – 6.10**	**58.27%**

	Lec: 20	• Multiplexers (Data Selectors) • Demultiplexers • Parity Generators/Checkers.	**Sections 6.1 – 6.10**	**60.36%**
Week No: 11	**Lec: 21**	• Latches, Flip-Flops, and Timers • Latches: Introduction • S-R Latch	**Sections 7.1, 7.2, 7.4**	**64.54%**
	Lec: 22	• Gated S-R Latch • Gated D-Latch.	**Sections 7.1, 7.2, 7.4**	**70.34%**
Week No: 12	**Lec: 23**	• Flip Flops: • S-R Flip Flop • J-K Flip Flop	**Sections 7.1, 7.2, 7.4**	**72.42%**
	Lec: 24	• D-Flip Flop • T-Flip Flop • Applications	**Sections 7.1, 7.2, 7.4**	**74.5%**
Week No:13	**Lec: 25**	• Shift Register Operations • Types of Shift Register Data I/Os	**Sections 8.1 – 8.5**	**78.66%**
	Lec: 26	• Bidirectional Shift Registers • Shift Register Counters • Shift Register Applications.	**Sections 8.1 – 8.5**	**80.74%**
Week No: 14	**Lec: 27**	• Counters	**Sections 9.1 – 9.4, 9.6, 9.8**	**84.9%**
	Lec: 28	• Finite State Machines • Asynchronous Counters	**Sections 9.1 – 9.4, 9.6, 9.8**	**86.98%**
Week No:15	**Lec: 29**	• Synchronous Counters • Up/Down Synchronous Counters	**Sections 9.1 – 9.4, 9.6, 9.8**	**93%**
	Lec: 30	• Cascaded Counters • Counter Applications	**Sections 9.1 – 9.4, 9.6, 9.8**	**100%**

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Week No: 16	REVISION

Labs outline and proposed lab projects here:

Lab	Objective	Mapped CLO
1	NOT, AND, OR Gate	CLO 3
2	Logic Gates Explored and Boolean Algebra	
3	Binary Conversion and Adders	
4	Karnaugh Maps	
5	Karnaugh Maps in Seven Segment Displays	
6	Decoder and Encoder	
7	Comparators	
8	Multiplexers and De-multiplexer	
9	Flip Flops	
10	Bidirectional Shift Registers	

S. No	Project Title
1	Digital Watch
2	Stop Watch
3	Frequency Down Converter
4	PWM
5	Traffic Signal Control System
6	Clock Generator
7	Security System
8	Serial to Parallel Converter
9	Parallel to Serial Converter
10	4 Digit Arithmetic Calculator

Course Instructor

Name	Dr. Santosh Kumar Banbhrani
Designation	Assistant Professor
Department	AI-Multimedia Gaming