AROR UNIVERSITY
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Faculty of Artificial Intelligence & Multimedia Gamming

BS – Multimedia Gamming

Digital Logic Design Lab

Lab # 07: Half Adder and Full Adder

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Submission Profile

Name: Submission date (dd/mm/yy):

Marks obtained:

Comments:

_____

Instructor

Lab Learning Objectives:

Upon successful completion of this experiment, the student will be able:

- To implement half and full adders with logic gates and create truth tables from them
- To implement multiple full adders with each other to explore the ripple effect
- To verify the truth table for a full adder

Lab Hardware and Software Required:

Platform: NI ELVIS III	✔ View User Manual: http://www.ni.com/en-us/support/model.ni-elvis-iii.html ✔ View Tutorials: https://www.youtube.com/playlist?list=PLvcPIuVaUMIWm8ziaSxv0gwtshBA2dh_M
Hardware: Digilent Digital Electronics Board for NI ELVIS III	✔ View NI DSDB Board Manual: http://www.ni.com/pdf/manuals/376627b.pdf
Software: NI Multisim 14.0.1 Education Version or newer	✔ Install Multisim: http://www.ni.com/gate/gb/GB_ACADEMICEVALMULTISIM/US ✔ View Help: http://www.ni.com/multisim/technical-resources/
Software: NI LabVIEW FPGA Vivado 2014.4	✔ Install: http://www.ni.com/download/labview-fpga-module-2015-sp1/5920/en/ **Note:** Digilent Driver (The installer above automatically downloads the installer below onto your computer) ✔ Navigate to: C:\NIFPGA\programs\Vivado2014_4\data\xicom\cable_drivers\nt64\digilent ✔ Install: install_digilent.exe

Background Theory:

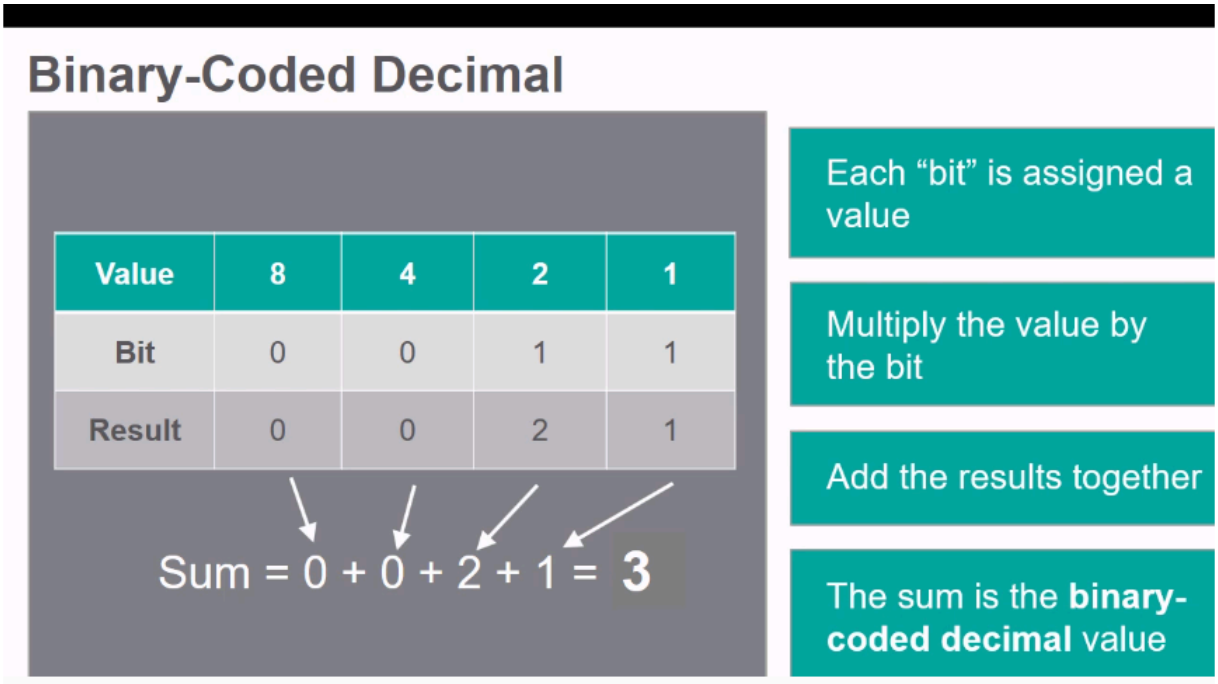


Figure 1-1 Video. View the video here: https://youtu.be/YYGAPRraclY

Video Summary

- In larger circuits it is not practical to make truth tables so binary is converted into a binary-coded decimal (BDC)
- Half adders can be represented in Multisim by a single component or by creating them using an AND and an XOR gate
- Half adders have two inputs and two outputs
- Full adders can be represented in Multisim by a single component or two AND gates and three XOR gates
- Full adders have three inputs and two outputs

Binary-Coded Decimals

Let's look at the following example of a 4-bit binary number (four binary numbers code to one decimal number):

0101

The number furthest to the right is given the value of 1 (similar to the ones column in regular addition). The position immediately to its left is given the value of 2 (similar to a tens column). The value to the left of this is 4 (similar to the hundreds column). The pattern you will notice is

that the values assigned to the number on the left increase by twice the value of the number before it.

In our example, from left to right, the BCD value for the four-bit binary code above, adding up the values is:

0 + 4 + 0 +1 = 5

Conversions that result in a single digit number (0-9) are already in BCD format. In order to output the decimal value of a binary number greater than 9 in circuitry, a Binary-to-BCD converter such as a Shift-Add-3 algorithm must be used.

Adders

Half-Adders:

- A half-adder does binary addition on two inputs (A and B).
- The two outputs are labeled sum (S) and carry (C).
- Half adders can be built with:
    - an XOR gate and an AND gate (shown on the left).
    - a component in Multisim (shown on the right).

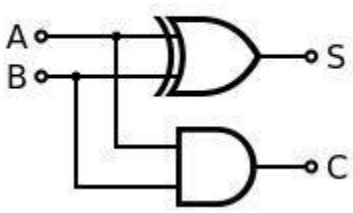


Figure 1-2 Half Adder from Gates

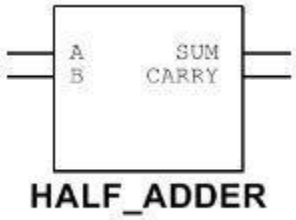
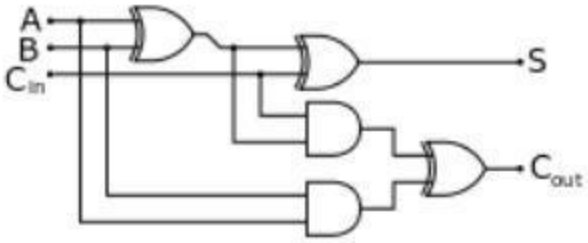


Figure 1-3 Half Adder Multisim

Full-Adders:

- A full-adder does binary addition on three inputs: A, B, and C_{in}.
- Full adders usually work in a cascade fashion where they are used to add binary numbers with an increasing number of bits.
- The two outputs are sum (S) and carry (C_{out}).
- You will notice that full adders can also use logic gates or a component.



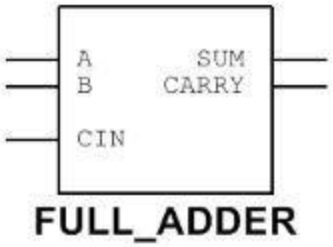


Figure 1-4 Full Adder from Gates *Figure 1-5 Full Adder Multisim*

Lab Example:

Build the following Half-Adder circuit using multiple Gates in Multisim:

Half-Adder Circuits

Half-adder circuits can be built using a combination of logic gates.

- Launch Multisim.
- Open a new circuit.
  - Select **File>>New**.
  - In the menu that appears, select **Blank** and click **Create**.
- Connect the following circuit:
  - Place an **XOR** gate and an **AND** gate from the **Misc Digital** group.
  - Place two **INTERACTIVE_DIGITAL_CONSTANTs** from the **Sources** group.
  - Place two **PROBE_DIG_REDs** from the **Indicators** group.
  - Wire them as shown:

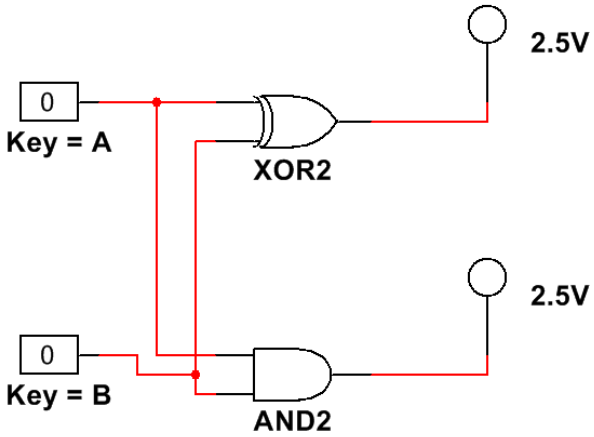


Figure 1-6 A Half Adder Circuit

- Click the **Run** button to begin simulating the circuit.

Figure 1-7 Run Button

- Using the **A** and **B** keys, vary the inputs into the circuit.

1-4 Fill out the truth table below.

A	B	XOR (SUM)	AND (CARRY)
0	0		
0	1		
1	0		
1	1		

- Stop the simulation by clicking the **Stop** button.

Figure 1-8 Stop Button

Can you see how the XOR and AND gates represent the sum and carry of the numbers A and B added together?

- 0 + 0 = 0
- 1 + 0 or 0 + 1 = 1, with no carry.
- 1 + 1 = 2, but 2 is not a binary number. In binary, 2 is represented as 10. The 1 is the carry and the 0 is the sum.

Lab Activity:

Build the following Full-Adder circuit using multiple Gates in Multisim:

Full-Adder Circuits

Open a new Multisim File

Connect the following circuit:

- Place three **XOR** gates and two **AND** gates from the **Misc Digital** group.
- Place the input connectors **SW0**, **SW1**, and **SW2**.
- Place the output connectors **LED0** and **LED1**.
- Wire them as shown:

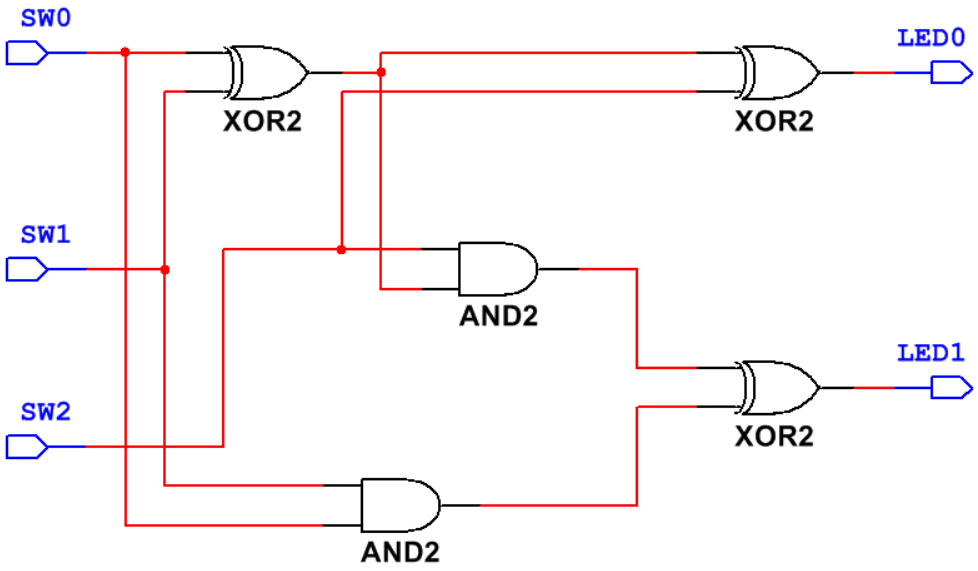


Figure 1-9 A Full Adder Circuit

1-5 Fill out the truth table below.

SW0	SW1	SW2	SUM	C_{out}
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Again, can you see how the truth table represents the sum and carry of the numbers A, B, and C_{IN} added together?

- 0 + 0 + 0 = 0
- 0 + 0 + 1 = 1, with no carry.
- 0 + 1 + 1 = 2, but 2 is not a binary number. In binary, 2 is represented as 10. The 1 is the carry and the 0 is the sum.
- 1 + 1 + 1 = 3. In binary, 3 is represented as 11. The first 1 is the carry and the second 1 is the sum.

Lab Exercise:

- Build the Half-Adder circuit using gates as well as Half-Adder on Multisim, verify the truth table, evaluate the expression of SUM & Carry and attach the picture of the circuit
- Build Full Adder circuit using gates as well as Half-Adder on Multisim, verify the truth table, evaluate the expression of SUM & Carry and attach the picture of the circuit