



AROR UNIVERSITY  
OF ART, ARCHITECTURE,  
DESIGN & HERITAGE,  
SUKKUR, SINDH

## **Faculty of Artificial Intelligence & Multimedia Gaming**

BS – Multimedia Gaming

Digital Logic Design Lab

### **Lab # 09: Multiplexer & Demultiplexer**

Engr. Muhammad Younis

#### **Submission Profile**

Name:

Submission date (dd/mm/yy):

Marks obtained:

Comments:

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Instructor

## Lab Learning Objectives:

Upon successful completion of this experiment, the student will be able:

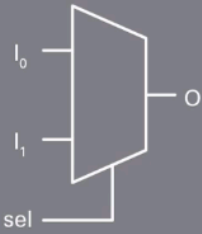
- Reflect on the similarities and differences between encoders and multiplexers
- Examine the function of different Multiplexer and Demultiplexer using logic gates

## Lab Hardware and Software Required:

<i>Platform: NI ELVIS III</i>	<ul style="list-style-type: none"><li>✓ View User Manual: <a href="http://www.ni.com/en-us/support/model.ni-elvis-iii.html">http://www.ni.com/en-us/support/model.ni-elvis-iii.html</a></li><li>✓ View Tutorials: <a href="https://www.youtube.com/playlist?list=PLvcPIuVaUMIWm8ziaSxv0gwtshBA2dh_M">https://www.youtube.com/playlist?list=PLvcPIuVaUMIWm8ziaSxv0gwtshBA2dh_M</a></li></ul>
<i>Software: NI Multisim 14.0.1 Education Version or newer</i>	<ul style="list-style-type: none"><li>✓ Install Multisim: <a href="http://www.ni.com/gate/gb/GB_ACADEMICEVALMULTISIM/US">http://www.ni.com/gate/gb/GB_ACADEMICEVALMULTISIM/US</a></li><li>✓ View Help: <a href="http://www.ni.com/multisim/technical-resources/">http://www.ni.com/multisim/technical-resources/</a></li></ul>

## Background Theory:

### Multiplexers



sel	I <sub>0</sub>	I <sub>1</sub>	O
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Combinational logic circuit

- Inputs = 2 (s)
- Selector inputs = s
- Output = 1

2-1 Multiplexer

- 2 inputs
- 1 output
- Uses SOP

Figure 1-1 Video. View the video here: [https://youtu.be/khmQ-LT\\_Cxg](https://youtu.be/khmQ-LT_Cxg)



Video Summary

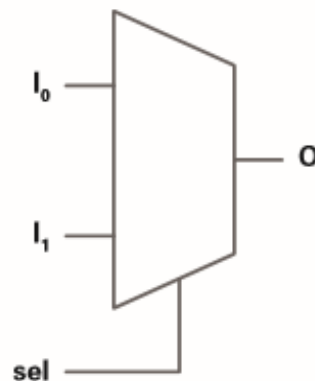
- Multiplexers are combinational logic circuits
- Clock multiplexing is used for operating the same logic function at different clock rates from different sources
- Demultiplexers are combinational logic circuits that have the opposite function of a multiplexer

## Multiplexers

The *multiplexer*, abbreviated *MUX*, is a combinational logic circuit which has multiple data inputs, one or more select inputs and one output.

- It passes the data on one of the inputs, depending on the selection signals, to the output
- With the help of this logic circuit, multiple signals can share the same data output
- Multiplexers have  $2^s$  inputs and  $s$  selector lines, which determine which of the inputs to output.
- Multiplexers are one of the most widely used combinational circuits, their application areas include:
  - o Data routing
  - o Operation sequencing
  - o Parallel-to-serial conversion
  - o Waveform generation

The simplest circuit is the 2-to-1 multiplexer, with the graphical symbol presented in the leftmost figure. Its functionality is described by the joining truth table. The multiplexer below is only 1-bit wide since bit line is connected to a single output bit line.



sel	$I_0$	$I_1$	O
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Figure 1-2 Image of 2-to-1 multiplexer (left) and truth table (right)

The truth table can be simplified to the following truth table for a better understanding of the circuit's operation:

sel	O
0	$I_0$
1	$I_1$

Figure 1-3 Simplified truth table

Using the sum-of-products Boolean function gives the following combinational logic circuit:

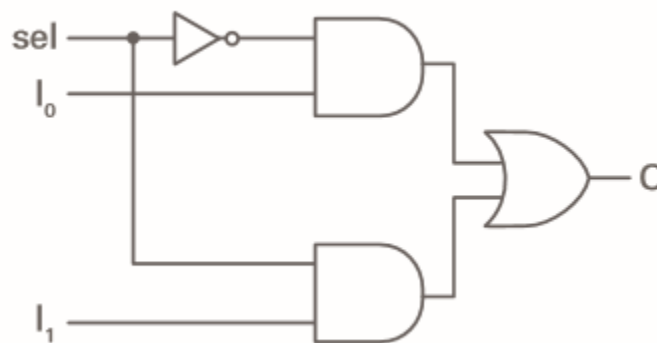


Figure 1-4 Combinational logic circuit

*Clock multiplexing* is a technique used for operating the same logic function at different clock rates, from different sources (inputs).

- The logic circuits are switched by the select signal often while the circuit is running
- This process of switching isn't very safe and can result in a glitch that occurs when one signal is going down as the other is going up.
- Clock safe switches can be implemented to eliminate glitches.

## Demultiplexers

*Demultiplexers (DEMUX)* have the opposite function of a multiplexer

- It places the value of a single data input on several data outputs depending on a selection signal
- Usually demultiplexers have  $s$  select inputs and  $2^s$  outputs
- Since demultiplexers take one input and connect it to many outputs, some of their uses are for communication (two-way communication usually includes both multiplexers and demultiplexers) and for serial to parallel converters

- The graphical symbol for a 1-to-4 demultiplexer is shown below (left) as well as the corresponding 1-to-4 DEMUX truth table (centre) and the CLC (right)

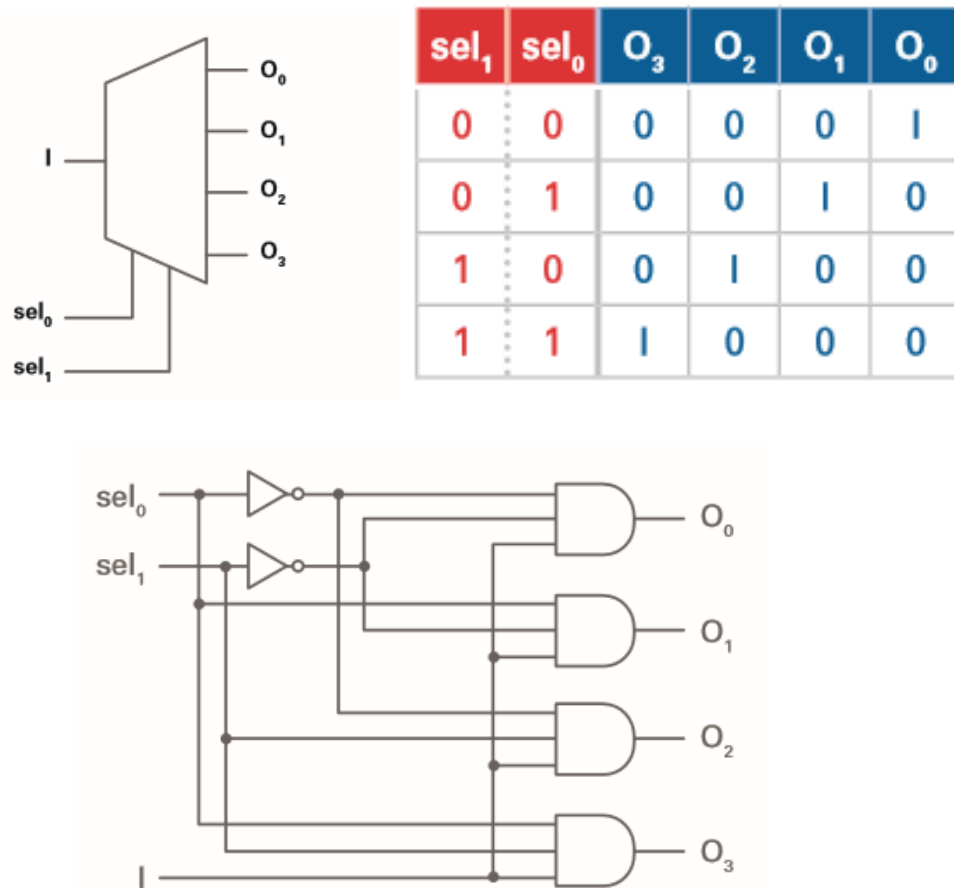


Figure 1-5 Demultiplexer (top left), truth table (top center) and CLC (bottom)

## Lab Activities:

### 4-to-1 MUX

Using the following truth table (right) to describe the behavior of a 4-to-1 MUX (left), design and implement the corresponding circuit in multisim.

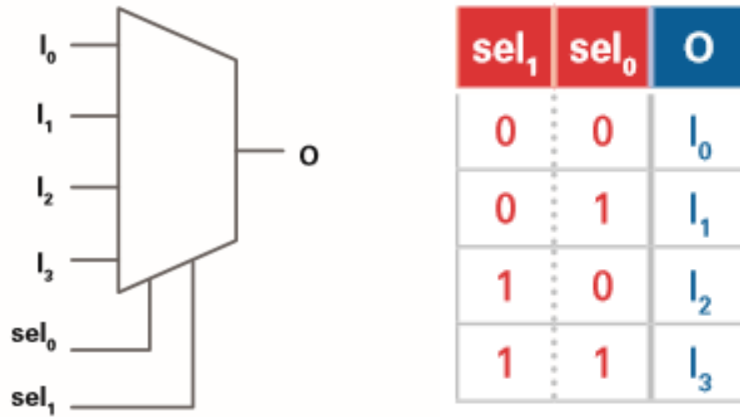


Figure 1-8 Image of 4-to-1 MUX (left) and truth table (right)

## 1-to-4 Demultiplexer

In simulation build and run the following 1-to-4 demultiplexer

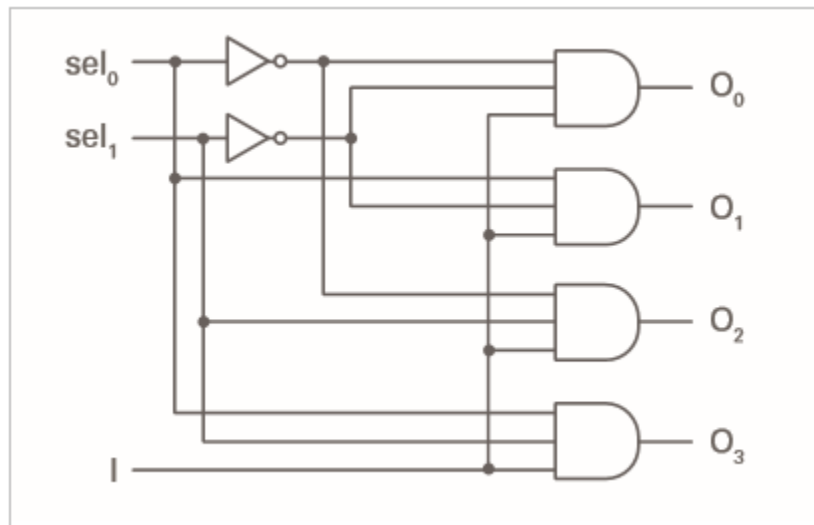


Figure 1-9 Image of 1-to-4 demultiplexer

### Lab Exercise:

- ☐ Implement 4 to 1 multiplexer circuit on **NI-ELVIS II** using 74HC153/74LS153
- ☐ Implement 1 to 4 de-multiplexer circuit on **NI-ELVIS II** using 74HC155/74LS155

1-1 Write the sum-of-products Boolean functions for the 4-to-1 Multiplexer:

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1-2 Write the sum-of-products Boolean functions for the 1-to-4 Demultiplexer:

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1-3 What is the function of the Selector (Sel) in Multiplexers and Demultiplexers?

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## 1.2 74LS153 MULTIPLEXER IC:

The TTL 74LS153 Multiplexer IC has two 4-input multiplexers. It has two selection inputs which act on both selectors, two enabling inputs which must be usually low, four inputs for each channel, and two outputs.

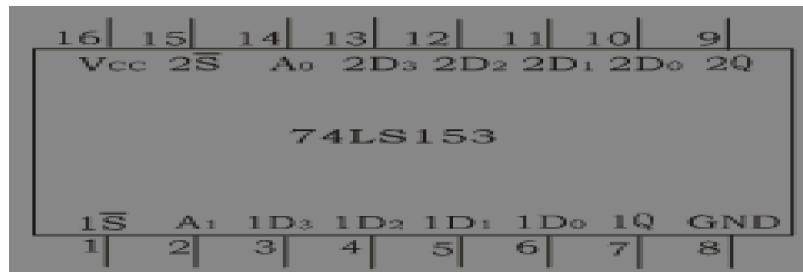


Figure 1-6 Pin diagram

## 1.3 74LS155 DE-MULTIPLEXER IC:

The TTL 74LS155 is a-output De-multiplexer. Inside it has two identical decoding circuits, from 1 to 4 lines, with individual strobe commands (inhabitation) and common inputs of the binary addresses. The individual strobes enable the activation or inhabitation of each of the two 4-bit sections. The data across the input IC appear inverted across the output, while the data across 2C is not inverted.

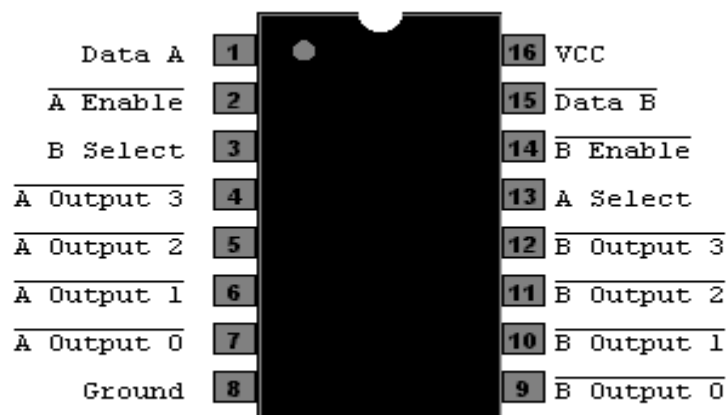


Figure 1-7 Pin Diagram