NAND VS NOR

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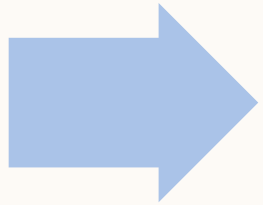
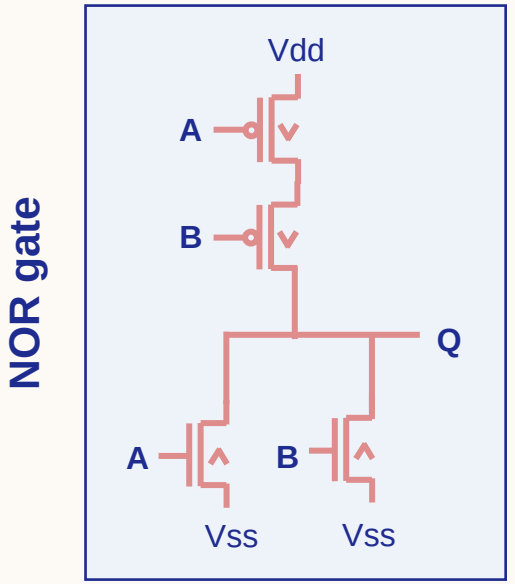
NOR GATE

To start building more complex logic using transistors, we need to think about building 2 pathways with CMOS transistors; one using p-type transistors that'll define when the *Vdd* signal should be connected to the output and the other using n-type transistors that'll define when the *Vss* signal should be connected to the output.

A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0



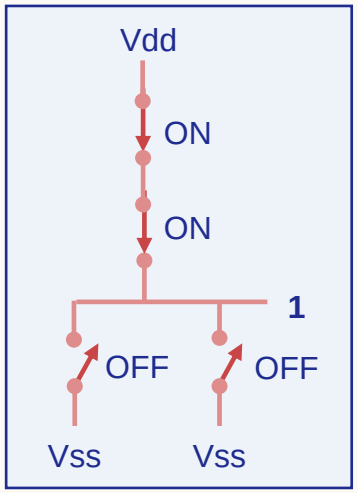


To build this NOR gate, we used p-type transistors in **series** to connect the *Vdd* signal, which means both A *and* B must be 0 to complete this connection. Whereas n-type transistors are used in **parallel** to connect the *Vss* signal, which means A *or* B must be 1 to complete this connection.

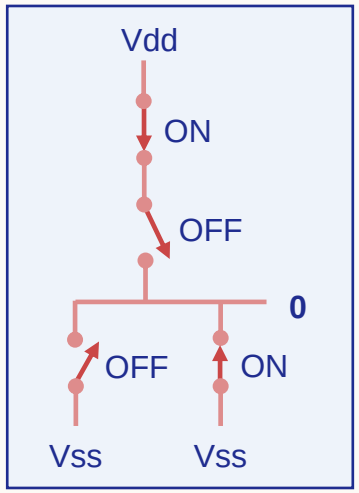
NOR LOGIC

If we look at this NOR transistor circuit design in more detail, we can explore the behaviour of each transistor i.e. whether it's ON or OFF, and how this affects the output…

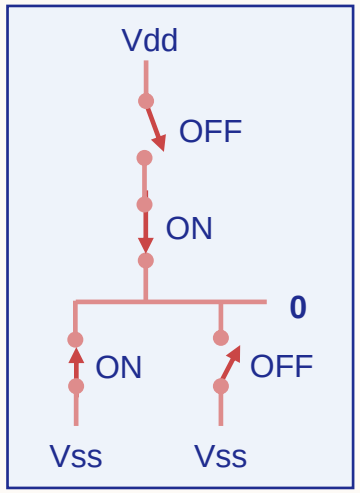
A = 0, B = 0



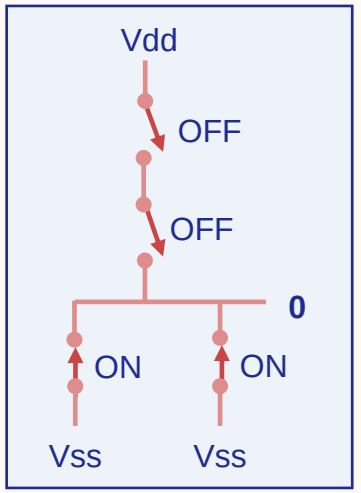
A = 0, B = 1



A = 1, B = 0



A = 1, B = 1

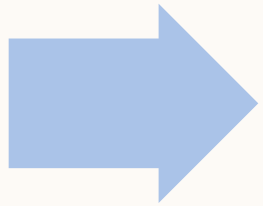


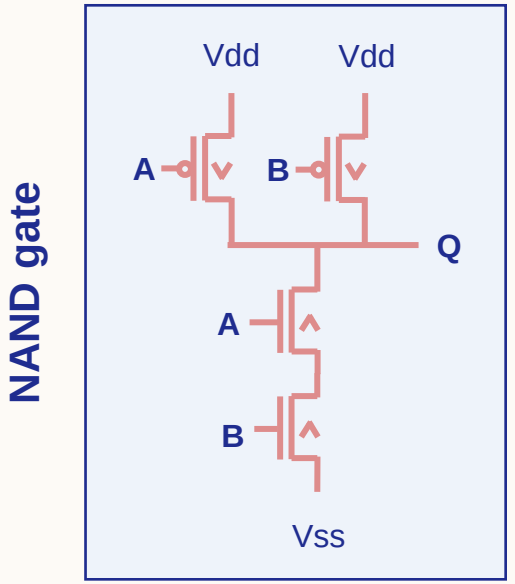
We can see the pathways connecting *Vss* and *Vdd* are **complementary** as exactly one pathway will create a complete conductive channel at any one time – we want our output to always be *either* 0 or 1!

NAND GATE

Using a similar process to the NOR gate, we need to think about exactly when we want the output to be connected to the *Vdd* signal and exactly when we want the output to be connected to the *Vss* signal…

A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0



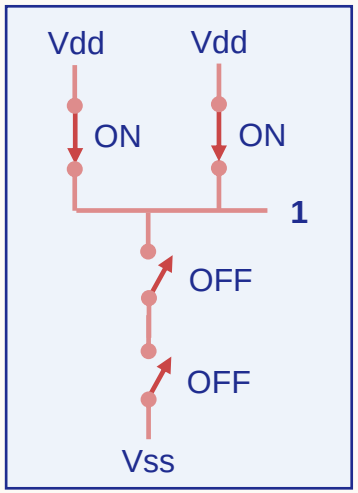


To build this NAND gate, we used p-type transistors in **parallel** to connect the *Vdd* signal, which means A *or* B must be 0 to complete this connection. Whereas n-type transistors are used in **series** to connect the *Vss* signal, which means both A *and* B must be 1 to complete this connection.

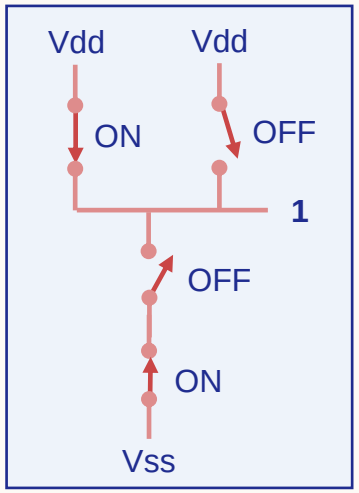
NAND LOGIC

Again, if we look at this NAND transistor circuit design in more detail, we can explore the behaviour of each transistor i.e. whether it's ON or OFF, and how this affects the output…

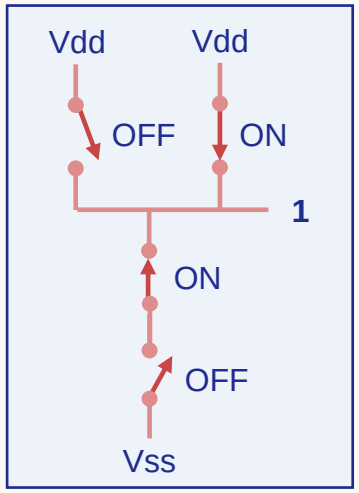
A = 0, B = 0



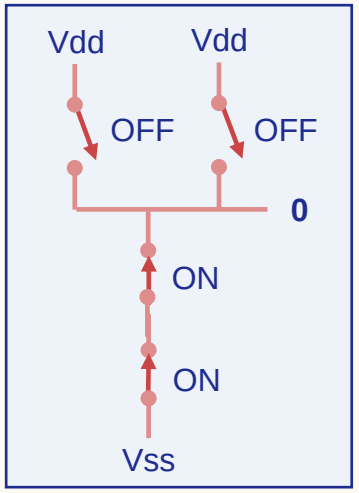
A = 0, B = 1



A = 1, B = 0



A = 1, B = 1



If both NAND and NOR gates use a similar transistor design (2 transistors in parallel and 2 transistors in series), then why has NAND become the industry standard..?

STRUCTURAL SPEED

Transistors in series are slower than transistors in parallel, as the electrical current has to pass through 2 transistors before reaching the output. Moreover, p-type transistors are slower than n-type transistors because holes cannot move around the silicon lattice as fast as electrons.

Therefore, the NOR design is considered **structurally slower** than the NAND design as, even though the *Vss* signal is passed through n-type transistors in series (the fastest option), the *Vdd* signal is passed through p-type transistors in parallel – the slowest option!

NAND is therefore the preferential gate in industry as they have a shorter **critical path** (the path between the input and output that has the longest delay), which can slow down the switching speed.