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	Name	Initials	Date	Title:		
Drawn	Peter Konecny	PK	13/04/2022	Interface between eurorack CV and Monotron		
Chkd				Document No:	Rev:	Sheet of
Approved				CV_MONOTRON-002	2	1/3

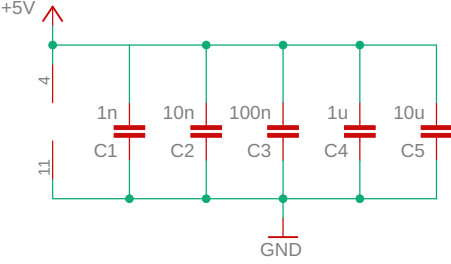
# Eurorack-monotron interface

R20 trimming range worst case:  
min:  $47 \cdot 101\% / (47 \cdot 101\% + 10 \cdot 90\% + 110 \cdot 99\%) = 0.287$   
max:  $(47 \cdot 99\% + 10 \cdot 90\%) / (47 \cdot 99\% + 10 \cdot 90\% + 110 \cdot 101\%) = 0.333$   
for 5V: Vmin = 1.435V; Vmax = 1.666V

R19 Trimming range worst case:  
min:  $39.8 \cdot 101\% / (39.8 \cdot 101\% + 10 \cdot 90\% + 50.3 \cdot 99\%) = 0.406$   
max:  $(39.8 \cdot 99\% + 10 \cdot 90\%) / (39.8 \cdot 99\% + 10 \cdot 90\% + 50.3 \cdot 101\%) = 0.488$

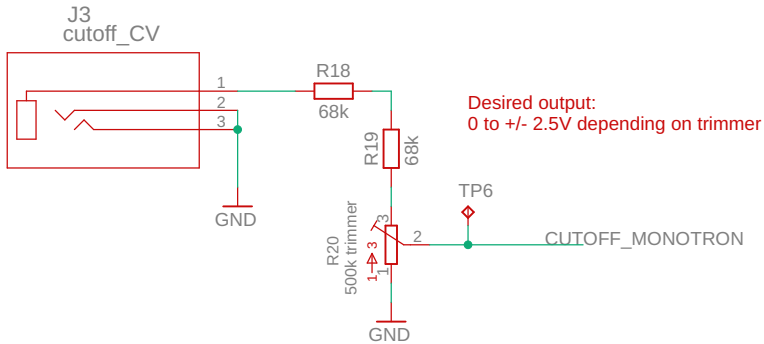
R15, R16 values:  
a) voltage divider so that 12V  
from gate is scaled down to max 5V:  
 $33/80 \cdot 12V = 4.95V$   
(not taking into account output impedance of gate signal source)  
b) 0R for LM324

Do not place JACKS too close to each other,  
as the connectors are wider than the plugs and might not fit



README:  
Both gate and pitch testpads on monotron enter a summing op-amp, which controls the VCO.  
However, the pitch itself does not trigger the VCO enable, while the gate does.  
The gate starts triggering at about 1.4V and C0 is generated when 1.56V is applied and then its 0.44V/oct.  
Eurorack voltages are 1V/oct so we need to scale it down to 0.44V/oct and offset it by 1.56V for the lowest note.  
Moreover, to prevent gate being triggered when note is not playing, the external gate\_cv controls a transistor Q1,  
turning it on when the note is OFF. By turning Q1 ON, the transistor pulls the + junction of the summing op-amp to 0,  
resulting in the output being 0 as well, which disables the monotron VCO, because its less than 1.4V,

The cutoff\_monotron signal connects to a summing op-amp in Monotron.  
The internal cutoff signal enters the op-amp through 68k resistor  
so doubling the value to 2\*68k will reduce the incoming signal effect by 2.  
However, it is important to measure the internal cutoff signal to see its magnitude,  
then choose R17, R18 to scale external signal accordingly.  
500k trimmer for attenuation control.

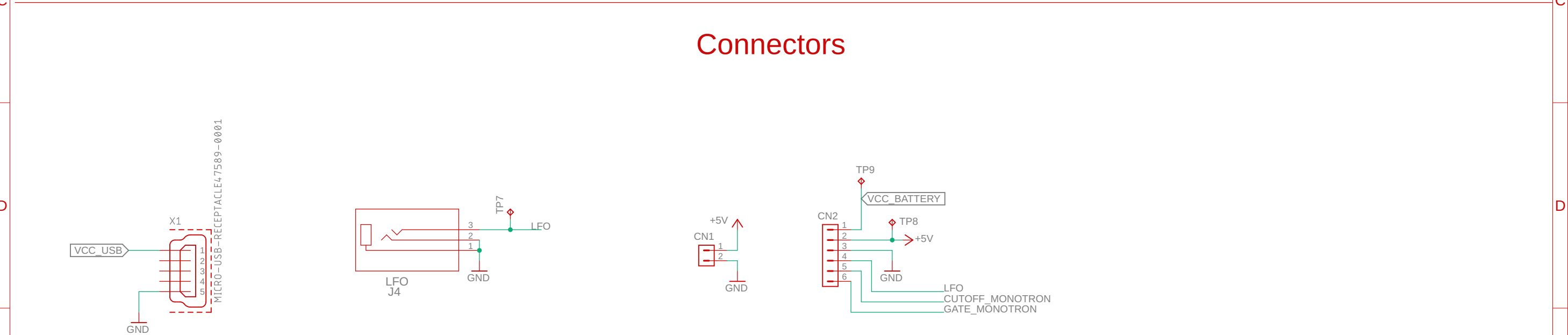


All resistors must be at least 1% accuracy  
All capacitors should be rated atleast 5V  
unless stated otherwise

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## Power management

The diagram illustrates a power management circuit centered around the U1 TPS2105D IC. The IC has several pins: EN (pin 3), IN2 (pin 1), IN1 (pin 5), GND (pin 2), OUT\_2 (pin 7), OUT (pin 8), NC\_2 (pin 4), and NC (pin 6). The circuit includes three input voltage sources: VCC\_USB, VCC\_BATTERY, and another VCC\_USB. A 10k resistor is connected between the top VCC\_USB and GND. A 220nF capacitor (C6) is connected between VCC\_BATTERY and GND. Another 220nF capacitor (C7) is connected between the bottom VCC\_USB and GND. The EN pin (pin 3) is connected to the top VCC\_USB. The IN2 pin (pin 1) is connected to VCC\_BATTERY. The IN1 pin (pin 5) is connected to the bottom VCC\_USB. The GND pin (pin 2) is connected to a common ground. The OUT\_2 pin (pin 7) and OUT pin (pin 8) are connected to a common output node. This node is connected to a series of capacitors: C8 (1uF), C9 (47uF), C10 (47uF), C11 (47uF), and C12 (47uF). The output of this capacitor chain is labeled +5V and is connected to a +5V output terminal. The NC\_2 pin (pin 4) and NC pin (pin 6) are connected to a common ground.



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