EXPERIMENT NO.4

COMBINATIONAL CIRCUIT DESIGN USING K-MAPS

SUBMITTED TO:

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SUBMITTED BY:

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2022-EE-176

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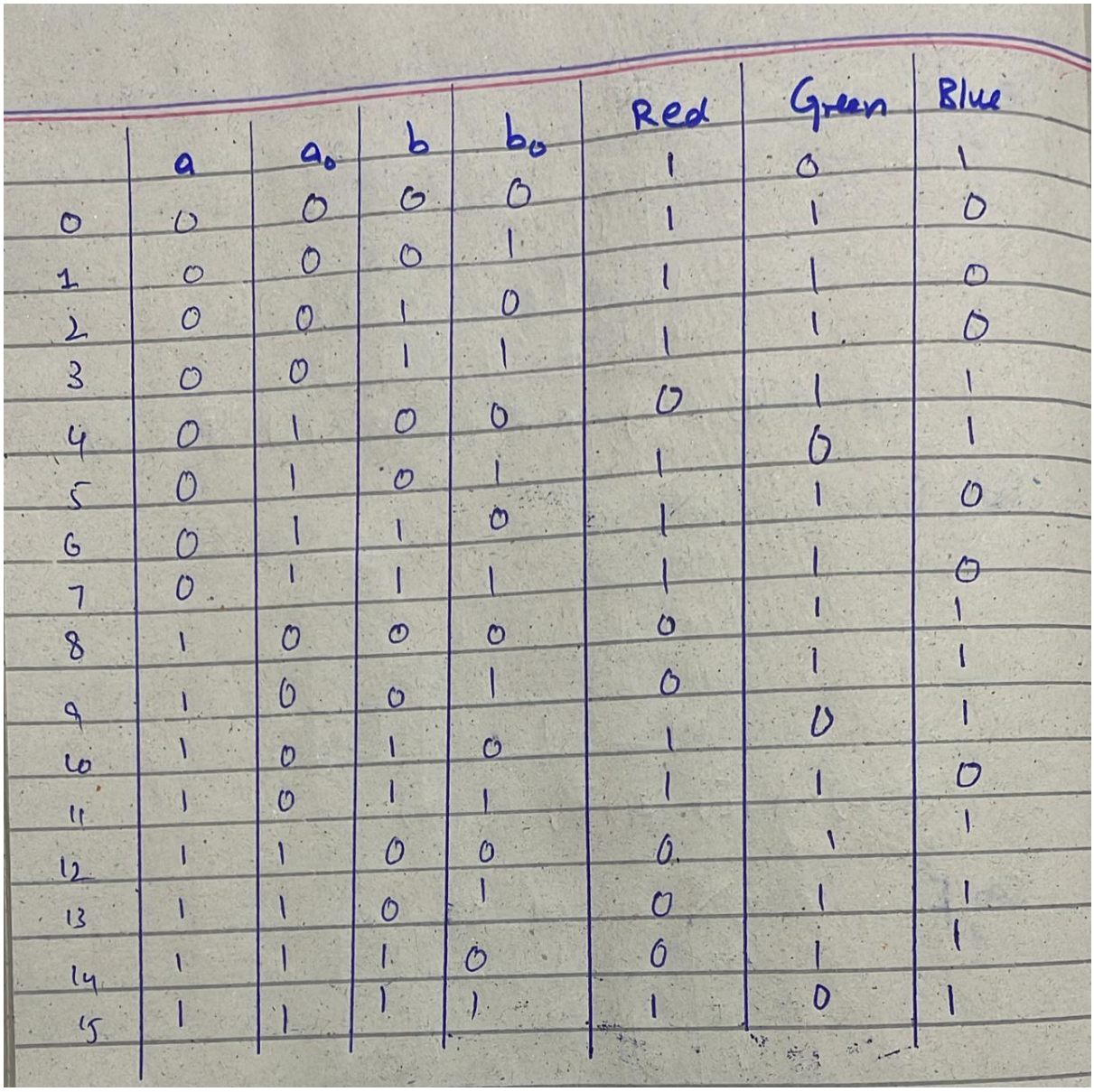
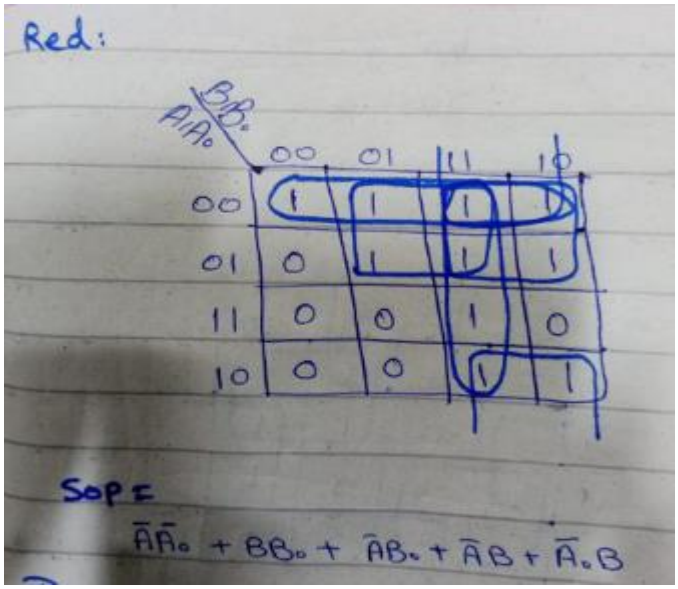
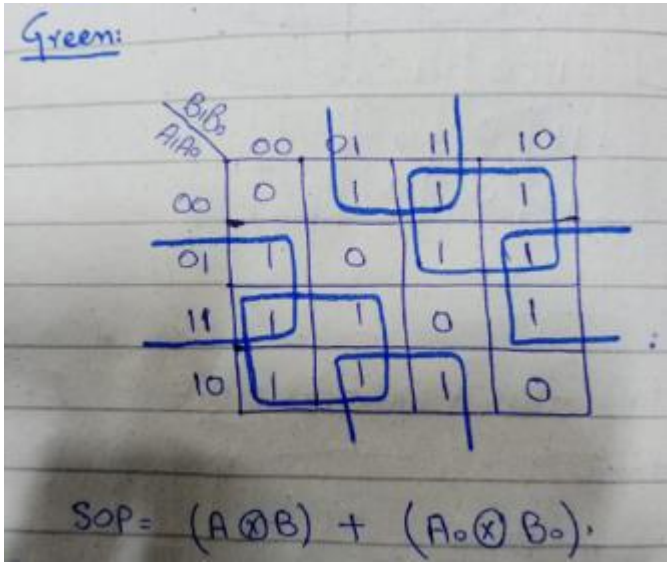
Truth Table:

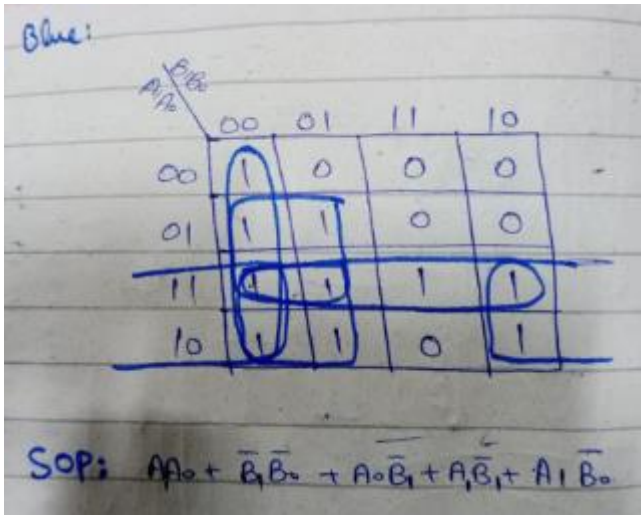


	a	a_0	b	b_0	Red	Green	Blue
0	0	0	0	0	1	0	1
1	0	0	0	1	1	1	0
2	0	0	1	0	1	1	0
3	0	0	1	1	1	1	0
4	0	1	0	0	0	1	1
5	0	1	0	1	1	0	1
6	0	1	1	0	1	1	0
7	0	1	1	1	1	1	0
8	1	0	0	0	0	1	1
9	1	0	0	1	0	1	1
10	1	0	1	0	1	0	1
11	1	0	1	1	1	1	0
12	1	1	0	0	0	1	1
13	1	1	0	1	0	1	1
14	1	1	1	0	0	1	1
15	1	1	1	1	1	0	1

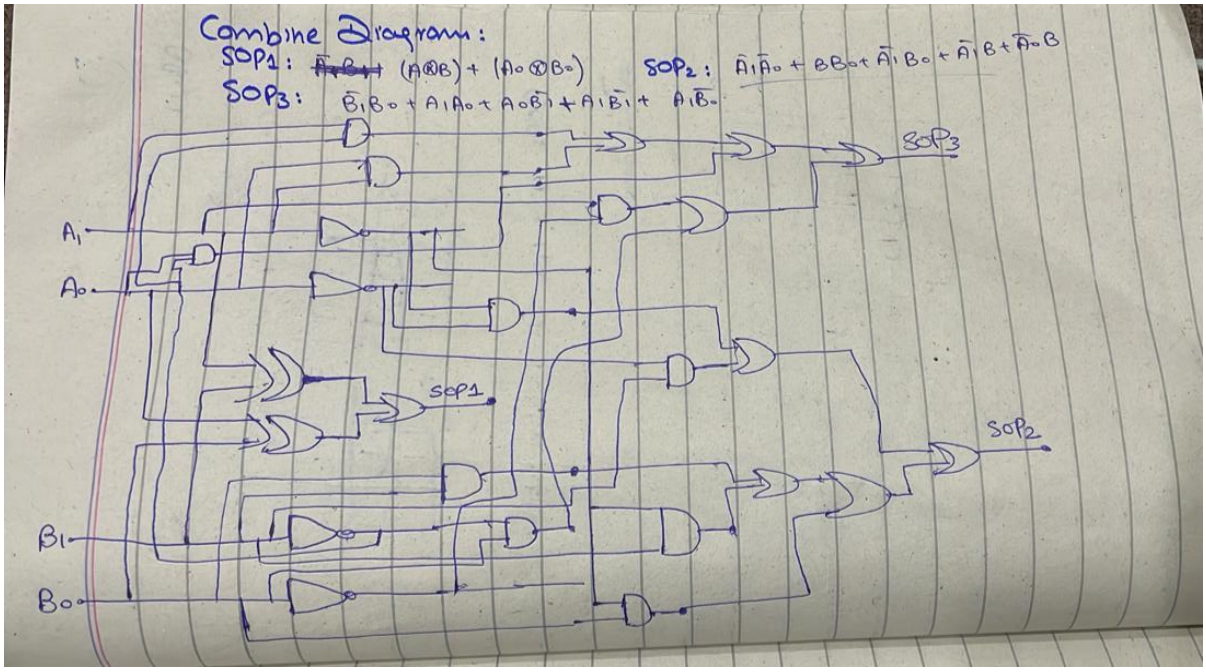
K-maps:


Red:
SOP =
$\bar{A}\bar{A}_0 + BB_0 + \bar{A}B_0 + \bar{A}B + \bar{A}_0B$

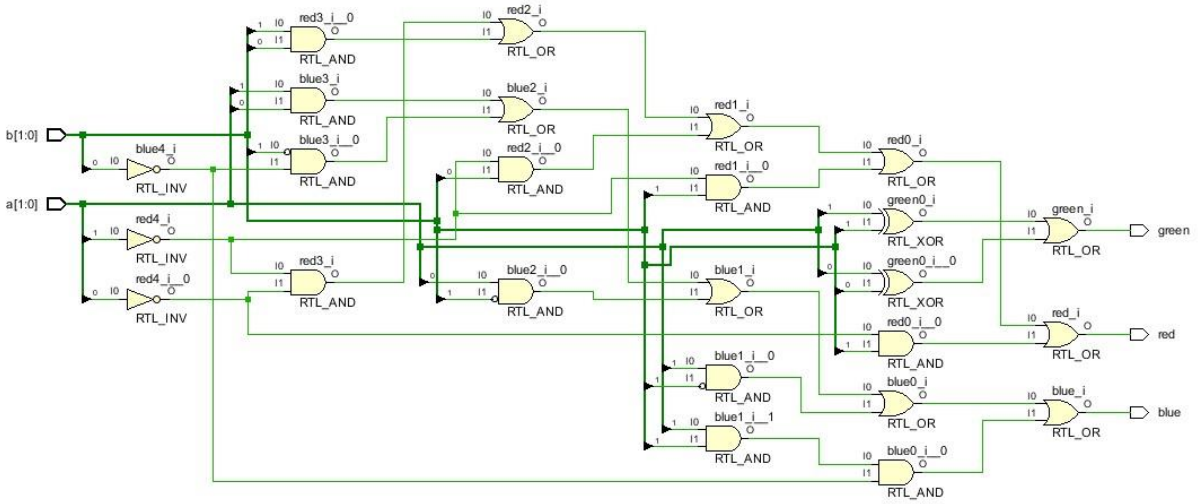

Green:
SOP = $(A \otimes B) + (A_0 \otimes B_0)$.


Blue:
SOP: $AA_0 + \bar{B}_1\bar{B}_0 + A_0\bar{B}_1 + A_1\bar{B}_1 + A_1\bar{B}_0$

Circuit Diagram:



Circuit diagram using vivado:



Delay in synthesis:

Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	2	3	b[1]	green	6.780	5.174	1.606	∞	input port clock
Path 2	∞	3	2	3	b[1]	blue	6.749	5.143	1.606	∞	input port clock
Path 3	∞	3	2	3	b[1]	red	6.739	5.133	1.606	∞	input port clock

Resource Utilization:

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	2	0	63400	<0.01
LUT as Logic	2	0	63400	<0.01
LUT as Memory	0	0	19000	0.00
Slice Registers	0	0	126800	0.00
Register as Flip Flop	0	0	126800	0.00
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

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F8 Muxes	0	0	15850	0.00

7. Primitives

Ref Name	Used	Functional Category
IBUF	4	IO
OBUF	3	IO
LUT4	3	LUT

System Verilog Code:

C: > Users > sa > Desktop > lab4_srct1.sv

```
module lab4_srct1(
    input logic [1:0] a,b,
    output logic red, green, blue
    );
    assign red=(~a[1]&~a[0])|(b[1]&b[0])|(~a[1]&b[0])|(~a[1]&b[1])|(~a[0]&b[1]);
    assign green=(a[1]^b[1])|(a[0]^b[0]);
    assign blue=(a[1]&a[0])|(~b[1]&~b[0])|((a[0])&(~b[1]))|((a[1])&(~b[1]))|((a[1]&b[1])&(~b[0]));

endmodule
```