EXPERIMENT NO.5

COMBINATIONAL CIRCUIT DESIGN USING K-MAPS

SUBMITTED TO:

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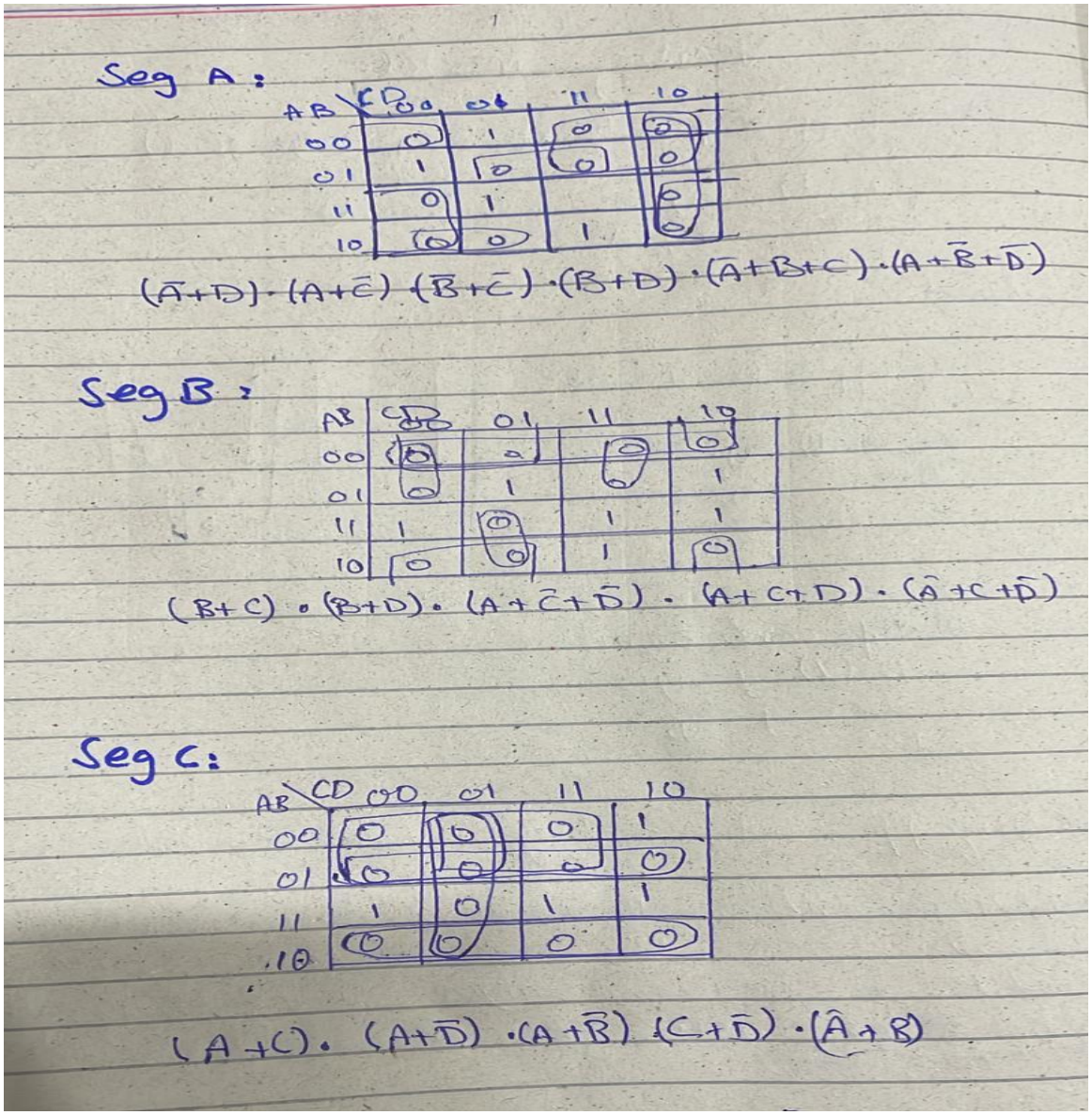
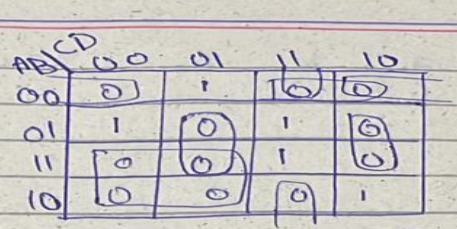
Truth Table:

charachters	A2	A1	A0	an. 0	an. 1	an. 2	an.3	an.4	an.5	an.6	an.7
0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	0	1	1	1	1	1	1
2	0	1	0	1	1	0	1	1	1	1	1
3	0	1	1	1	1	1	0	1	1	1	1
4	1	0	0	1	1	1	1	0	1	1	1
5	1	0	1	1	1	1	1	1	0	1	1
6	1	1	0	1	1	1	1	1	1	0	1
7	1	1	1	1	1	1	1	1	1	1	0

K-maps:

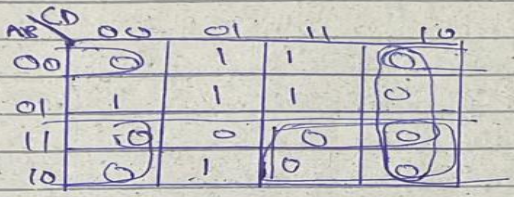


Seg D



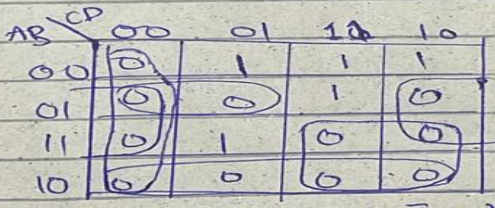
$(\bar{A}+C)\cdot(\bar{B}+C+D)\cdot(A+B+D)\cdot(B+\bar{C}+\bar{D})\cdot(\bar{B}+\bar{C}+D)$

Seg E



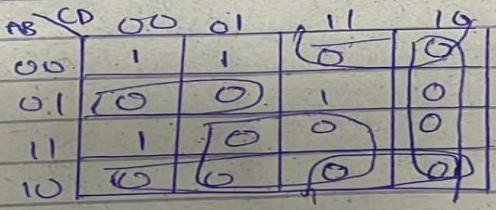
$(B+D)\cdot(\bar{A}+\bar{C})\cdot(\bar{A}+\bar{B})\cdot(\bar{C}+D)$

Seg F



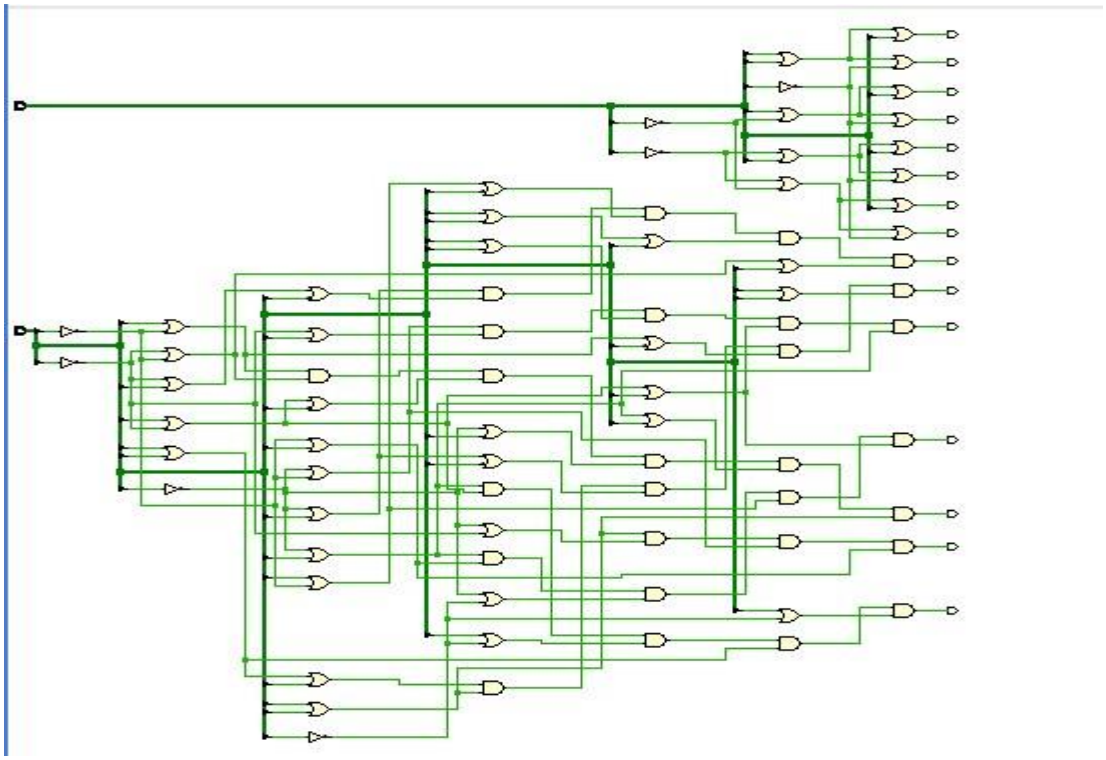
$(\bar{A}+\bar{C})\cdot(\bar{B}+D)\cdot(C+D)\ (A+\bar{B}+C)\cdot(\bar{A}+B)$

Seg G



$(\bar{A}+B)\cdot(\bar{C}+D)\cdot(\bar{A}+D)\cdot(B+\bar{C})\cdot(A+\bar{B}+C)$

Circuit diagram using Vivado:



Delay in Synthesis:

Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	2	8	b[0]	an_2	6.836	5.230	1.606	∞	input port clock
Path 2	∞	3	2	8	b[2]	an_3	6.805	5.199	1.606	∞	input port clock
Path 3	∞	3	2	8	b[2]	an_7	6.804	5.199	1.606	∞	input port clock
Path 4	∞	3	2	7	a[1]	seg_f	6.798	5.192	1.606	∞	input port clock
Path 5	∞	3	2	7	a[1]	seg_b	6.792	5.187	1.606	∞	input port clock
Path 6	∞	3	2	7	a[1]	seg_a	6.792	5.186	1.606	∞	input port clock
Path 7	∞	3	2	8	b[0]	an_5	6.789	5.184	1.606	∞	input port clock
Path 8	∞	3	2	8	b[0]	an_4	6.788	5.182	1.606	∞	input port clock
Path 9	∞	3	2	7	a[3]	seg_d	6.784	5.178	1.606	∞	input port clock
Path 10	∞	3	2	8	b[0]	an_6	6.779	5.173	1.606	∞	input port clock

Delay in Implementation:

Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	2	8	b[1]	an_6	11.080	5.339	5.741	∞	input port clock
Path 2	∞	3	2	7	a[2]	seg_a	10.407	5.414	4.993	∞	input port clock
Path 3	∞	3	2	7	a[2]	seg_b	10.150	5.159	4.991	∞	input port clock
Path 4	∞	3	2	8	b[1]	an_7	10.114	5.400	4.714	∞	input port clock
Path 5	∞	3	2	8	b[1]	an_2	10.110	5.192	4.917	∞	input port clock
Path 6	∞	3	2	8	b[1]	an_3	9.927	5.406	4.521	∞	input port clock
Path 7	∞	3	2	7	a[2]	seg_f	9.832	5.397	4.434	∞	input port clock
Path 8	∞	3	2	8	b[1]	an_0	9.649	5.382	4.268	∞	input port clock
Path 9	∞	3	2	7	a[3]	seg_d	9.623	5.382	4.241	∞	input port clock
Path 10	∞	3	2	7	a[2]	seg_e	9.298	5.137	4.161	∞	input port clock

Resource Utilization:

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	22	0	210	10.48
Bonded IPADs	0	0	2	0.00
PHY_CONTROL	0	0	6	0.00
PHASER_REF	0	0	6	0.00
OUT_FIFO	0	0	24	0.00
IN_FIFO	0	0	24	0.00
IDELAYCTRL	0	0	6	0.00
IBUFDS	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	300	0.00
ILOGIC	0	0	210	0.00
OLOGIC	0	0	210	0.00

7. Primitives

Ref Name	Used	Functional Category
OBUF	15	IO
LUT3	8	LUT
LUT4	7	LUT
IBUF	7	IO

System Verilog Code:

```
module lab5source(
    input logic [3:0] a,
    input logic [2:0] b,
    output logic seg_a,seg_b,seg_c,seg_d,seg_e,seg_f,seg_g,
    output logic an_0,an_1,an_2,an_3,an_4,an_5,an_6,an_7
    );
    assign seg_a=(a[3]|~a[1]) & (~a[2]|~a[1]) & (a[3]|~a[2]|~a[0]) & (~a[3]|a[0]) & (~a[3]|a[2]|a[1])  & (a[2]|a[0]);
    assign seg_b=(a[3]|a[1]|a[0]) & (a[2]|a[0]) & (~a[3]|a[1]|~a[0]) & (a[3]|~a[1]|~a[0]) & (a[2]|a[1]);
    assign seg_c=(~a[3]|a[2]) & (a[3]|~a[2]) & (a[3]|~a[0]) & (a[3]|a[1]) & (a[1]|~a[0]);
    assign seg_d=(~a[3]|a[1]) & (~a[2]|a[1]|~a[0]) & (a[2]|~a[1]|~a[0]) & (a[3]|a[2]|a[0]) & (~a[2]|~a[1]|a[0]);
    assign seg_e=(a[2]|a[0]) & (~a[3]|~a[2]) & (~a[3]|~a[1]) & (~a[1]|a[0]);
    assign seg_f=(~a[3]|~a[1]) & (~a[2]|a[0]) & (a[1]|a[0]) & (a[3]|~a[2]|a[1]) & (~a[3]|a[2]);
    assign seg_g=(~a[3]|a[2]) & (~a[1]|a[0]) & (~a[3]|~a[0]) & (a[2]|~a[1]) & (a[3]|~a[2]|a[1]);

    assign an_0= b[2]|b[1]|b[0];
    assign an_1= b[2]|b[1]|~b[0];
    assign an_2= b[2]|~b[1]|b[0];
    assign an_3= b[2]|~b[1]|~b[0];
    assign an_4= ~b[2]|b[1]|b[0];
    assign an_5= ~b[2]|b[1]|~b[0];
    assign an_6= ~b[2]|~b[1]|b[0];
    assign an_7= ~b[2]|~b[1]|~b[0];

endmodule
```