Experiment # 3

Submitted To:

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Submitted By:

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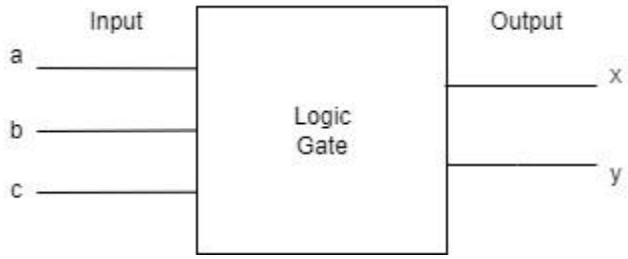
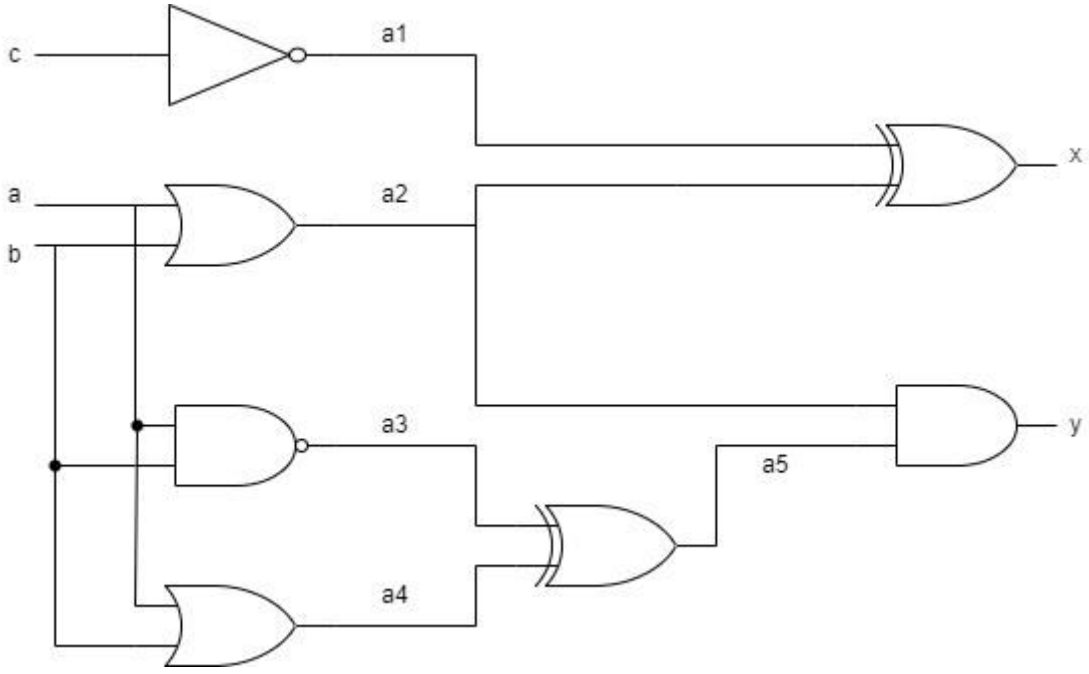
Digital System

Number of Inputs and outputs:



Circuit Diagram:



Q#1:

Truth Table:

a	b	c	a1	a2	a3	a4	a5	x	Y
0	0	0	1	0	1	0	1	1	0
0	0	1	0	0	1	0	1	0	0
0	1	0	1	1	1	1	0	0	0
0	1	1	0	1	1	1	0	1	0
1	0	0	1	1	1	1	0	0	0
1	0	1	0	1	1	1	0	1	0
1	1	0	1	1	0	1	1	0	1
1	1	1	0	1	0	1	1	1	1

Q#2:

Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	2	1	c	x	8.773	5.130	3.643	∞	input port clock
Path 2	∞	3	2	2	b	y	8.327	5.335	2.992	∞	input port clock

Q#3:

```
module source(
    output logic x,y,

    input logic a,b,c

    );
    wire k,l,f,m,h;
    not k1(a1,c);
    or k2(a2,a,b);
    nand k3(a3,a,b);
    or k4(a4,a,b);
    xor k5(a5,f,m);
    xor k6(x,a1,a2);
    and k7(y,a2,a5);


endmodule
```

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	1	0	63400	<0.01
LUT as Logic	1	0	63400	<0.01
LUT as Memory	0	0	19000	0.00
Slice Registers	0	0	126800	0.00
Register as Flip Flop	0	0	126800	0.00
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	5	0	210	2.38

Primitives

Ref Name	Used	Functional Category
IBUF	3	IO
OBUF	2	IO
LUT3	1	LUT
LUT2	1	LUT