TABLE 5-6 Control Functions and Microoperations for the Basic Computer

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Fetch
                                  R'T_0:
                                               AR \leftarrow PC
                                  R'T_1:
                                              IR \leftarrow M[AR], PC \leftarrow PC + 1
Decode
                                  R'T_2:
                                              D_0, \ldots, D_7 \leftarrow \text{Decode } IR(12-14),
                                              AR \leftarrow IR(0-11), I \leftarrow IR(15)
Indirect
                                 D_7^{\prime}IT_3:
                                               AR \leftarrow M[AR]
Interrupt:
    T_0'T_1'T_2'(IEN)(FGI + FGO):
                                              R \leftarrow 1
                                   RT_0:
                                              AR \leftarrow 0, TR \leftarrow PC
                                   RT_1:
                                              M[AR] \leftarrow TR, PC \leftarrow 0
                                              PC \leftarrow PC + 1, IEN \leftarrow 0, R \leftarrow 0, SC \leftarrow 0
                                   RT_2:
Memory-reference:
   AND
                                  D_0T_4:
                                              DR \leftarrow M[AR]
                                  D_0T_5:
                                              AC \leftarrow AC \land DR, SC \leftarrow 0
   ADD
                                  D_1T_4:
                                              DR \leftarrow M[AR]
                                  D_1T_5:
                                              AC \leftarrow AC + DR, E \leftarrow C_{out}, SC \leftarrow 0
  LDA
                                  D_2T_4:
                                              DR \leftarrow M[AR]
                                              AC \leftarrow DR, SC \leftarrow 0
                                  D_2T_5:
  STA
                                              M[AR] \leftarrow AC, SC \leftarrow 0
                                  D_3T_4:
  BUN
                                  D_4T_4:
                                              PC \leftarrow AR, SC \leftarrow 0
                                                                                           suggest to break these two microoperations
  BSA
                                  D_5T_4:
                                              M[AR] \leftarrow PC, \quad AR \leftarrow AR + 1
                                                                                           into separate steps. BSA will take T4..T6
                                  D_5T_5:
                                              PC \leftarrow AR, SC \leftarrow 0
  ISZ
                                  D_6T_4:
                                              DR \leftarrow M[AR]
                                  D_6T_5:
                                              DR \leftarrow DR + 1
                                  D_6T_6:
                                              M[AR] \leftarrow DR, if (DR = 0) then (PC \leftarrow PC + 1), SC \leftarrow 0
Register-reference:
                                  D_7I'T_3 = r (common to all register-reference instructions)
                                  IR(i) = B_i (i = 0, 1, 2, ..., 11)
                                       r:
                                              SC \leftarrow 0
  CLA
                                   rB_{11}:
                                              AC \leftarrow 0
  CLE
                                              E \leftarrow 0
                                   rB_{10}:
                                              AC \leftarrow \overline{AC}
  CMA
                                    rB_9:
  CME
                                    rB_8:
                                              E \leftarrow \overline{E}
  CIR
                                    rB_7:
                                              AC \leftarrow \operatorname{shr} AC, AC(15) \leftarrow E, E \leftarrow AC(0)
  CIL
                                    rB_6:
                                              AC \leftarrow \text{shl } AC, \quad AC(0) \leftarrow E, \quad E \leftarrow AC(15)
  INC
                                    rB_5:
                                              AC \leftarrow AC + 1
  SPA
                                              If (AC(15) = 0) then (PC \leftarrow PC + 1)
                                    rB_4:
  SNA
                                              If (AC(15) = 1) then (PC \leftarrow PC + 1)
                                    rB_3:
  SZA
                                    rB_2:
                                              If (AC = 0) then PC \leftarrow PC + 1
  SZE
                                    rB_1:
                                              If (E = 0) then (PC \leftarrow PC + 1)
  HLT
                                    rB_0:
                                              S \leftarrow 0
Input-output:
                                  D_7IT_3 = p (common to all input-output instructions)
                                  IR(i) = B_i (i = 6, 7, 8, 9, 10, 11)
                                              SC \leftarrow 0
                                      p:
  INP
                                              AC(0-7) \leftarrow INPR, FGI \leftarrow 0
                                  pB_{11}:
  OUT
                                  pB_{10}:
                                              OUTR \leftarrow AC(0-7), FGO \leftarrow 0
                                              If (FGI = 1) then (PC \leftarrow PC + 1)
  SKI
                                   pB_9:
  SKO
                                   pB_8:
                                              If (FGO = 1) then (PC \leftarrow PC + 1)
  ION
                                              IEN \leftarrow 1
                                   pB_7:
  IOF
                                              IEN \leftarrow 0
                                   pB_6:
```