ULTRA LOW POWER Full Custom 4-Bit ALU DESIGN

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***Abstract*–This paper proposes an ultra-low power Arithmetic Logic Unit in the context of heart rate sensor applications. Several optimizations were handled on some of the ALU 5 main blocks, which are the Adder, Shifter, Comparator, Logic unit, and the Final Multiplexer blocks. The obtained results were as follows: an average power of 0.664 µW and a worst case delay of 323 ps.**

I. Introduction

Vitals reading applications are increasingly being used for practical purposes such as monitoring health levels for athletes, regular medical checkups and health regulation, and so on. To broaden the range of applications of vital sensors, Formula one (F1) drivers nowadays wear a glove that monitors many of their health aspects to ensure drivers safety.

Since the sensor is battery operated, it is crucial to ensure that they complete their required mission for a long time without any battery outage that can definitely lead to disasters if there is a health problem that is not monitored. For this, it has to be a very low power application and since the sensor incorporates a microcontroller which has two main components: the Arithmetic Logic Unit (ALU) and the Control Unit (CU), it is crucial to design a low power ALU.

In this paper, we propose a new ALU architecture supporting 16 operations, which are Add, Add with Carry, Subtract, Subtract with borrow, 1's complement, 2's complement, Increment, Decrement, Shift right, Shift left, Rotate right, Rotate left, AND, OR, XOR, and compare. This ALU is optimized for low power applications as discussed below, and it operates on VDD = 0.7 V.

The sections are organized as follows. Section I is an introduction to discuss the importance of the application. Section II discusses the ALU architecture and operations opcodes. Section III details the blocks specifications and implementations. Results are then discussed in Section IV. Finally, Section V concludes the paper.

II. Architecture

Firstly, the Arithmetic Logic Unit (ALU) consists of 5 main blocks, as shown in figure 1, which are control unit, adder, shifter, logic unit, and the final mux. The inputs for the ALU are two inputs, A(4 bit) and B(4bit), and a 4 bit selector input to select the operation that the ALU will perform according to the OP-code. The table below shows the OP-code for the different 16 functions of the ALU.

OP3 OP2 OP1 OP0	Function
0 0 0 0	Add
0 0 0 1	Add with carry
0 0 1 0	Subtract
0 0 1 1	Subtract with borrow
0 1 0 0	1's complement
0 1 0 1	2's complement
0 1 1 0	Increment
0 1 1 1	Decrement
1 0 0 0	Shift right
1 0 0 1	Shift left
1 0 1 0	Rotate right
1 0 1 1	Rotate left
1 1 0 0	AND
1 1 0 1	OR
1 1 1 0	XOR
1 1 1 1	Compare

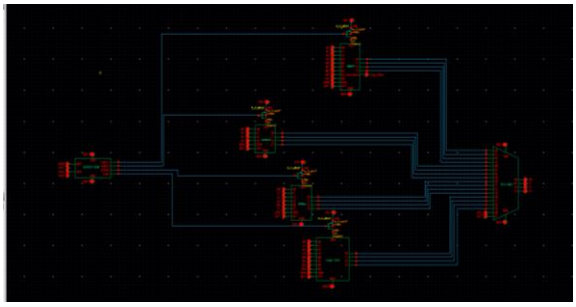


Figure 1. ALU Schematic

III. Blocks

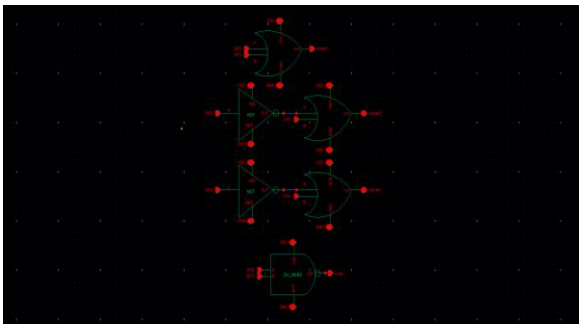
A. *Power Gating (control unit)*

Based on the input OP code, there will only be one block ON and the rest will be off for a given input. Therefore, we designed the control unit block as a block of combinational circuits to operate a desired block and turn off all other blocks in the ALU, reducing power consumption. Power gating is done by using a PMOS transistor to pull up the supply voltage of the needed block.

Figure 2. Power Gating schematic

B. *Shifter*

A barrel shifter using PTL NMOS-based muxes is an optimized 4-bit shifter that supports Rotate Left and Shift Left operations. It consists of 11 PTL-based 2-1 muxes that use a total of 22 NMOS transistors and



eliminates the masking overhead for the most significant bit by supporting only a single direction. The shifter operates by rotating left by k0k1 amount and then propagating the output in case of a Rotate Left operation or discarding k0k1 bits if it is a Shift Left operation. The selection logic for the masking muxes is controlled by specific signals, and the shifter uses level restorers at the output to compensate for the weak 1 output produced by NMOS. Overall, using PTL NMOS-based muxes in a barrel shifter results in a simpler and more efficient design.

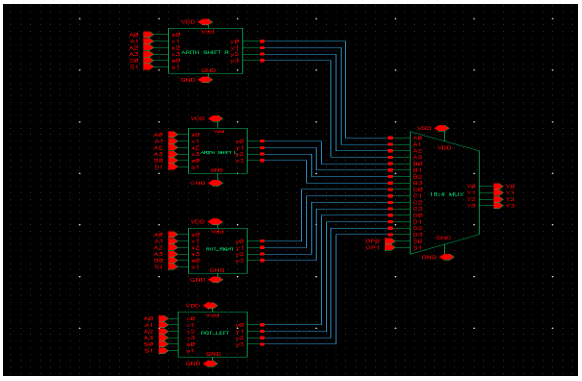


Figure 3. Shifter schematic

C. *Adder*

The adder block is responsible for computing the arithmetic operations in the ALU. The adder is

designed to compute 8 possible operations: add, add with carry, subtract, subtract with borrow, increment, decrement, 1's complement and 2's complement. We implemented the ripple carry adder because it has the least power consumption which suits our application. As shown in Fig. 4, the architecture of the RCA is composed of 4 cascaded full adders, and each input to these adders is controlled using a multiplexer to choose the proper input for each operation of the 8 possible operations.

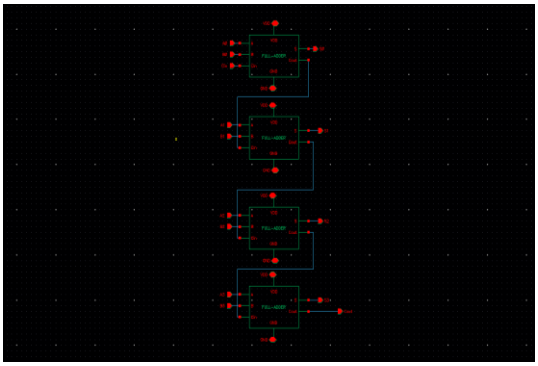


Figure 4. 4-bit Ripple Carry Adder schematic

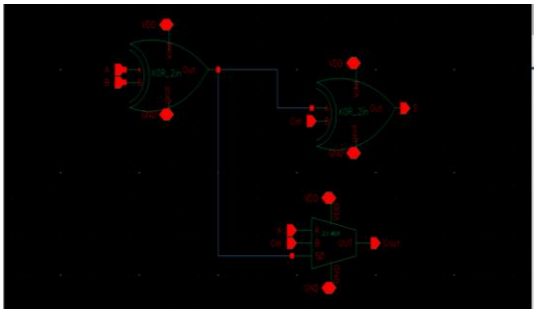


Figure 5. Full Adder schematic

D. Comparator

The comparator implements three functionalities: Set on larger than, set on less than, set on equal. This structure is implemented as shown in Fig. 5 using four 2-input XNOR, one 2- input AND, one 3-input AND, two 4-input AND, one 5-input AND, one 4- input OR, one 2-input NOR, and four inverters.

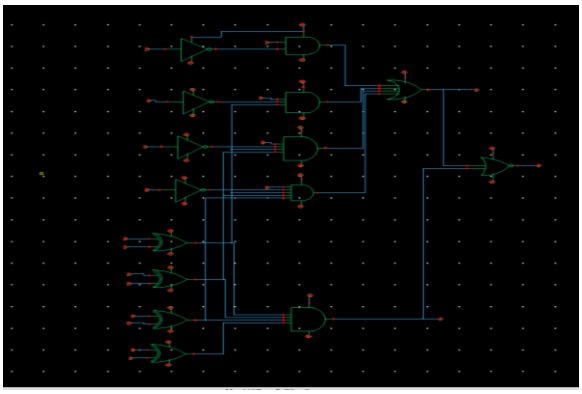


Figure 6. Comparator schematic

E. Logic Unit

As shown in Fig. 7, The logic unit performs 4 logical operations which are AND, OR, XOR, and comparator. We did each operation using 4 logic gates for each operation: one for each bit of the 2 inputs (A and B). We selected the output logic function using 4 x 4:1 Multiplexers that are controlled using two selection lines (S1, S0).

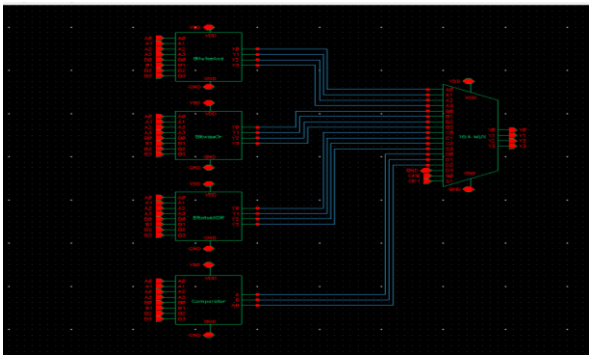


Figure 7. Logic Unit schematic

F. MUXs

As shown in figure 8, we modulated the already existing 4:1 MUXs to make a bigger 16:4 MUX by arranging the inputs in this format, which is used for the final MUX and the MUXs that select the outputs of each block. The 4:1 MUX is constructed in a traditional architecture using 8T + 2 inverters (12 T). It has good enough power and delay characteristics.

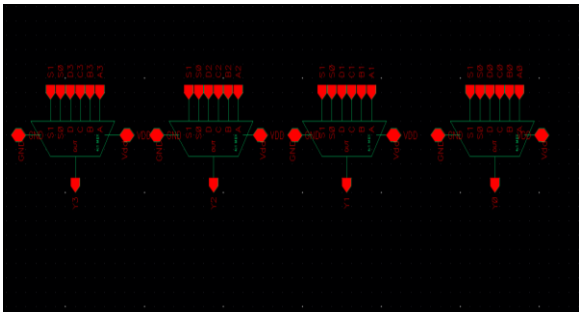


Figure 8. 16:4 MUX schematic

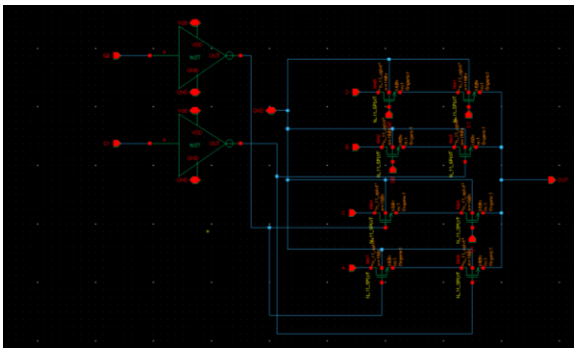


Figure 9. 4:1 MUX schematic

IV. Results and Discussion

A. *Adder Results*

As shown in Fig. 10, The results were computed all over the possible combination of inputs while setting the opcode to operate on subtract with borrow. The average power of the adder is 1.056 µW. This value is computed by sweeping over the whole possible combinations of opcode operations and different combinations of inputs A,B. Furthermore, the tpHL and tpLH were measured to be 220.67ps and 326.26ps respectively.

Average Power	TpHL (ps)	TpLH (ps)
1.056µW	220.67	326.26

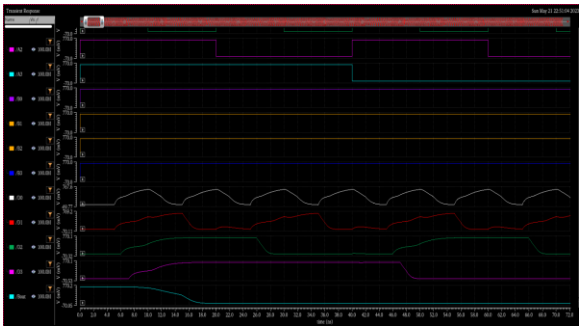


Figure 10. Subtract with borrow output

B. *Shifter Results*

Figure 11 presents the results of a comprehensive analysis of the shifter's performance when rotating left with all possible scenarios of the number of shifts and all combinations of inputs. The average power consumption of the shifter was found to be 0.371 µW, which was calculated by sweeping over all possible combinations of opcode operations and different combinations of inputs A and B. Furthermore, the tpHL and tpLH were measured to be 124.81ps and 112.732ps respectively.

Figure 11. Rotate left waveform

Average Power	TpHL (ps)	TpLH (ps)
0.371 µW	124.81	112.732

C. Comparator

Figure 12 displays the output waveform of the Set on larger than operation. To ensure all possible combinations, the inputs were entered as pulses with multiples of the clock period. The average power consumption of the comparator was found to be 0.716 µW, which was computed by sweeping over all

possible combinations of opcode operations and different combinations of inputs A and B. Also, the tpHL and tpLH were measured to be 195.7ps and 225.1ps respectively. The table below summarizes the power and delay of the comparator block.

Average Power	TpHL (ps)	TpLH (ps)
0.716 µW	195.7	225.1

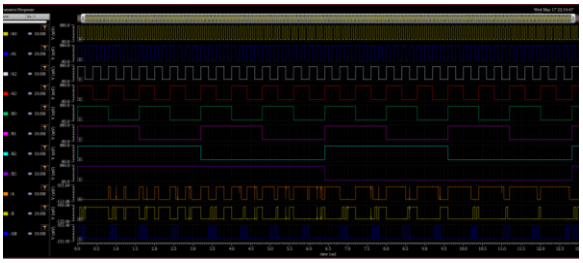


Figure 12. Comparator waveform

D. Logic Unit

Figure 13 depicts the output waveform for the NAND operation, which was computed by entering inputs as pulses with multiples of the clock period to ensure all possible combinations. The critical path for the logic unit is the AND operation, as each bit goes through a NAND gate and then an inverter. The table below summarizes the power and delay of the Logic unit block.

Average Power	TpHL (ps)	TpLH (ps)
0.502 µW	122.7	148.35

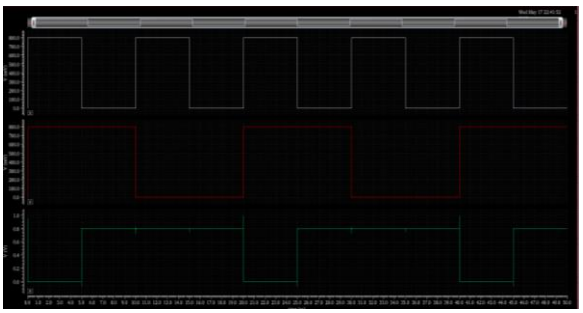


Figure 13. NAND waveform

E. MUX Results

The critical path for the final mux is choosing any of the 3 blocks (adder, comparator, or logic unit) as it goes through one 4_1 mux, 16-4 mux. The table below shows the power and delay of the final mux block:

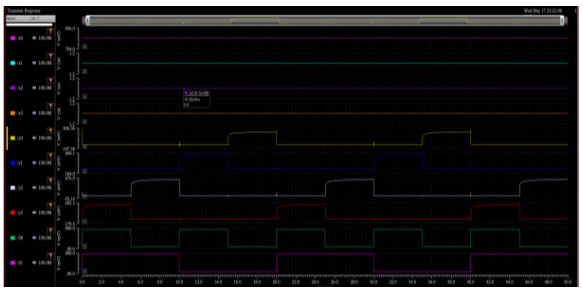


Figure 13. MUX (Shift-Right) waveform

Average Power	TpHL (ps)	TpLH (ps)
93.2 nW	11.93	12.8

F. Control Unit Results

The control unit is the block that acts as the mind of the ALU. It operates a certain block and turns off all other blocks based on the OP code inserted.
The table below shows the power and delay of the control unit block:

Average Power	TpHL (ps)	TpLH (ps)
26.82 nW	169.4	189.6

G. ALU Results

The table below shows the power and delay of the whole ALU:

Average Power	TpHL (ps)	TpLH (ps)
0.664 µW	269.4	375.6

H. Glitches

Initially, the output of the ALU had glitches, particularly during adder operations. These glitches occurred because when cascading full adders in the RCA, the inputs to the next blocks experienced different delays due to different paths. We attempted to solve this issue by adding dummy capacitances to the inputs of the full adders, but this was not an efficient solution. Therefore, we decided to increase the rise and fall time of the input to 100 ps to eliminate the effect of sudden changes in input that allowed glitchy current to flow in the transistor junction capacitance and increase glitch values. As shown in comparator output waveform (Figure 12), increasing the rise and fall times resulted in small glitches in the output of the critical path of our ALU. However, these glitches did not affect the logic of the ALU since their value was less than Vdd/2= 0.35 V, which is the Vm of the next stage.

V. Conclusion

The paper describes the development of a 4-bit ALU with ultra-low power consumption for use in heartbeat regulators. The ALU is built using static CMOS and pass transistor logic, and operates at a supply voltage of 0.7 V and frequency of 100MHz. On average, the design consumes only 0.664 μW of power and has a delay time of 323 psec.

VI. Recommendations

A more efficient multi-core-like system is theorized. This system should use 4 1-bit ALUs working together. They would operate also with a VDD lower than Vth. A 1 bit ALU is a much simpler circuit than a monolithic 4 bit ALU. Hence, it can run with no issues on such voltage, saving much power. Moreover, using a multi-core-like design will enable the ALU to run at an overall slower clock but with the same throughput. In addition, a more power efficient comparator could be designed, which has fewer stages; thus, power consumption decreases.

VII. References

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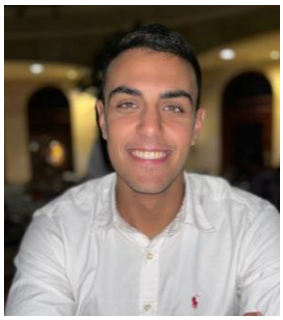

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